

3- 5 cells Li-ion/polymer battery protection IC

MM3575 series

Outline

The MM3575 series are protection IC using high voltage CMOS process for overcharge, overdischarge and overcurrent protection of the rechargeable Lithium-ion or Lithium-polymer battery. The overcharge, overdischarge, discharging overcurrent, charging overcurrent, cell balance and from V5 to V3 pin disconnect of the rechargeable from 3 to 5cell Lithium-ion or Lithium-polymer battery can be detected. By using cascade connection, it is also possible to protect 6 or more cells rechargeable Lithium-ion battery. And the regulator can be constructed by using external Nch MOS FET. The internal circuit of IC is composed by the voltage detector, the reference voltage source, delay time control circuit, and the logical circuit, etc.

Features

- 1) Range and accuracy of detection/release voltage
 - Overcharge detection voltage
 - Overcharge release voltage
 - Overdischarge detection voltage
 - Overdischarge release voltage
 - Discharging overcurrent detection voltage1
 - Discharging overcurrent detection voltage2
 - Short detection voltage
 - Charging overcurrent detection voltage
 - · Cell balance detection voltage
- 2) Range of detection delay time
 - Overcharge detection delay time
 - Overdischarge detection delay time
 - Discharging overcurrent detection delay time1
 - Discharging overcurrent detection delay time2
 - Short detection delay time
 - Charging overcurrent detection delay time
 - · Disconnect detection delay time
 - · Cell balance detection delay time
- 3) 0V battery charge function

Selection from "Prohibition" or "Permission"

- 4) Protected operation can be detect of V5 to V1 pin disconnection
- 5) The setting for three cell, for four cell, and for five cell protection can be set with the SEL pin.
- 6) The charge and discharge of the battery can be controlled with SDC pin and SOC pin.
- 7) Power save mode built-in



The details listed here are not a guarantee of the individual products at the time of ordering. When using the products, you will be asked to check their s

(Unless otherwise specified, $Ta=25^{\circ}$)

3.6V to 4.5V, 5mV steps 3.4V to 4.5V, 50mV steps 2.0V to 3.0V, 50mV steps 2.0V to 3.5V, 50mV steps +30mV to +300mV, 5mV steps 2 or 4 times of VDET3-1 4 or 8 times of VDET3-1 -300mV to -20mV, 5mV step 3.6V to 4.5V, 5mV steps

Selection from 0.25s, 1.0s, 1.2s, 4.1s

Selection from 0.25s, 1.0s, 1.2s, 4.1s

Setting by a capacitor of COC pin.

Setting by a capacitor of COC pin. Selection from 100us, 200us, 300us

Setting by a capacitor of COC pin.

Selection from 0.1s, 0.25s, 0.5s

Selection from 25ms, 50ms, 100ms

Accuracy±50mV Accuracy±80mV Accuracy±100mV Accuracy±15mV Accuracy±15% Accuracy±100mV Accuracy±10mV Accuracy±30mV (Ta=0~50℃)

Accuracy±25mV (Ta=0~50℃)





9) Low current consumption

 VDD pin current consumption(Vcell=4.3V) 	Typ. 25.0uA Max. 35.0uA
 VDD pin current consumption(Vcell=3.5V) 	Typ. 20.0uA Max. 30.0uA
 VDD pin current consumption(Vcell=2.0V) 	Typ. 10.0uA Max. 15.0uA
· VDD pin current consumption at power save1(Vcell=3.5V)	Typ. 12.0uA Max. 16.0uA
· VDD pin current consumption at power save2(Vcell=3.5V)	Typ. 4.0uA Max. 6.0uA

10 Package type

・VSOP-24A

7.90 × 7.60 × 1.25 [mm]

Pin explanations

VSOP-24A	Pin No.	Symbol	Function
	1	VDD	The input terminal of the power supply of IC.
	2	SOC	The control terminal of output over charge detection.
	3	SDC	The control terminal of output over discharge detection.
	4	VM2	Input terminal connected to charger negative voltage.
	5	OV	Charge control output terminal. Output type is Pch open drain.
	6	VM1	Input terminal connected to discharge voltage.
1 0 24	7	DCHG	Discharge control output terminal. Output type is CMOS.
	8	COC	A terminal which sets delay time of overcurrent.
2 23	9	CS1	Input of overcurrent detection.
3 22	10	CS2	Common terminal of overcurrent detection circuit.
	11	DRIVE	The drive terminal of FET for regulator.
4 21	12	REG_IN	The input terminal of regulator voltage
5 20	13	SEL	This pin is for changing function for 3cell in series or 4cell in series , 5cell in series.
6 TOP VIEW 19 7 18	14	VSS	The input terminal of the negative voltage of V1 cell. The input terminal of the ground of IC.
8 17	15	OUT1	V1 cell balance control output terminal.
8 9 16	16	V1	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell.
10 15	17	OUT2	V2 cell balance control output terminal.
11 14	18	V2	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell.
12 13	19	OUT3	V3 cell balance control output terminal.
	20	V3	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell.
	21	OUT4	V4 cell balance control output terminal.
	22	V4	The input terminal of the positive voltage of V4 cell, and the negative voltage of V5 cell.
	23	OUT5	V5 cell balance control output terminal.
	24	V5	The input terminal of the positive voltage of V5 cell.



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
VDD pin supply voltage	V _{VDDMAX}	VSS-0.3	VSS+30.0	V
Voltage between the input terminals of voltage of battery	V _{cellMAX}	-0.3	10.0	V
VM1 pin supply voltage	$V_{\rm VM1MAX}$	VDD-30	VDD+0.3	V
VM2 pin supply voltage	V_{VM2MAX}	VDD-30	VDD+0.3	V
OV pin supply voltage	V _{OVMAX}	VDD-30	VDD+0.3	V
DCHG pin supply voltage	V _{DCHGMAX}	VSS-0.3	VDD+0.3	V
OUT1~5 pin supply voltage/ _{OUT1~5MAX}			VDD+0.3	V
Storage temperature	T _{STG}	-55	125	°

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating ambient temperature	T _{OPR}	-40	85	C
Operating voltage	V _{OPR}	VSS+3.5	VSS+22.5	V

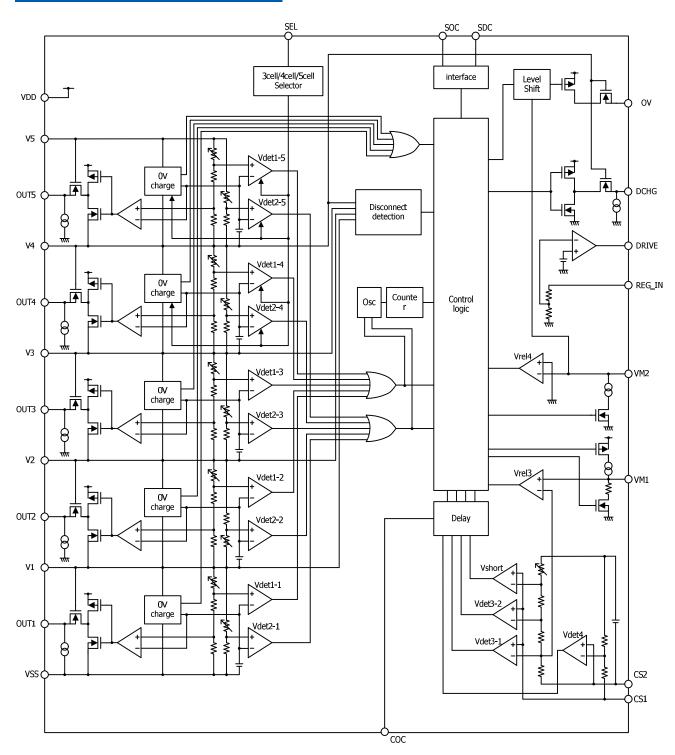
Electrical characteristics

					(特記なき場合、1	[a=25℃)
Parameter	Symbol	Note	Min	Тур	Max	Unit
		Current consumption				
Current consumption1 (VDD)	I _{DD1}	Vcell=4.3V	-	25.0	35.0	uA
Current consumption2 (VDD)	I_{DD2}	Vcell=3.5V	-	20.0	30.0	uA
Current consumption3 (VDD)	I _{DD3}	Vcell=2.0V, V-=VSS	-	10.0	15.0	uA
Power save 1 Current consumption (VDD)	I_{DD_PS1}	Vcell=3.5V, SDC,SOC=OPEN	-	12.0	16.0	uA
Power save 2 Current consumption (VDD)	$I_{DD_{PS2}}$	Vcell=3.5V, SDC,SOC=VSS	-	4.0	6.0	uA
		Detection / Release volta	ge			
Overcharge detection voltage	V_{DET1}	Ta=0∼50℃	Typ-0.025	V _{DET1}	Typ+0.025	V
Overcharge release voltage	V_{REL1}		Тур-0.050	V _{REL1}	Typ+0.050	V
Cell balance detection voltage	V_{DET_CB}	Ta=0∼50℃	Тур-0.030	V_{DET_CB}	Typ+0.030	V
Overdischarge detection voltage	V _{DET2}		Тур-0.080	V _{DET2}	Typ+0.080	V
Overdischarge release voltage	V_{REL2}		Тур-0.100	V _{REL2}	Typ+0.100	V
Discharging overcurrent detection voltage 1	V _{DET3-1}		Typ-0.015	V _{DET3-1}	Typ+0.015	V
Discharging overcurrent detection voltage 2			Typ-15%	V _{DET3-2}	Typ+15%	V
Short detection voltage	V _{SHORT}		Тур-0.100	V _{SHORT}	Typ+0.100	V
Charging overcurrent detection voltage	V _{DET4}		Тур-0.010	V _{DET4}	Typ+0.010	V
		Detection voltage delay ti	me			
Overcharge detection delay time	t _{VDET1}		Typ-25%	t _{VDET1}	Typ+25%	S
Cell balance detection delay time	t_{VDET_CB}		Typ-25%	t_{VDET_CB}	Typ+25%	S
Overdischarge detection delay time	t _{VDET 2}		Typ-25%	t _{VDET 2}	Typ+25%	S
Discharging overcurrent detection delay time 1	t _{VDET3-1}		Typ-30%	t _{VDET3-1}	Typ+30%	ms
Discharging overcurrent detection delay time 2	t _{VDET3-2}		Typ-30%	t _{VDET3-2}	Typ+30%	ms
Short detection delay time	t _{short}		Typ-50%	t _{short}	Typ+50%	us
Charging overcurrent detection delay time	t _{VDET4}		Typ-30%	t _{VDET4}	Typ+30%	ms
Disconnect detection delay time	t _{vdet5}		Typ-25%	t _{vdet5}	Typ+25%	ms





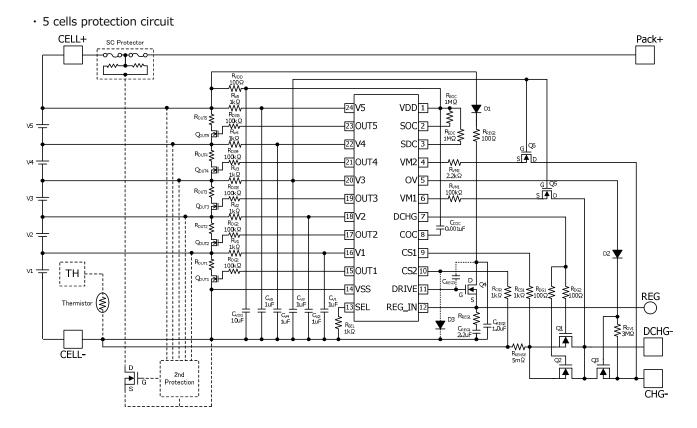
Block diagram







Typical application circuit

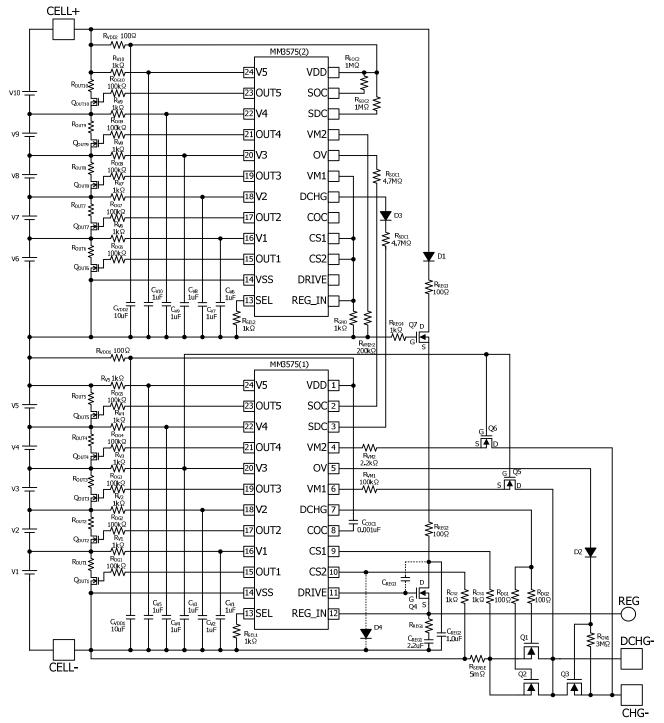


※ This circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. assumes no responsibility for any trouble or damage as a result of the use of this circuits.





• 10 cells protection circuit



% This circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied. Mitsumi Electric Co., Ltd. assumes no responsibility for any trouble or damage as a result of the use of this circuits.