3 to 4 cells lithium–ion/lithium–polymer battery secondary protection IC

MM3625 series

Outline

The MM3625 series are secondary protection IC using high voltage CMOS process for overcharge protection of the rechargeable Lithium-ion or Lithium-polymer battery. The high accuracy overcharge detection of each cell of the rechargeable 3,4 cell Lithium-ion or Lithium-polymer battery is possible. The IC has a regulator and it is possible to stop regulator by detected overdischarge.The internal circuit of IC is composed by the voltage detector, the reference voltage source, delay time control circuit, the logical circuit, and regulator circuit etc.

Features

(Unless otherwise specified,Ta=25℃)

1) Range and accuracy of detection/release voltage

・Overcharge detection voltage	3.6V to 4.5V, 5mV steps	Accuracy±25mV
・Overcharge release voltage	3.4V to 4.5V, 50mV steps	Accuracy±50mV
・VOU OFF voltage	2.1V to 3.2V, 50mV steps	Accuracy±50mV

2) Range of detection delay time

・Overcharge detection delay time	$1ms\sim(1ms\times2^{n1})+(1ms\times2^{n2})+(1ms\times2^{n3})$
・Overcharge release delay time	$1ms\sim(1ms\times2^{n1})$
・VOUT OFF delay time	$1ms\sim(1ms\times2^{n1})+(1ms\times2^{n2})+(1ms\times2^{n3})$

*n1,n2 and n3 can select two arbitrary integers between 0 to 17.
(However n1≠n2≠n3)

3) Range of regulator output voltage

・VOUT pin output voltage	1.8V to 5.0V, 50mV steps

4) The setting for three cell and for four cell protection can be set with the SEL pin

5) Regulator output can be control with the EN pin

6) FUSE pin can control with the CTL pin

7) Low current consumption

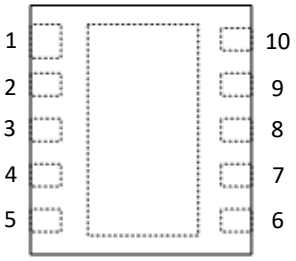
・Current consumption1 (VCELL=3.5V)	Typ. 4.5uA, Max. 6.5uA
・Current consumption2 (VCELL=2.5V)	Max. 0.1uA

8) Package type

・PLP-10A	2.70 × 2.50 × 0.6 [mm]

Mitsumi Electric CO.,LTD.
Semiconductor Business Division
Strategy Engineering Department
tel:+81-46-230-3470

Pin explanations

PLP-10A	Pin No.	Symbol	Function
	1	VDD	The input terminal of the power supply of IC andthe positive voltage of V4 cell .
	2	V3	The input terminal of the positive voltage of V3 cell, and the negative voltage of V4 cell.
	3	V2	The input terminal of the positive voltage of V2 cell, and the negative voltage of V3 cell.
	4	V1	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell.
	5	VSS	The input terminal of the negative voltage of V1 cell. The input terminal of the ground of IC.
	6	SEL	This terminal is for changing function for 3cell in series or 4cell in series.
	7	VOUT	Regulator output terminal.
	8	FUSE	Charge control output terminal. Output type is CMOS.
	9	EN	Regulator output ON control terminal.
	10	CTL	FUSE output ON control terminal.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
VDD pin supply voltage	V_{VDDMAX}	VSS-0.3	VSS+20	V
Voltage between the input pins of voltage of battery	$V_{cellMAX}$	-0.3	10	V
FUSE pin	$V_{FUSEMAX}$	VSS-0.3	VDD+0.3	V
VOUT pin output voltage	V_{OUT_MAX}	VSS-0.3	VSS+20	V
Storage temperature	T_{STG}	-55	125	℃

Recommended Operating Conditions

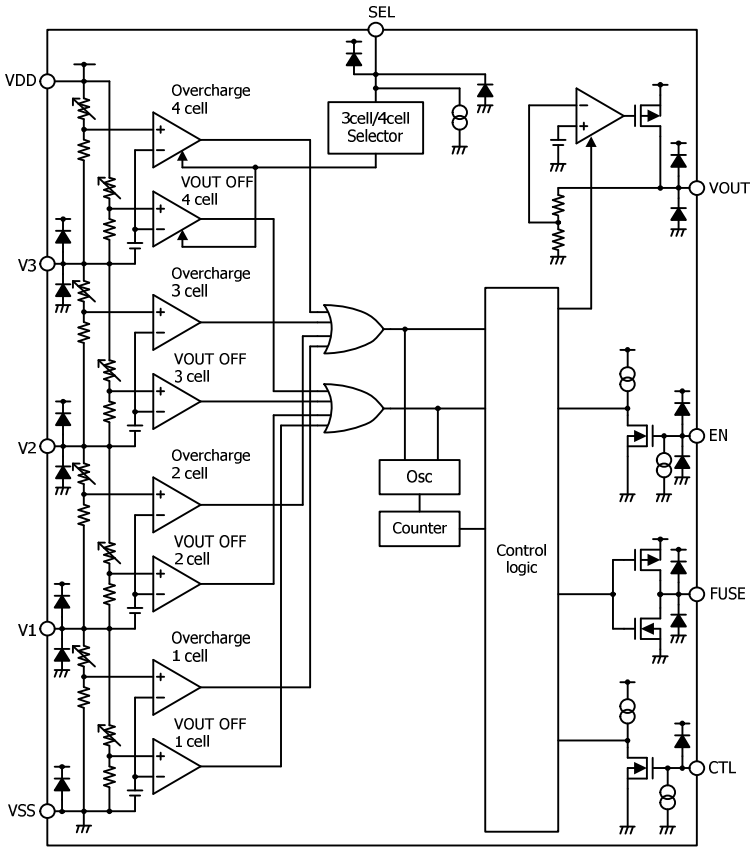
Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_{OPR}	-40	85	℃
Supply Voltage	V_{OPR}	VSS+4.5	VSS+18	V

Electrical characteristics

(Unless otherwise specified,Ta=25℃)

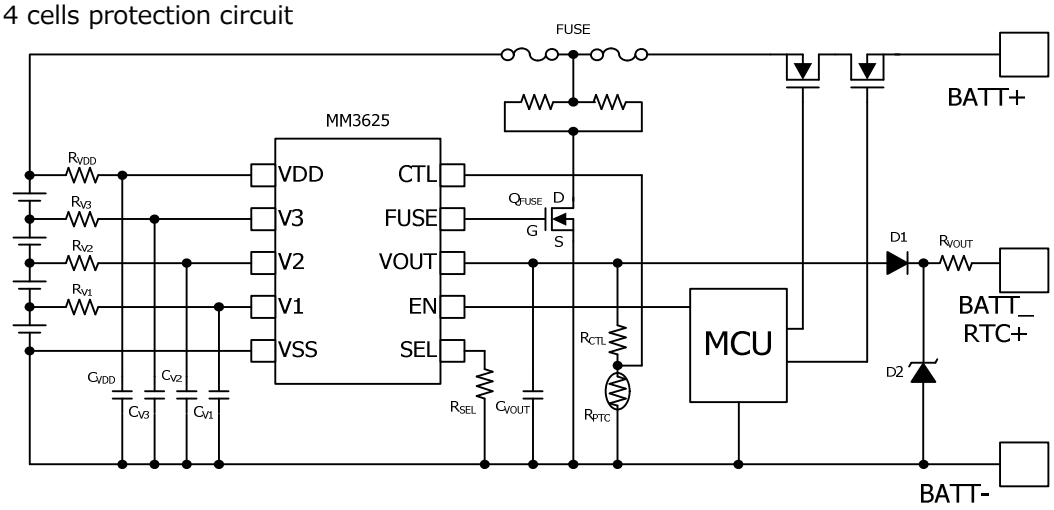
Parameter	Symbol	Note	Min	Typ	Max	Unit
Input/Output pin						
EN input voltage L	$V_{EN}L$	V_{CELL}=3.5V	0.0	-	0.5	V
EN input voltage H	$V_{EN}H$	V_{CELL}=3.5V	2.5	-	-	V
EN pin pulldown current	I_{EN}	V_{CELL}=3.5V	-	0.150	0.225	uA
SEL input voltage L	$V_{SEL}L$	V_{CELL}=3.5V	0.0	-	0.5	V
SEL input voltage H	$V_{SEL}H$	V_{CELL}=3.5V	VDD-0.5	-	VDD	V
SEL pin pulldown current	I_{SEL}	V_{CELL}=3.5V	-	0.150	0.225	uA
CTL input voltage L	$V_{CTL}L$	V_{CELL}=3.5V	0.50	0.65	0.80	V
CTL input voltage H	$V_{CTL}H$	V_{CELL}=3.5V	1.35	1.60	1.85	V
CTL pin pulldown current	I_{CTL}	V_{CELL}=3.5V	-	0.150	0.225	uA
FUSE pin output voltage H	$V_{FUSE}H$	V_{CELL}=4.3V V_{CTL}=VDD	16.6	16.9	-	V
FUSE pin output voltage L	$V_{FUSE}L$	V_{CELL}=3.5V	-	0.3	0.6	V
VOUT pin output voltage	V_{OUT}	I_{OUT}=20uA	Typ-0.1	V_{OUT}	Typ+0.1	V
Current consumption						
Consumption current 1	I_{DD1}	VCELL=3.5V	-	4.5	6.5	uA
Consumption current 2	I_{DD2}	VCELL=2.5V	-	-	0.1	uA
V3 pin input current	I_{V3}	VCELL=3.5V	-300	-	300	nA
V2 pin input current	I_{V2}	VCELL=3.5V	-300	-	300	nA
V1 pin input current	I_{V1}	VCELL=3.5V	-300	-	300	nA
Detection/Release voltage						
Overcharge detection voltage	V_{DET1}	Ta=0～+50℃	Typ-0.025	V_{DET1}	Typ+0.025	V
Overcharge release voltage	V_{REL1}		Typ-0.050	V_{REL1}	Typ+0.050	V
Standby Voltage	V_{DET2}		Typ-0.050	V_{DET2}	Typ+0.050	V
Detection/Release delay time						
Overcharge detection delay time	t_{VDET1}		Typ*0.75	t_{VDET1}	Typ*1.25	s
Overcharge release delay time	t_{VREL1}		Typ*0.75	t_{VREL1}	Typ*1.25	ms
VOUT OFF delay time	t_{VDET2}		Typ*0.75	t_{VDET2}	Typ*1.25	ms
FUSE pin output delay time (CTL)	t_{CTL_DET}		7.5	10.0	12.5	ms
FUSE pin output release delay time (CTL)	t_{CTL_REL}		3.0	4.0	5.0	ms

Block diagram



Typical application circuit

・4 cells protection circuit



・These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied.

・Mitsumi Electric Co., Ltd. assumes no responsibility for any trouble or damage as a result of the use of these circuits.

・When connecting a battery, it recommends where EN pin is inputed to a VSS pin level, a battery is connected in an order from VDD pin or VSS pin.