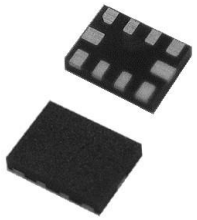
16bit Delta-sigma ADC
MM4113A16, MM4114A16, MM4115A16 data sheet

OUTLINE



The MM4113A16, MM4114A16, and MM4115A16 are high-precision, low-power, 16-bit delta sigma analog-to-digital converter ICs with I2C compatible interface.
MM4115 can measure two differential inputs or four single-ended inputs by the internal input multiplexer.

MM4114A16 and MM4115A16 have a build-in PGA (programmable gain amplifier), and are well suited for sensor measurement applications because having input voltage range switching function. This ADC operates in either continuous-conversion mode or single-shot conversion mode.

FEATURE

- 3 products line-up : MM4113, MM4114, MM4115
- 16bit Resolution (no missing codes)
- Single-Cycle Setting
- Programmable Data Rate：8 SPS ~ 860 SPS
- Multiplexer allows 4 single inputs and 2 differential inputs (MM4115)
- Input voltage range can be changed by installing PGA (MM4114, MM4115)
- Installing Programmable Comparator (MM4114, MM4115)
- Low Current Consumption ： 150 μA (Continuous-Conv. Mode)
- Ultra Small SQFN Package ： 2.0(W) x 1.5(D) x 0.4(H) mm
- I2C Interface : 4 different slave address are selectable
- Operation temperature : -40 ℃ ～ +125 ℃

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CONTENT

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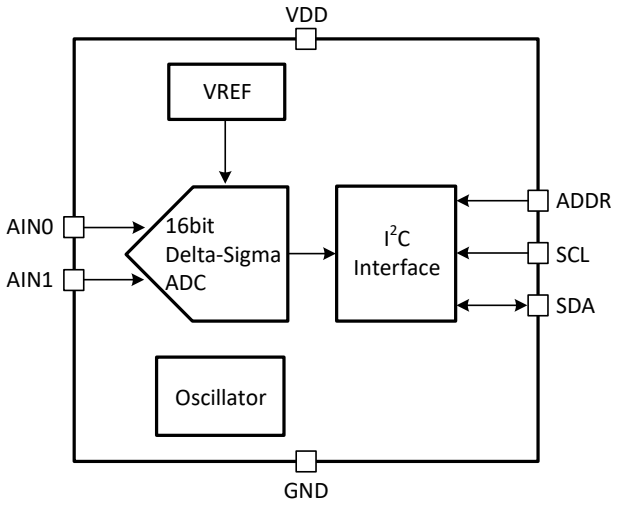
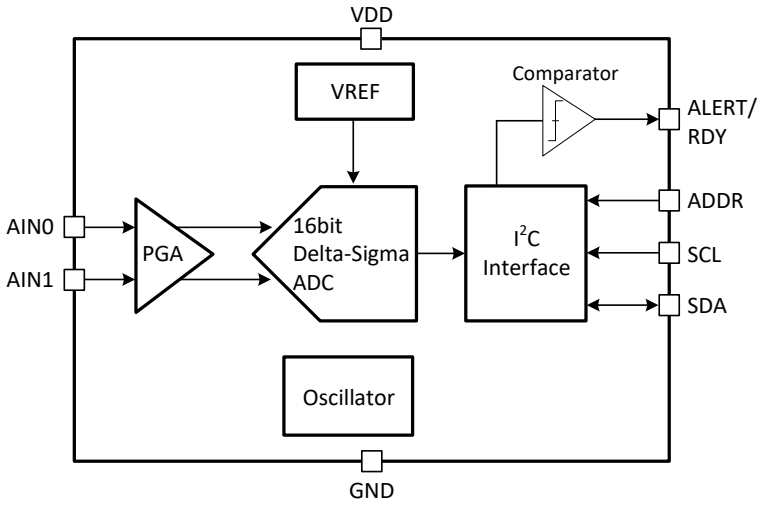
BLOCK DIAGRAM

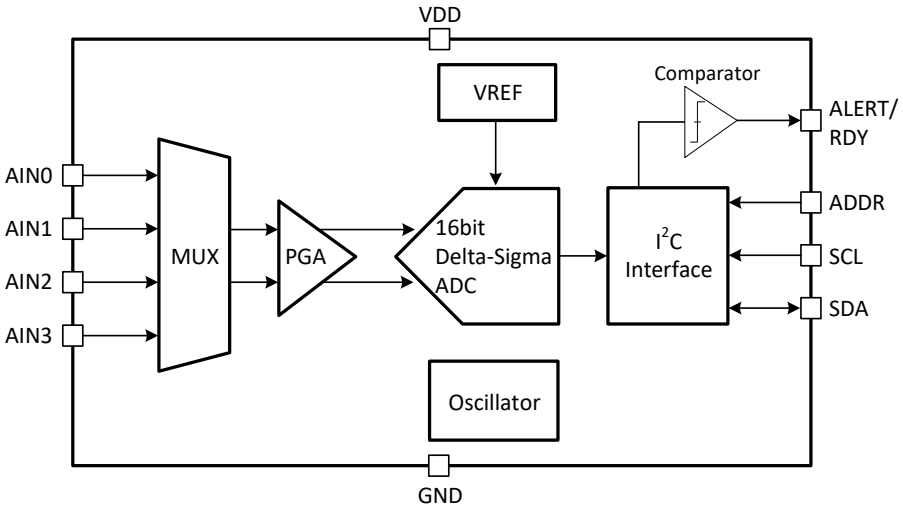
MM4113



MM4114



MM4115



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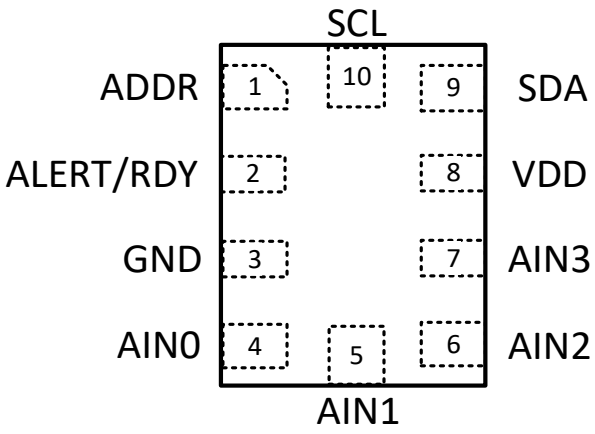
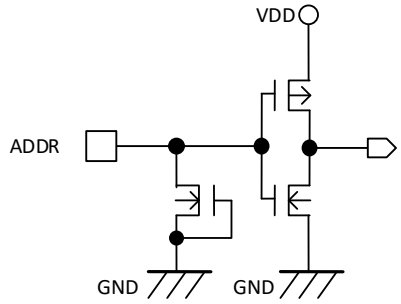
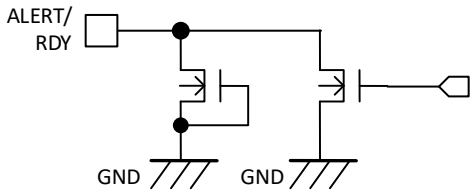
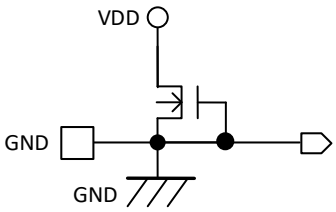
PIN CONFIGURATION



TERMINAL EXPLANATIONS

NO	PIN SYMBOL	TYPE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
1	ADDR	Input		I2C slave address select
2	ALERT/RDY	Output		Comparator output or conversion ready (Open Drain Output) ※MM4113 : Not connected
3	GND	Supply		Ground

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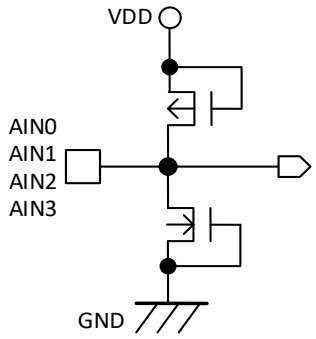
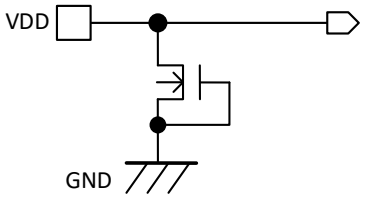
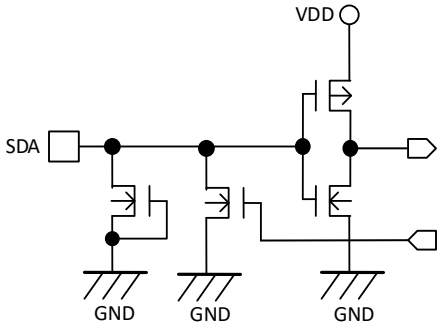
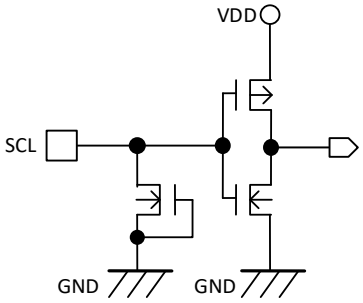
NO	PIN SYMBOL	TYPE	INTERNAL EQUIVALENT CIRCUIT	FUNCTION
4	AIN0	Input		Analog input 0
5	AIN1			Analog input 1
6	AIN2			Analog input 2 ※MM4113, MM4114 : Not connected
7	AIN3			Analog input 3 ※MM4113, MM4114 : Not connected
8	VDD	Supply		Power Supply
9	SDA	I/O		Data input/output through I2C serial communication
10	SCL	Input		Clock input through I2C serial communication

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ABSOLUTE MAXIMUN RATINGS

Unless otherwise specified
Ta = 25 ℃

ITEM	SYMBOL	MIN.	MAX.	UNIT
Power supply voltage	VDD_{abx}	-0.3	7.0	V
Analog input voltage (note[1])	V_{AINabx}	GND – 0.3	VDD + 0.3	V
Digital input voltage (note[2])	V_{DINabx}	GND – 0.3	5.5	V
Continuous input current	Icntabx	-10	10	mA
Operating ambient temperature	Ta_{MAX}	-40	125	℃
Junction temperature	Tj_{MAX}	-40	150	℃
Storage temperature	T_{stg}	-60	150	℃
Power dissipation (on board) (note[3])	P_d	-	270	mW

note[1] : AIN0, AIN1, AIN2, AIN3
note[2] : ADDR, ALERT/RDY, SDA, SCL
note[3] : Conditions: 10 mm x 12 mm, t = 1.6 mm, single-sided board, and copper foil 10%

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified
Ta = 25 ℃

ITEM	SYMBOL	MIN.	MAX.	UNIT
Operating ambient temperature	T_{op}	-40	125	℃
Operating voltage	V_{op}	2.0	5.5	V
Analog absolute input voltage (note[1])	V_{AINx}	GND	VDD	V
Full-scale input voltage range (note[2])	FSR	±0.256	±6.144	V
Digital input voltage (note[3])	V_{DINx}	GND	5.5	V

note[1] : AIN0, AIN1, AIN2, AIN3
note[2] : AINP and AINN indicate the selected positive and negative inputs.
note[3] : ADDR, ALERT/RDY, SDA, SCL

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified

MIN./MAX. Specifications : T_a = –40 to 125 °C, VDD = 3.3 V, DR = 8 SPS, FSR = ±2.048 V

TYP. Specifications : T_a = 25 °C, VDD = 3.3 V, DR = 8 SPS, FSR = ±2.048 V

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ANALOG INPUT						
Common-mode input impedance	Zcom	FSR = ±6.144 V	-	>100	-	MΩ
		FSR = ±4.096 V	-	>100	-	
		FSR = ±2.048 V	-	>100	-	
		FSR = ±1.024 V	-	>100	-	
		FSR = ±0.512 V	-	>100	-	
		FSR = ±0.256 V	-	>100	-	
Differential input impedance	Zdiff	FSR = ±6.144 V	-	15	-	MΩ
		FSR = ±4.096 V	-	10	-	
		FSR = ±2.048 V	-	5	-	
		FSR = ±1.024 V	-	2.5	-	
		FSR = ±0.512 V	-	1.3	-	
		FSR = ±0.256 V	-	0.6	-	
SYSTEM PERFORMANCE						
Resolution (note[1])	Reso		16	-	-	Bits
Data rate	DR		8, 16, 32, 64, 128, 250, 475, 860			SPS
Data rate variation	DR_var	ALL data rates	-10	-	10	%
Integral nonlinearity (note[2])	INL	DR = 8 SPS, FSR = ±2.048 V, Ta = 25 °C	-	1	3	LSB
		DR = 8 SPS, FSR = ±2.048 V	-	-	5	LSB
Offset error	Erof	FSR = ±2.048 V differential inputs	-3	±1	3	LSB
		FSR = ±2.048 V single-ended inputs	-	±3	-	LSB
Offset drift over temperature	|ΔErof_t|	FSR = ±2.048 V	-	0.005	-	LSB/°C
Long-term offset drift	Erof_ltr	FSR = ±2.048 V Ta = 125 °C, 1000 hours	-	±1	-	LSB
Offset power-supply rejection	PSRof	FSR = ±2.048 V Supply variation	-	1	-	LSB/V
Offset channel match	Erof_ch	Match between any two inputs	-	3	-	LSB
Gain error	Erga	FSR = ±2.048 V Ta = 25°C	-0.15	0.01	0.15	%
Gain drift over temperature |Erga(-40°C)-Erga(125°C) |/165°C	|ΔErga_t|	FSR = ±0.256 V	-	7	-	ppm/°C
		FSR = ±2.048 V	-	5	40	
		FSR = ±6.144 V	-	5	-	

note[1] : Ensured by design.

note[2] : Best-fit INL; covers 99% of full-scale

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Unless otherwise specified

MIN./MAX. Specifications : T_a = –40 to 125 °C, VDD = 3.3 V, DR = 8 SPS, FSR = ±2.048 V

TYP. Specifications : T_a = 25 °C, VDD = 3.3 V, DR = 8 SPS, FSR = ±2.048 V

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SYSTEM PERFORMANCE						
Long-term gain drift	Erga_ltr	FSR = ±2.048 V Ta = 125 °C, 1000 hours	-	±0.05	-	%
Gain power-supply rejection	PSRga	FSR = ±2.048 V Supply variation	-	80	-	ppm/V
Gain match	Erga_re	Match between any two gains	-	0.02	0.1	%
Gain channel match	Erga_ch	Match between any two gains	-	0.05	0.1	%
Common-mode rejection ratio	CMRR	At DC, FSR = ±0.256 V	-	105	-	dB
		At DC, FSR = ±2.048 V	-	100	-	
		At DC, FSR = ±6.144 V	-	90	-	
		f_{CM} = 60 Hz, DR = 8 SPS	-	105	-	
		f_{CM} = 50 Hz, DR = 8 SPS	-	105	-	
DIGITAL INPUT/OUTPUT DC Characteristics						
High-level input voltage	V_{IH}		0.7VDD	-	VDD	V
Low-level input voltage	V_{IL}		GND	-	0.3VDD	V
Low-level output voltage	V_{OL}	I_{OL} = 3mA	GND	0.15	0.4	V
Input leakage current	I_{ILH}	GND < V_{DINx} < VDD	-10	-	10	µA
POWER SUPPLY						
Supply current	Idds	Power-down, Ta = 25°C	-	0.5	2.0	µA
	Iddo	Operating, Ta=25°C	-	150	200	
		Operating	-	-	300	
Power dissipation	Pop	VDD = 5.0 V	-	0.9	-	mW
		VDD = 3.3 V	-	0.5	-	
		VDD = 2.0 V	-	0.3	-	

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TIMING CHARACTERISTICS : I2C

Unless otherwise specified,
Ta = -40 to 125 °C, VDD = 2.0 to 5.5 V

ITEM	SYMBOL	FAST MODE			HIGH-SPEED MODE			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I2C Clock frequency	F_{SCL}	0.01	-	0.4	0.01	-	3.4	MHz
Bus free time between START and STOP condition	T_{BUF}	600	-	-	160	-	-	ns
Hold time after repeated START condition.	T_{HDSTA}	600	-	-	160	-	-	ns
Setup time for a repeated START condition	T_{SUSTA}	600	-	-	160	-	-	ns
Setup time for STOP condition	T_{SUSTO}	600	-	-	160	-	-	ns
Data hold time	T_{HDDAT}	0	-	-	0	-	-	ns
Data setup time	T_{SUDAT}	100	-	-	10	-	-	ns
Low period of the SCL clock signal	T_{LOW}	1300	-	-	160	-	-	ns
High period of the SCL clock signal	T_{HIGH}	600	-	-	60	-	-	ns
Rise time for both SDA and SCL signals (note[1])	T_R	-	-	300	-	-	160	ns
Fall time for both SDA and SCL signals (note[1])	T_F	-	-	300	-	-	160	ns

note[1] : For the maximum values in high-speed mode, the load capacity of bus line must be less than 400 pF.

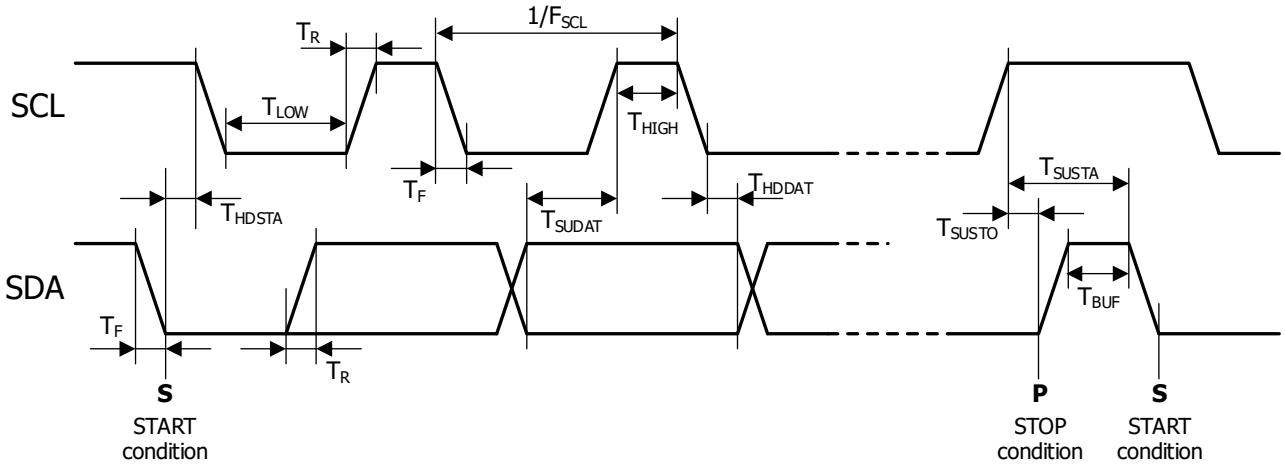

Figure 1. I2C Interface Timing

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DETAILED DESCRIPTION

OVERVIEW

The MM4113, MM4114, and MM4115 are 16-bit delta sigma analog-to-digital converter. This consists of a ΔΣ ADC core with an internal reference voltage source, a clock oscillator, and an I2C interface circuit.

MM4114 and MM4115 also have a programmable gain amplifier (PGA) and digital comparator.

FEATURE DESCRIPTION

MULTIPLEXER

MM4115 is equipped with an input multiplexer as shown in Figure 2. This multiplexer can measure two differential signals or four single-ended signals by setting MUX[2:0] in Config register. When measuring the single-ended signal, the negative input of the ADC is internally connected to GND using a switch in the multiplexer.

MM4113 and MM4114 do not have an input multiplexer. It can measure either 1ch differential signals or 1ch single-end signals. For single-end measurements, connect the AIN1 pin externally to the GND.

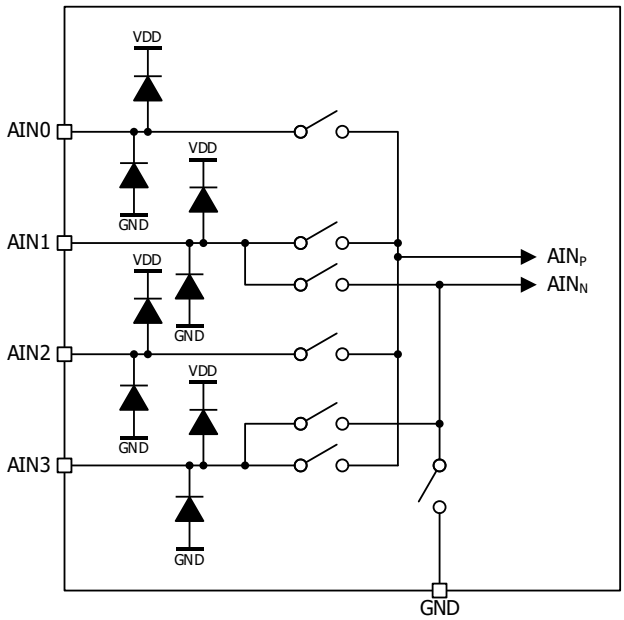

Figure 2. Input Multiplexer

Table 1. Input signal selection

MUX[2:0]	AIN_P	AIN_N
0	AIN0	AIN1
1	AIN0	AIN1
2	AIN1	AIN3
3	AIN2	AIN3
4	AIN0	GND (note$_1$)
5	AIN1	GND (note$_1$)
6	AIN2	GND (note$_1$)
7	AIN3	GND (note$_1$)

Note[1] : AINN is connected internally

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ANALOG INPUT CIRCUIT

MM4113, MM4114, and MM4115 use a switched-capacitor input stage to sample the voltage between AINP and AINN. In this IC, the input signal is sampled at 250 kHz by the built-in oscillator. The structure of the sampling circuit of the analog input stage can be expressed by the equivalent circuit of Figure 3, and switching is performed at the timing shown in Figure 4. Charge / discharge during this sampling period causes a very small transient current to flow through the analog input pins, and the mean of this current can be used to calculate the effective input impedance (Zcom or Zdiff). The impedance of the analog input may affect the measurement accuracy. The impedance of the signal source should be considered in light of the standard value of the input impedance.

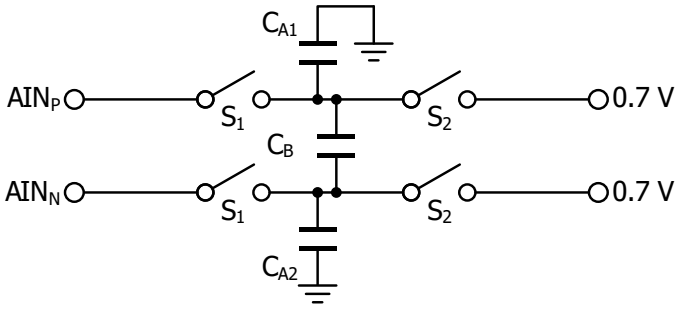

Figure 3. Simplified Analog Input Circuit

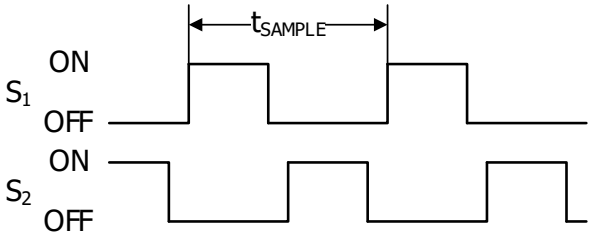

Figure 4. S1 and S2 Switching Timing

FULL−SCALE RANGE（FSR）AND LSB SIZE

For MM4114 and MM4115, a programmable gain amplifier (PGA) is implemented before the ΔΣADC. This allows the magnitude of the minimum resolution (LSB) to be set. Table 2 shows the relation between the full-scale range (FSR = ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, ±0.256 V) and the LSB. Full scale can be set by PGA[2:0] bits in Config register. In addition, LSB can be calculated from FSR by the equation below.

LSB SIZE = FSR / 2^{16}

Table 2. Full-Scale Range and Corresponding LSB Size

PGA[2:0]	FSR	LSB SIZE
0	±6.144 V	187.5 μV
1	±4.096 V	125 μV
2	±2.048 V	62.5 μV
3	±1.024 V	31.25 μV
4	±0.512 V	15.625 μV
5 - 7	±0.256 V	7.8125 μV

The analog input voltages must never exceed the analog input voltage limits given in the Absolute Maximum Ratings. If the power supply voltage is less than or equal to the full scale range, the full scale output code of the ADC cannot be obtained.

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OUTPUT DATA RATE AND CONVERSION TIME

MM4113, MM4114, and MM4115 can use the DR[2:0] bits in Config register to select the output data rate from the following : 8, 16, 32, 64, 128, 250, 475, 860 SPS

Table 3. Data rate selection

DR[2:0]	Data Rate
0	8 SPS
1	16 SPS
2	32 SPS
3	64 SPS
4	128 SPS
5	250 SPS
6	475 SPS
7	860 SPS

DIGITAL COMPARATOR (MM4114, MM4115)

MM4114 and MM4115 have a programmable digital comparator that can issue an alert from ALERT/RDY pin. Since ALERT/RDY pin is an open-drain pin, a pull-up resistor is required.

The digital comparator has two modes. In traditional comparator mode, ALERT/RDY pin is asserted when the converted data exceeds the limit set in the High-side threshold register (Hi_thresh) (default low-active). It is then deasserted when the conversion data falls below the value set in the Lo side threshold register (Lo_thresh). In window comparator mode, ALERT/RDY pin is asserted when the converted data exceeds the Hi_thresh register value or falls below the Lo_thresh register value.

In both modes, the COMP_LAT bit can be used to latch and hold the state after the assertion. This assertion can be cleared by a SMBus alert-response or by reading Conversion register. (Refer to Figure 6 for SMBus alert response signals.) In this situation, the lowest slave address output from MM4114 and MM4115 are prioritized and deasserted.In traditional comparator mode, the SMBus alert status bit indicates a 1 if the converted data exceeds Hi_thresh. In window comparator mode, the SMBus alert status bit indicates a 1 if the converted data exceed the Hi_thresh, and a 0 if the converted data exceed the Lo_thresh.

The comparator can also be configured to activate ALERT/RDY pin only when the thresholds set in the threshold registers (Hi_thresh and Lo_thresh) are continuously exceeded. The COMP_QUE[1:0] bits in Config register can set the number of times the threshold is continuously exceeded to 1, 2, or 4. The COMP_QUE[1:0] bits can also disable the comparator function and make ALERT/RDY pin to Hi-Z. In addition, the COMP_POL bit in Config register can control High- or low-activation of ALERT/RDY pin.

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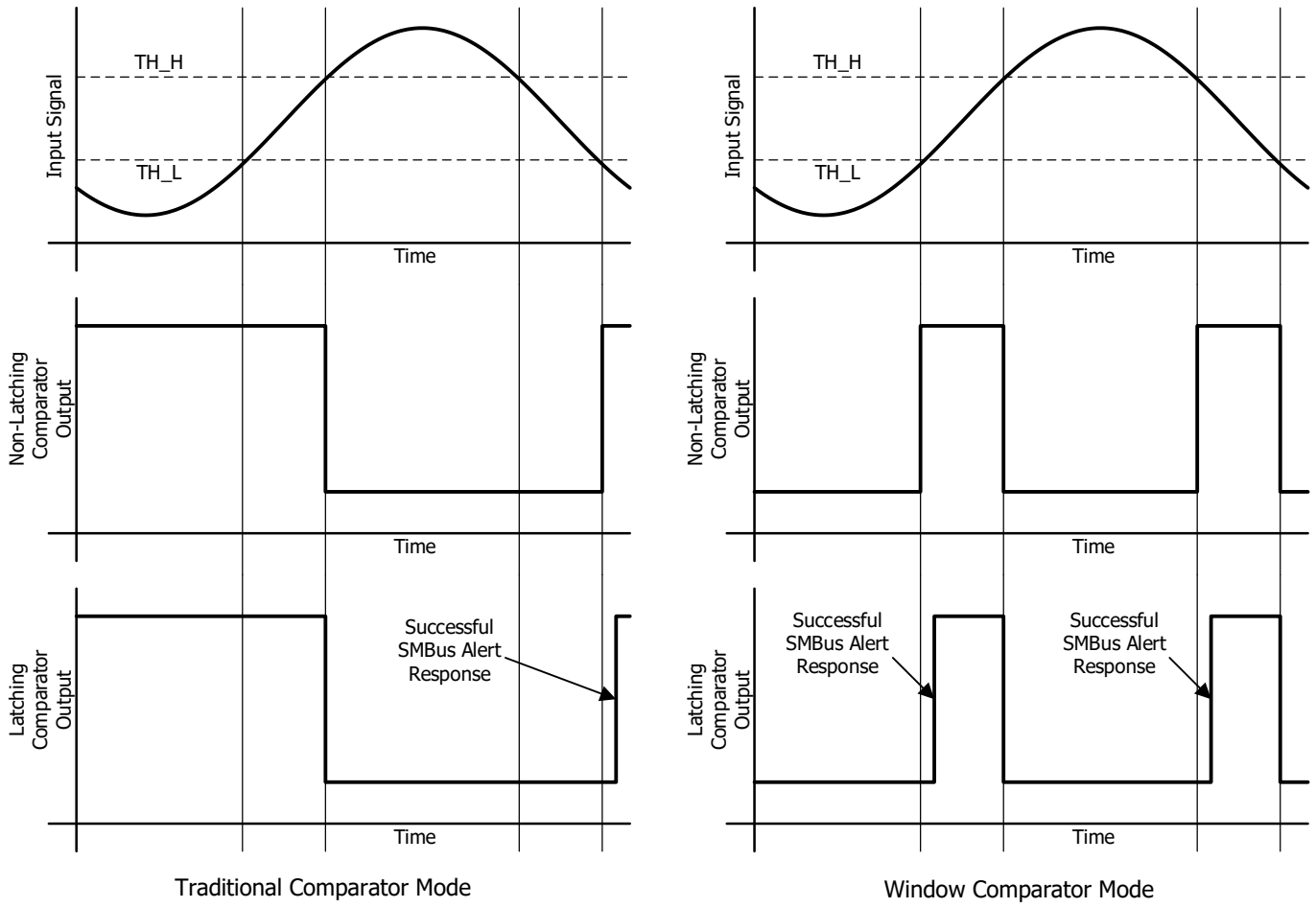

Figure 5. ALERT Pin Timing Diagram

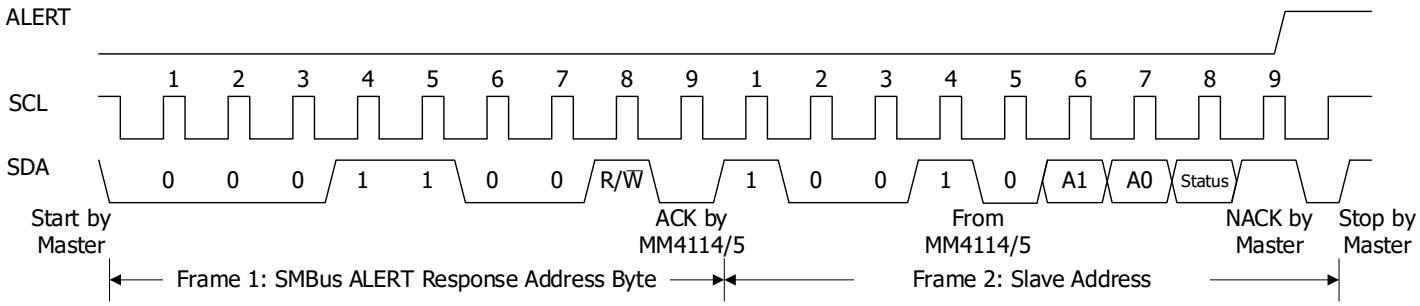

Figure 6. Timing Diagram for SMBus Alert Response

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CONVERSION READY PIN (MM4114, MM4115)

ALERT/RDY pin can also be set as a conversion ready pin. Setting the most significant bit of the Hi_thresh register to 1 and the most significant bit of the Lo_thresh register to 0 enables the conversion ready pin. When the COMP_QUE[1:0] bits are set to any 2-bit value other than 11, the conversion ready signal is output from ALERT/RDY pin. At this time, the functionality of the COMP_MODE and COMP_LAT bits is disabled. When this pin is set as a conversion ready pin, a pull-up resistor must be connected to ALERT/RDY pin as well. As shown in Figure 7, MM4114 and MM4115 output approximately 8 us-conversion ready pulses from ALERT/RDY pin at the completion of conversion in continuous conversion mode.

In single-shot mode, when the COMP_POL bit is set to 0, ALERT/RDY pin is asserted to the low-level on completion of the conversion. The polarity of the COMP_POL bit is still valid for this setting.

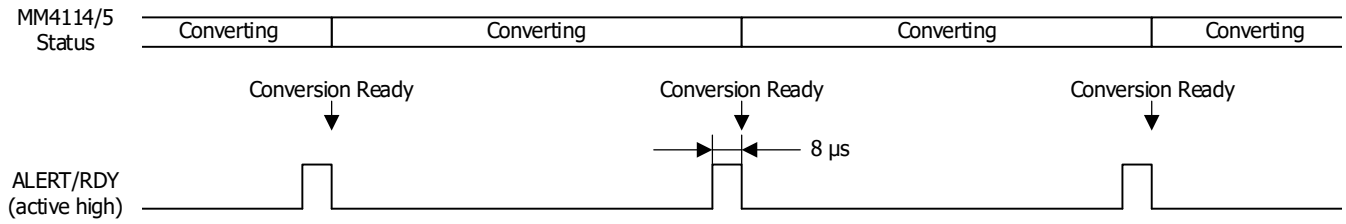

Figure 7. Conversion Ready Pulse in Continuous-Conversion Mode

DEVICE FUNCTION MODES

RESET AND POWER—UP

MM4113, MM4114, and MM4115 initialize at power up and sets all registers to their defaults. This initialization process is completed in about 200 µs, and then automatically goes into the power-down state.

When the I2C general call reset command (06h) is received, the reset processing is executed in the same way as when the device is started.

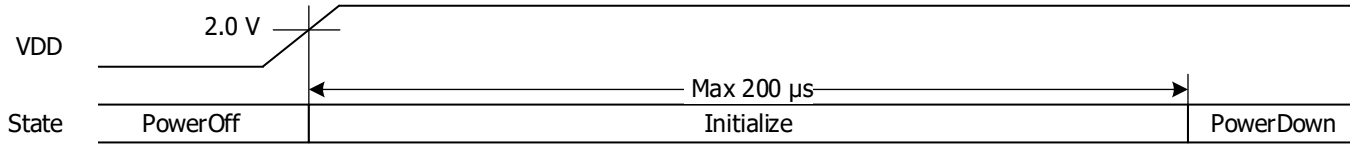

Figure 8. Startup at power on

POWER-OFF AND REBOOT

After power off, MM4113, MM4114, and MM4115 require a wait time of 100us or more for reboot.

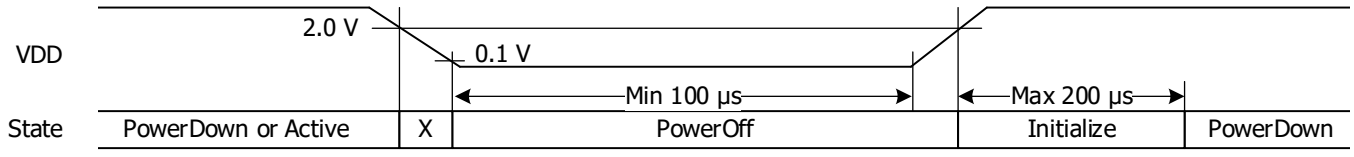

Figure 9. Power off and reboot

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OPERATING MODES

MM4113, MM4114, and MM4115 operate either in continuous-transform mode or single-shot mode. The respective operation mode is selected using the MODE bit of Config register.

SINGLE—SHOT MODE

When MODE bit in Config register is set to 1, MM4113, MM4114, and MM4115 set the single-shot mode and powers down the internal circuit. It remains powered down until 1 is written to Operational Status (OS) bit in Config register. When the OS bit is set to 1, the device starts within approximately 25 us, resets the OS bit to 0, and performs AD conversion once. After the conversion is completed, the conversion result is stored in Conversion register, and the device goes into the power-down state again. If 1 is written to the OS bit during conversion, the new command is disabled and conversion currently being executed continues. To switch to continuous conversion mode, 0 must be written to MODE bit in Config register.

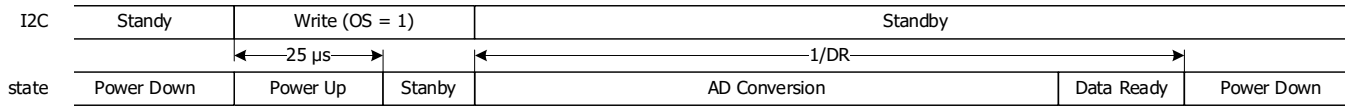

Figure 10. Single-shot conversion

CONTINUOUS-CONVERSION MODE

In continuous conversion mode (MODE bit is set to 0), MM4113, MM4114, and MM4115 perform AD conversion continuously. After the conversion is completed, the result is stored in Conversion register and the next conversion is immediately started. If a new configuration setting is written, the configuration settings of the currently running conversion are retained and the next conversion is performed with the new configuration setting. To switch to single-shot conversion mode, 1 must be written to MODE bit in Config register or reset the device.

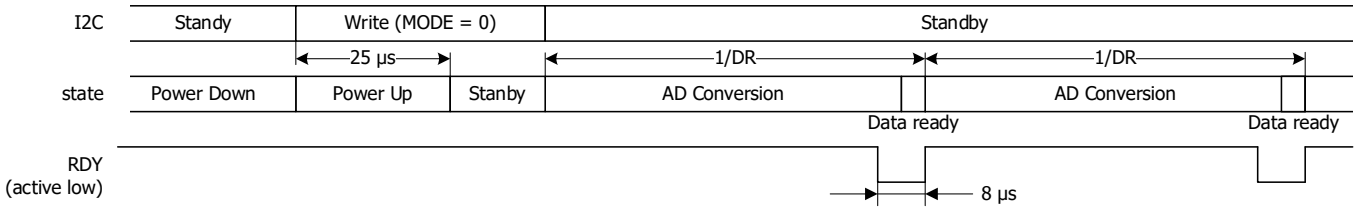

Figure 11. Continuous conversion

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I2C INTERFACE

MM4113, MM4114, and MM4115 communicate as slaves on the I2C interfaces. For speed mode, this IC supports standard mode (100 kHz), fast mode (400 kHz), and high speed mode (3.4 MHz). It also supports the I2C bus timeout function, which releases the bus when the bus communication becomes idle (SCL is low) for longer than 25 ms.

Figure 12 and 13 show the read/write sequence in normal mode and fast mode. In the read sequence, the internal register can be read by writing the pointer address and then reading it again. In the write sequence, data can be written after the pointer address is written. Figure 14 shows the sequences in high-speed mode.

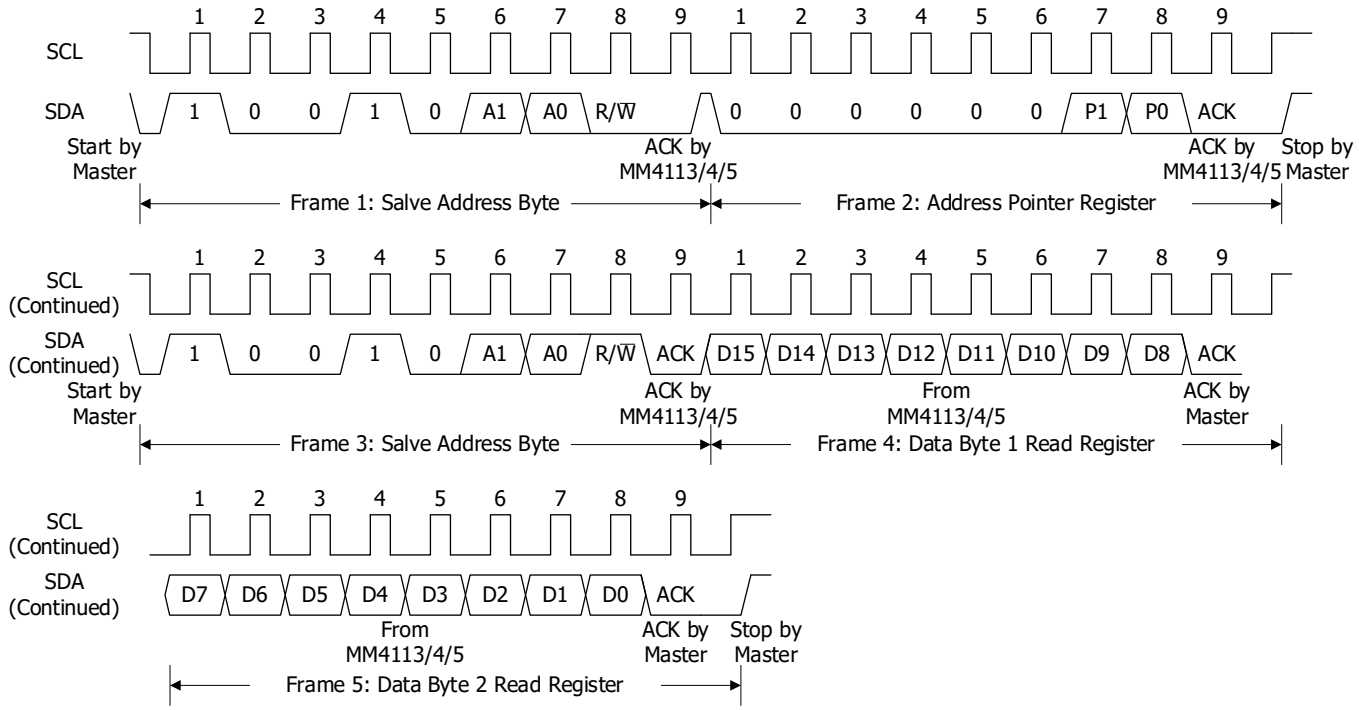

Figure 12. Timing Diagram for Reading from MM4113, MM4114, MM4115

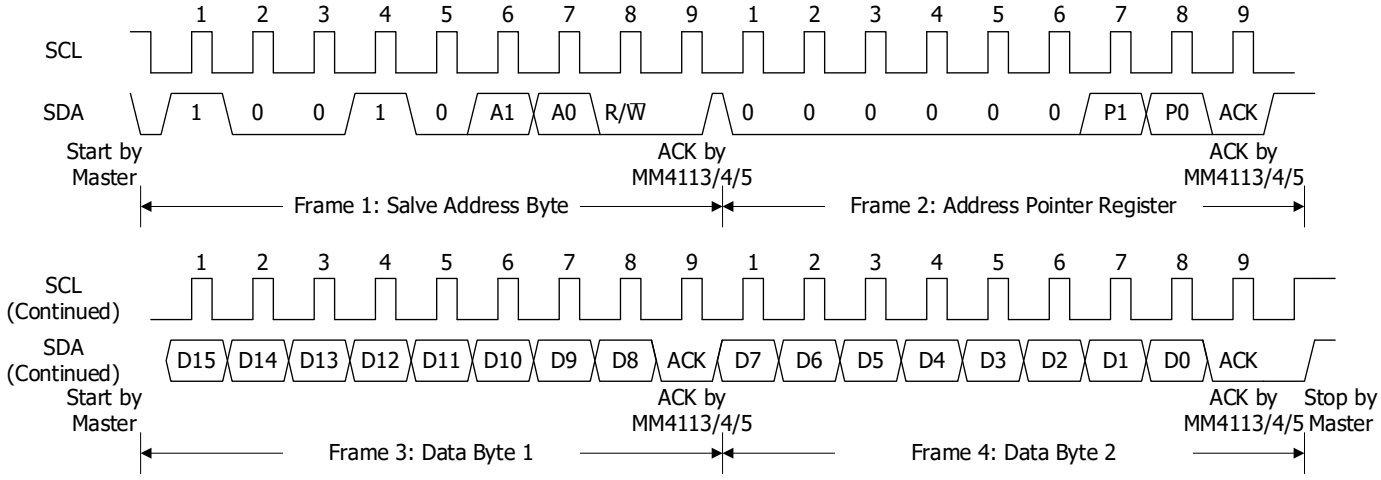

Figure 13. Timing Diagram for Writing to MM4113, MM4114, MM4115

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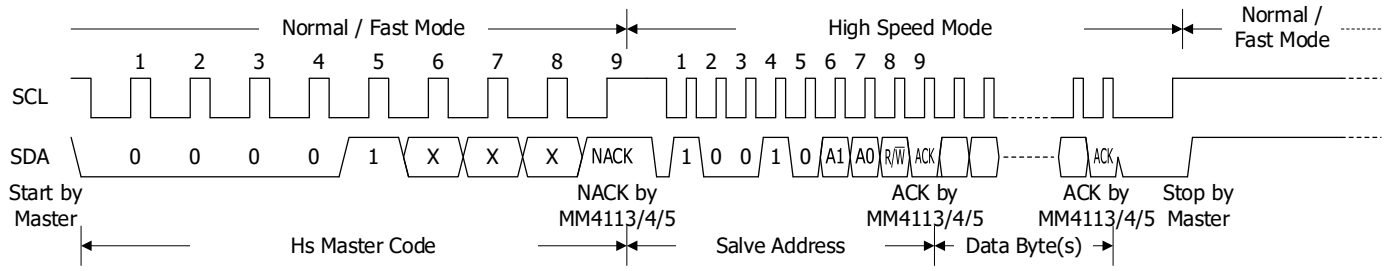

Figure 14. Hs master code

I2C ADDRESS SELECTION

In MM4113, MM4114, and MM4115, ADDR pin is used to set the I2C address of the device. This pin can be connected to GND, VDD, SDA or SCL. As shown in Table 4, four distinct slave addresses can be selected for one pin.

Table 4. ADDR Pin Connection and Corresponding Slave Address

ADDR PIN CONNECTION	SLAVE ADDRESS
GND	100 1000
VDD	100 1001
SDA	100 1010
SCL	100 1011

I2C GENERAL CALL

MM4113, MM4114, and MM4115 respond to an I2C general call (0000 0000). When the general call address is checked and the second byte is 00000110 (06h), MM4113, MM4114, and MM4115 reset the register and enters the power-down state.

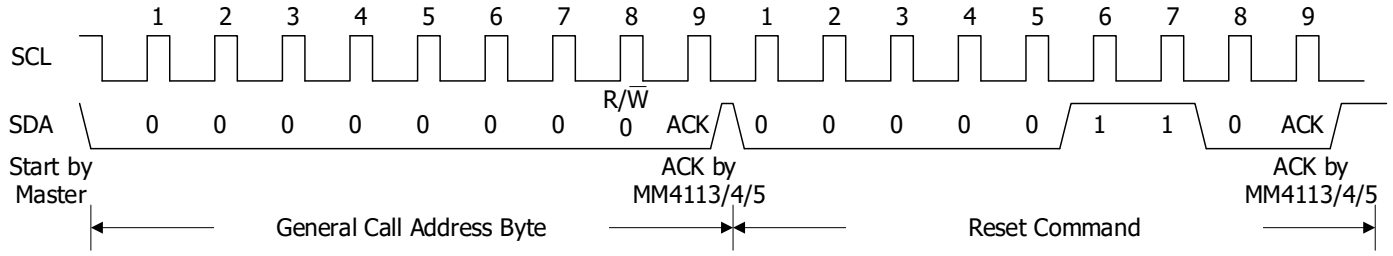

Figure 15. General call reset

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DATA FORMAT

MM4113, MM4114, and MM4115 converted data is 16-bit data in left-aligned 2's complement format. Table 5 shows the ideal output code for differential inputs. Figure 16 shows the code transitions relative to the input voltage.

Table 5. Input Signal versus Ideal Output Code

INPUT SIGNAL $V_{IN} = V(AIN_P)-V(AIN_N)$	IDEAL OUTPUT CODE
≧ +FS $(2^{15}-1)/2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0000h
$-FS/2^{15}$	FFFFh
≦ -FS	8000h

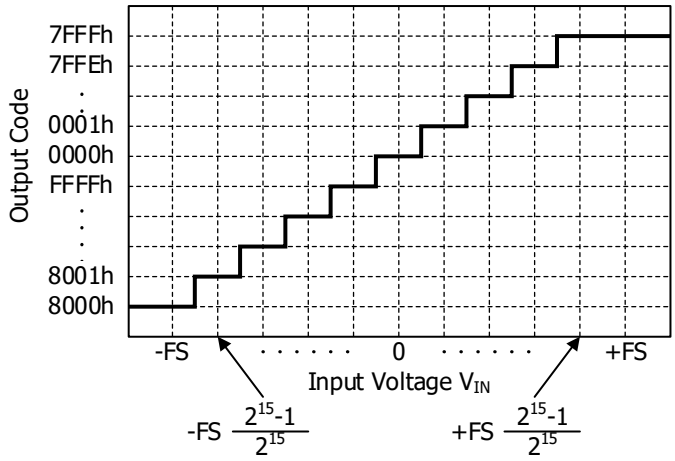

Figure 16. Code Transition Diagram

Only the positive-code range from 0000h to 7FF0h is used to measure single-ended signals. However, if V(AINP) is near 0V, the device may output a negative code because of the offset of the device.

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REGISTER MAP

MM4113, MM4114, and MM4115 have four registers that can be accessed through the I2C interface. Address Pointer register specifies the access destination. Conversion register stores the ADC-converted data. Config register is used to set the operating mode and check the status. The other two registers (Lo_thresh and Hi_thresh) set the threshold used by the comparator function, but not available on MM4113.

Address Pointer Register (address = N/A) [reset = N/A]

All four registers are accessible by writing to the Address Pointer register. See Table 6.

Table 6. Address Pointer Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	P[1:0]	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 7. Address Pointer Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	W	0h	Always write 0h
1:0	P[1:0]	W	0h	Address pointer Register 00 : Conversion Register 01 : Config Register 10 : Lo_thresh Register 11 : Hi_thresh Register

Conversion Register (P[1:0] = 0h) [reset = 0000h]

Conversion register is the two's complement form of the last conversion result. At power-up and reset, Conversion register is cleared to 0 and remains 0 until the first conversion is completed.

Table 8. Conversion Register

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
R-00h							
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
R-00h							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 9. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	D[15:0]	R	0000h	16-bit conversion result

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Config Register (P[1:0] = 1h) [reset = 8583h]

Config register is used to control the operation mode, input selection, data rate, full scale range, and comparator mode.

Table 10. Config Register

15	14	13	12	11	10	9	8
OS	MUX[2:0]			PGA[2:0]			MODE
R/W-1h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			COMP_MODE	COMP_POL	COMP_LAT	COMP_QUE[1:0]	
R/W-4h			R/W-0h	R/W-0h	R/W-0h	R/W-3h	

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 11. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OS	R/W	1h	This bit determines ADC operation status and starts single-shot conversion. When writing: 0 : No effect 1 : Start a single conversion (during power-down state) When reading : 0 : Conversion is in progress. 1 : Conversion is completed.
14:12	MUX[2:0]	R/W	0h	These bits configure the input multiplexer. (MM4115) These bits does not work with MM4113 and MM4114. 000 : AIN_P = AIN0 and AIN_N = AIN1 (default) 001 : AIN_P = AIN0 and AIN_N = AIN3 010 : AIN_P = AIN1 and AIN_N = AIN3 011 : AIN_P = AIN2 and AIN_N = AIN3 100 : AIN_P = AIN0 and AIN_N = GND 101 : AIN_P = AIN1 and AIN_N = GND 110 : AIN_P = AIN2 and AIN_N = GND 111 : AIN_P = AIN3 and AIN_N = GND
11:9	PGA[2:0]	R/W	2h	These bits set gain amplifier. (MM4114, MM4115) These bits does not work with MM4113. 000 : FSR = ±6.144 V (note[1]) 001 : FSR = ±4.096 V (note[1]) 010 : FSR = ±2.048 V (default) 011 : FSR = ±1.024 V 100 : FSR = ±0.512 V 101 : FSR = ±0.256 V 110 : FSR = ±0.256 V 111 : FSR = ±0.256 V

note[1] : This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to the analog input of the device.

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Bit	Field	Type	Reset	Description
8	MODE	R/W	1h	This bit sets ADC operating mode. 0 : Continuous-conversion mode 1 : Single-shot mode or power-down state (default)
7:5	DR[2:0]	R/W	4h	These bits set conversion data rate. 000 : 8 SPS 001 : 16 SPS 010 : 32 SPS 011 : 64 SPS 100 : 128 SPS (default) 101 : 250 SPS 110 : 475 SPS 111 : 860 SPS
4	COMP_MODE	R/W	0h	This bit sets the comparator mode. (MM4114, MM4115) This bit does not work with MM4113. 0 : Traditional comparator (default) 1 : Window comparator
3	COMP_POL	R/W	0h	This bit sets the polarity of the ALERT/RDY pin. (MM4114, MM4115) This bit does not work with MM4113. 0 : Active low (default) 1 : Active high
2	COMP_LAT	R/W	0h	This bit sets whether the ALERT/RDY pin latches. (MM4114, MM4115) This bit does not work with MM4113. 0 : Non-latching comparator (default). 1 : Latching comparator
1:0	COMP_QUE[1:0]	R/W	3h	These bits specify comparator judgment count and comparator usage. (MM4114, MM4115) These bits does not work with MM4113. 00 : Assert after one conversion 01 : Assert after two conversions 10 : Assert after four conversions 11 : Disable comparator and set ALERT/RDY pin to high-impedance (default)

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Lo_thresh (P[1:0] = 2h)[reset = 8000h] and Hi_thresh (P[1:0] = 3h)[reset = 7FFFh] Register

Lo_thresh and Hi_thresh resistors are used to store the comparator upper and lower limits of the thresholds. The output of this comparator is determined by comparing the ADC conversion result with the value of this register. For this reason, the register value of Hi_thresh must always be greater than that of Lo_thresh.

To use the conversion ready function, the MSB of Hi_thresh must be set to 1 and the MSB of Lo_thresh to 0. ALERT/RDY pin outputs the OS bit in single-shot mode and Conversion Ready pulses in continuous-conversion mode.

Table 12. Lo_thresh Register

15	14	13	12	11	10	9	8
Lo_thresh15	Lo_thresh14	Lo_thresh13	Lo_thresh12	Lo_thresh11	Lo_thresh10	Lo_thresh9	Lo_thresh8
R/W-80h							
7	6	5	4	3	2	1	0
Lo_thresh7	Lo_thresh6	Lo_thresh5	Lo_thresh4	Lo_thresh3	Lo_thresh2	Lo_thresh1	Lo_thresh0
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 13. Hi_thresh Register

15	14	13	12	11	10	9	8
Hi_thresh15	Hi_thresh14	Hi_thresh13	Hi_thresh12	Hi_thresh11	Hi_thresh10	Hi_thresh9	Hi_thresh8
R/W-7Fh							
7	6	5	4	3	2	1	0
Hi_thresh7	Hi_thresh6	Hi_thresh5	Hi_thresh4	Hi_thresh3	Hi_thresh2	Hi_thresh1	Hi_thresh0
R/W-FFh							

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 14. Lo_thresh and Hi_thresh Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Lo_thresh [15:0]	R/W	8000h	Low threshold value
15:0	Hi_thresh [15:0]	R/W	7FFFh	High threshold value

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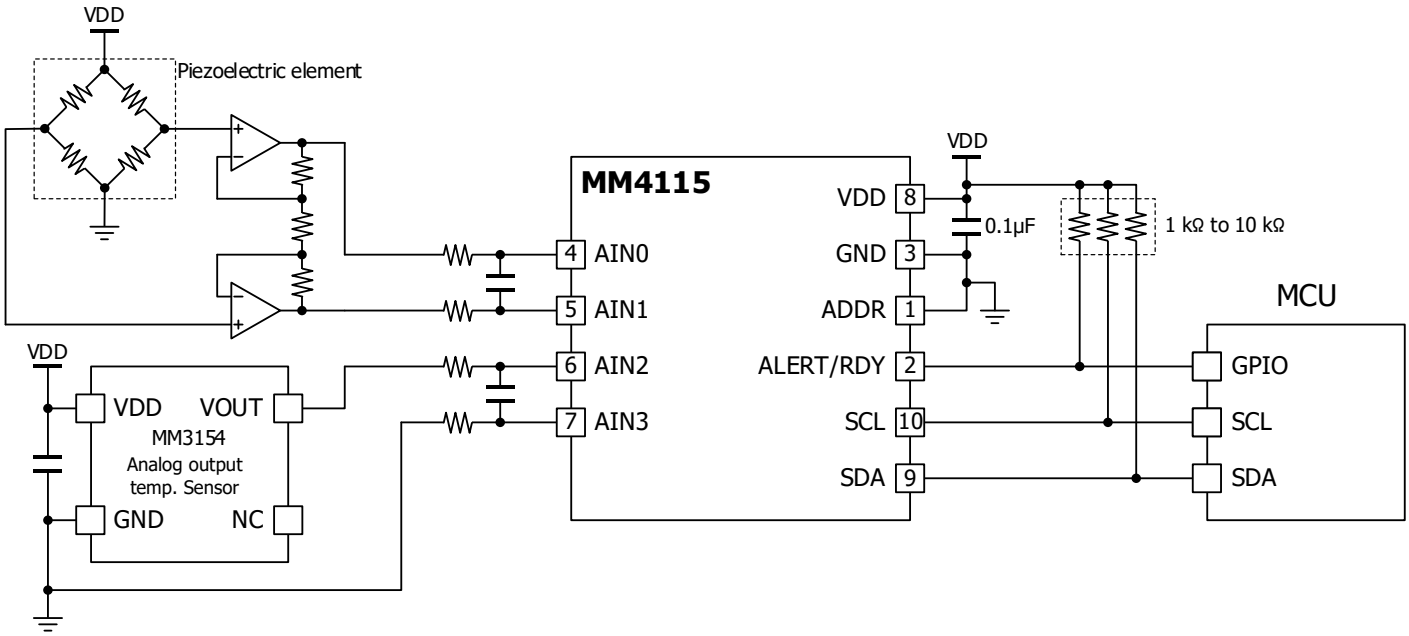
TYPICAL APPLICATION CIRCUIT



APPLICATION HINTS

Transient current flows through MM4113/14/15 during conversion. Connecting a 0.1 µF power supply bypass capacitor absorbs instantaneous current changes and improves tolerance to fluctuations in power supply voltage and noise generation.

Connection of the analog input must be done with sufficiently small output impedance compared to input impedance of the data rate to use. In addition, connecting a low-pass filter to the input reduces the effects of folding distortion and external noise. It is recommended that these constants be checked on the actual machine.

The I2C bus pins of SDA and SCL to VDD must be connected using a pull-up resistor of 1 to 10 kΩ. The resistance value of the resistor to connect must be selected considering the wiring capacitance and data rate of the I2C bus.

Analogue inputs of MM4113/14/15 have protective diodes. However, the current processing capacity of these diodes is limited and applying an analog input voltage to the power rail for extended periods of time in excess of approximately 300 mV may cause permanent damages.

Unused analog input pins must be unconnected or connected to VDD, GND, or intermediate potential.
When ALERT/RDY output pin is not used, it must be unconnected or connected to VDD using a pull-up resistor.

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified

Ta = 25 °C, VDD = 3.3 V, FSR = ±2.048 V, DR = 8 SPS

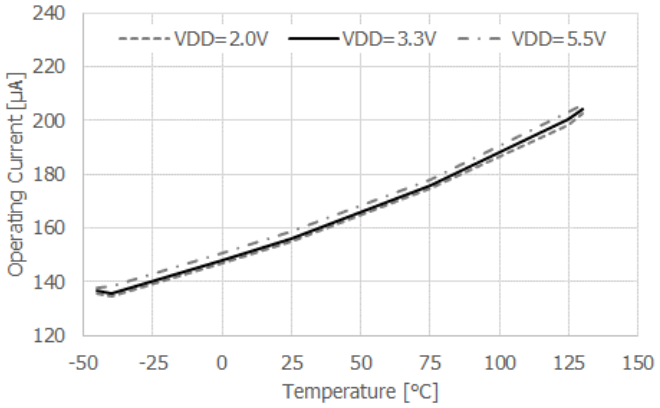

Figure 17. Operating Current vs Temperature

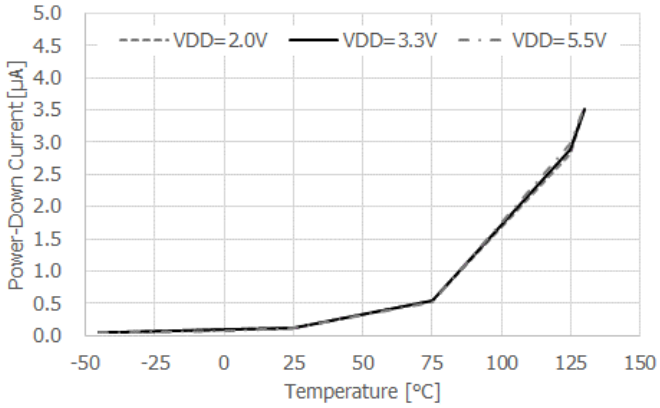

Figure 20. Power-Down Current vs Temperature

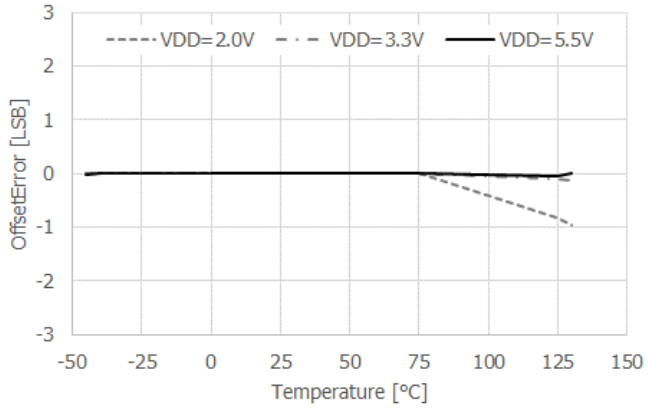

Figure 18. OffsetError vs Temperature

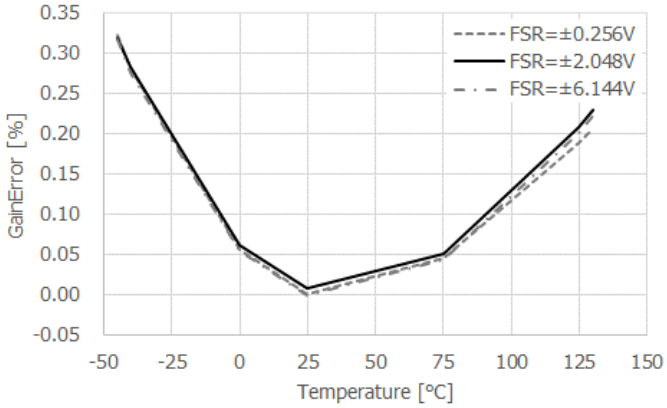

Figure 21. GainError vs Temperature

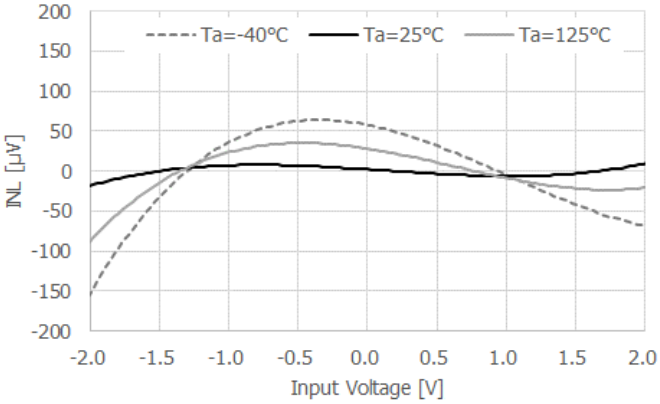

Figure 19. INL vs Input Voltage

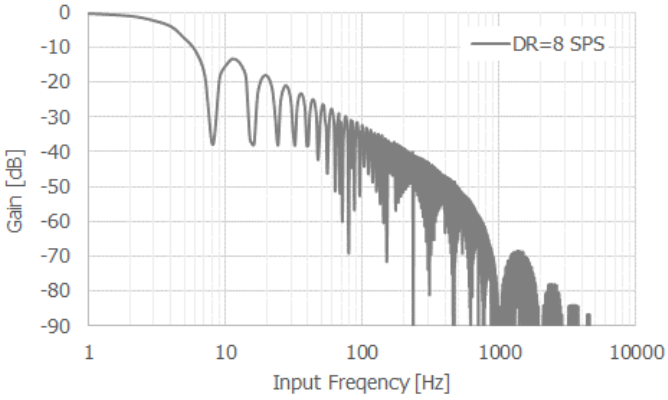

Figure 22. Full Power Band Width

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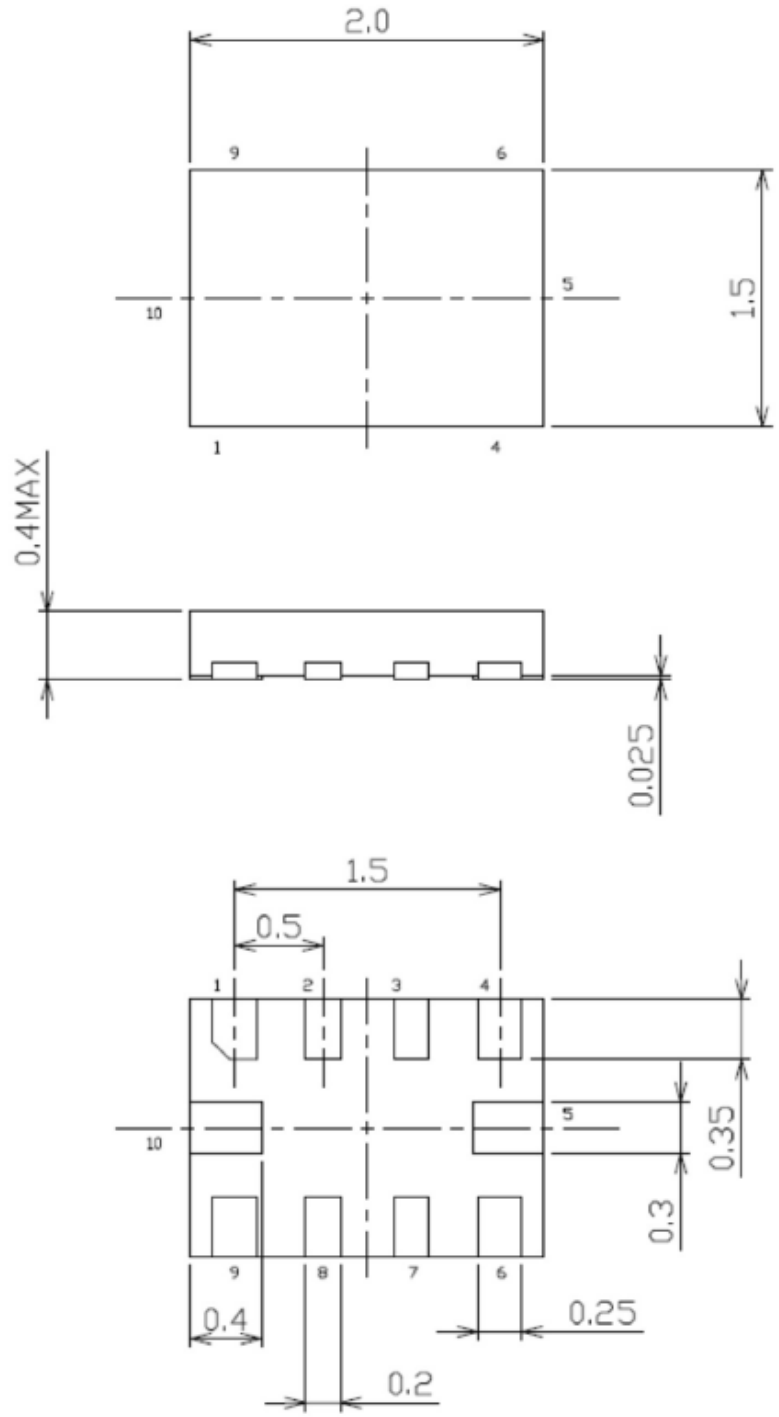
DIMENSIONS

パッケージ: SQFN-10
PACKAGE

UNIT	mm



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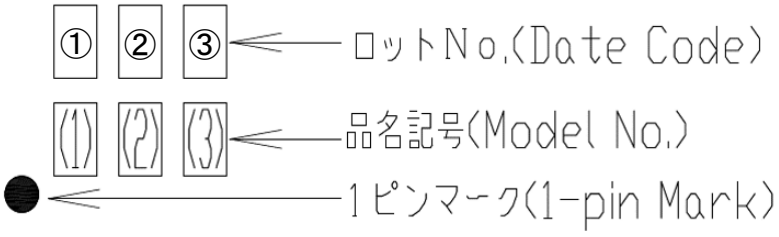
MARKING CONTENTS



Model Name	Model No		
	(1)	(2)	(3)
MM4113A16Rxx	1	1	3
MM4114A16Rxx	1	1	4
MM4115A16Rxx	1	1	5

【生産年の表記方法/How to indicate a production year】

1桁目(①)/The 1st digit (①)	
西暦年末尾 the last digit of a production year	使用表示文字 mark
xxx1	1
xxx2	2
xxx3	3
xxx4	4
xxx5	5
xxx6	6
xxx7	7
xxx8	8
xxx9	9
xxx0	0

2桁目、及び3桁目(②③)/The 2nd and 3rd digit (②③)			
生産週 production week	使用表示文字 mark	生産週 production week	使用表示文字 mark
1	01	27	27
2	02	28	28
3	03	29	29
4	04	30	30
5	05	31	31
6	06	32	32
7	07	33	33
8	08	34	34
9	09	35	35
10	10	36	36
11	11	37	37
12	12	38	38
13	13	39	39
14	14	40	40
15	15	41	41
16	16	42	42
17	17	43	43
18	18	44	44
19	19	45	45
20	20	46	46
21	21	47	47
22	22	48	48
23	23	49	49
24	24	50	50
25	25	51	51
26	26	52	52
		53	53

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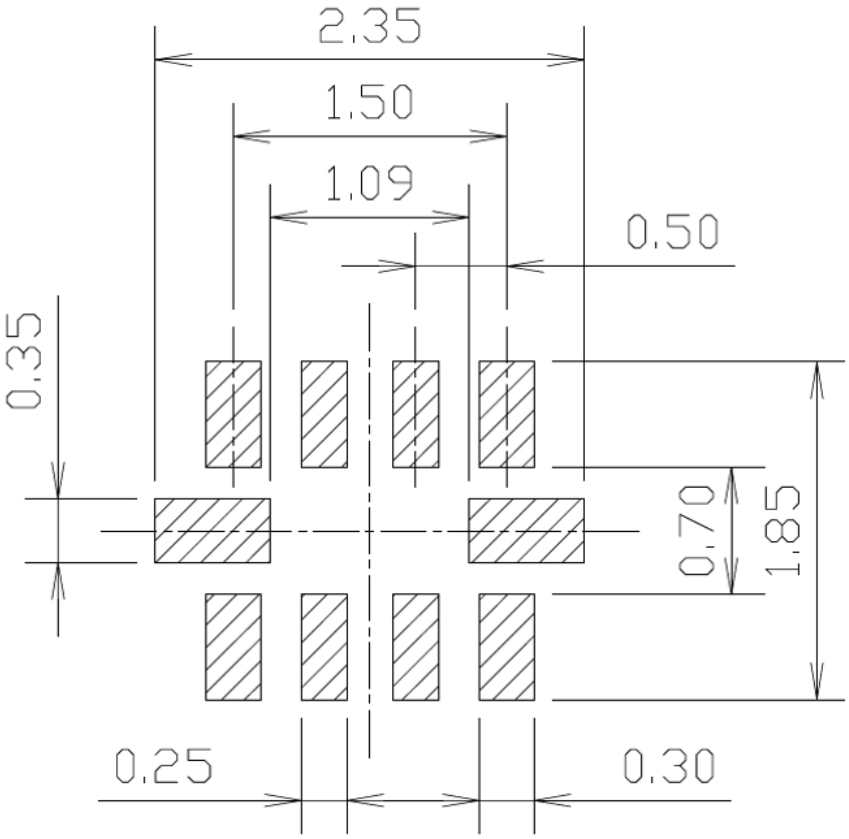
RECOMMENDED LAND PATTERN

UNIT mm



The dimension are for reference only and not guaranteed by design.

To design practically, correction should be made for optimized dimensions considering the effects of the board type to be mounted, mount (soldering) method, type and coating thickness of cream solder.

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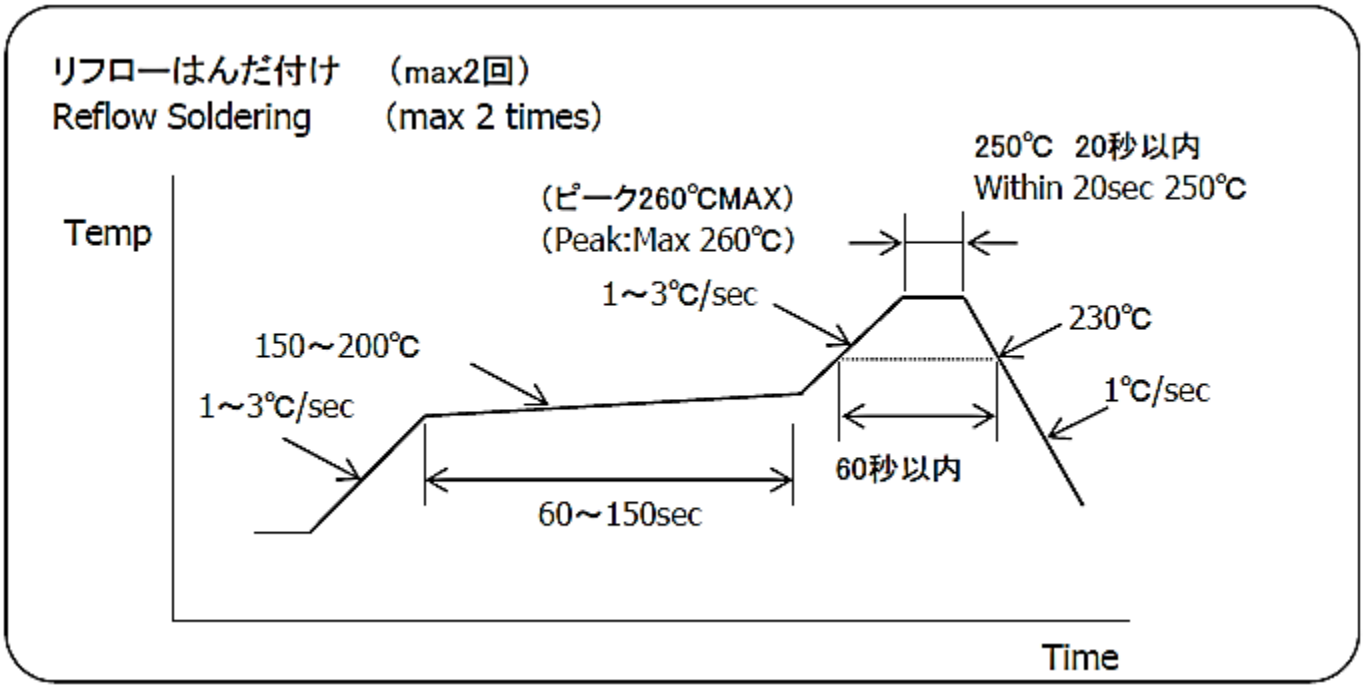
MOUNTING CONDITION FOR PACKAGE

Pb-Free recommended profile condition



This profile gives recommended values, which are not guaranteed.
For mounting the package, evaluate the profile with the equipment, conditions, and materials to be used.

・Mounting by flow solding
Flow soldering cannot be used for mounting of this package.

・Mounting by manual soldering
Manual soldering cannot be used for mounting of this package.

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MOUNTING CONDITION FOR PACKAGE

Storage method

【Storage condition】

Store the device under the following conditions.

Temperature：5 to 30 ℃
Humidity：40 to 70 %RH
Storage life：1 year

For the product in the moisture-proof packaging, follow these conditions after unpacking.

Temperature：5 to 30 ℃
Humidity：40 to 70 %RH
Storage life：168 hours

Do not store this device where a large amount of dust or harmful volatile gas exists, electrostatic is easily charged, condensation is generated, or changes in temperature and humidity are wide, or under the direct sunlight.

【Baking】

If the storage time specified above has passed, mounting by soldering may cause cracks on the moistureabsorbed package. Before mounting, the package should be baked under the following conditions.

Temperature：125 ℃
Storage life：16 to 24 hours

Embossing tapes and reels are not heat-resistant type.
Before baking, the device should be placed in a heat-resistant container.
In consideration of the time-consuming baking process and the possibility of deformed terminal, the device should be mounted promptly within the time observing the storage conditions.
If a long-term storage is needed, a desiccator or a dry box should be used.

【Handling instructions】

Shipping boxes must be handled with care because any drop or shock may damage the device.
Additionally, the device must be handled in the place with the protection against electrostatic charge and without extreme changes of temperature/humidity.

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LINE-UP

Device	Resolution	Data rate	Input channels		PGA	Digital comparator	Interface
			Differencial	Single-End			
MM4113	16Bit	8 ~ 860 SPS	1	1	No	No	MM4113
MM4114	16Bit	8 ~ 860 SPS	1	1	Yes	Yes	MM4114
MM4115	16Bit	8 ~ 860 SPS	2	4	Yes	Yes	MM4115
MM4013	12Bit	128 ~ 3300 SPS	1	1	No	No	MM4013
MM4014	12Bit	128 ~ 3300 SPS	1	1	Yes	Yes	MM4014
MM4015	12Bit	128 ~ 3300 SPS	2	4	Yes	Yes	MM4015

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Strategy Engineering Department Semiconductor Business Division
Tel: +81-46-230-3470 / http://www.mitsumi.co.jp

Notes:
Any products mentioned this datasheet are subject to any modification in their appearance and others for improvements without prior notification. The details listed here are not a guarantee of the individual products at the time of ordering. When using the products, you will be asked to check their specifications.

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