

IC for Regulator+Reset Monolithic IC MM1687 Series

Outline

This IC is a regulator + reset IC developed for optical disc drives such as DVD-ROM drives. The output voltage of the regulator and detection voltage of the reset are fixed, while the output voltage of the reset and detection voltage of the reset are programmable ranging from 1.5V to 5.0V, and 2.7V to 5.0V respectively upon request.

Features

- 1. Output voltage accuracy $\pm 2\%$
- 2. Dropout voltage 0.12V typ. ($I_o=150mA$)
- 3. Large output current 300mA max.
- 4. High ripple rejection 80dB typ.
- 5. Incorporates a thermal shutdown circuit
- 6. Incorporates a current limit circuit
- 7. Reset detection voltage 3.0 to 5.0V
- 8. Delay time from the voltage detection to the reset release can be easily programmed.

Package

SOP-8D

Applications

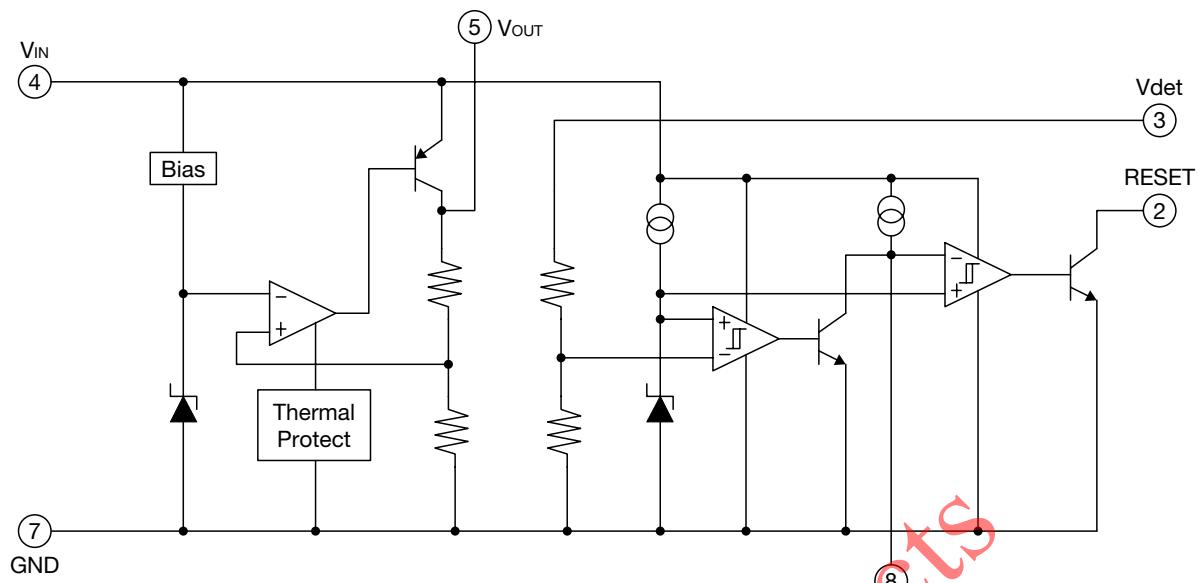
- 1. CD-ROM drive
- 2. Optical disc drivers

Pin Assignment

1	NC
2	Reset
3	Vdet
4	V _{IN}
5	V _{OUT}
6	NC
7	GND
8	Cd

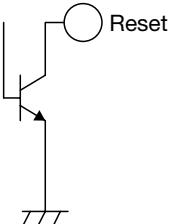
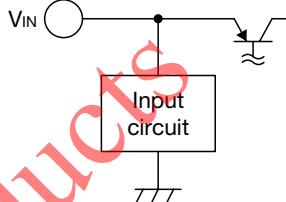
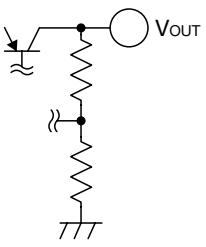
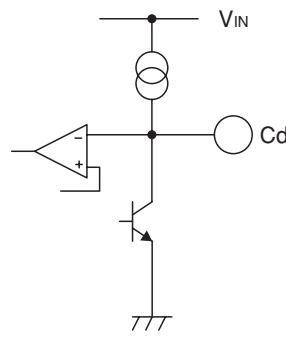
SOP-8D
(TOP VIEW)

Block Diagram



Phased Out Products

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram						
1,6	NC								
2	Reset	Reset-output pin Reset logical table	 <table border="1" style="margin-left: 10px;"> <tr> <td></td> <td>Reset</td> </tr> <tr> <td>Vdet < Vs</td> <td>L</td> </tr> <tr> <td>Vdet > Vs</td> <td>H</td> </tr> </table>		Reset	Vdet < Vs	L	Vdet > Vs	H
	Reset								
Vdet < Vs	L								
Vdet > Vs	H								
3	Vdet	Voltage-supply pin (RESET)							
4	V _{IN}	Input pin The capacitor is required to connect with the input pin more than 1μF.							
5	V _{OUT}	Output pin							
7	GND	Ground							
8	C _d	Delay time capacitor pin The delay time of reset output can be set according to the capacitor value connected with C _d . $t_{PLH} = 450000 \cdot C$ <p>t_{PLH}: Delay time (s) C: capacitance (F)</p>							

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-55~+150	°C
Supply voltage	V _{IN}	-0.3~+10	V
Output current	I _{OUT}	500	mA
Power dissipation	P _d	950 (*1)	mW

Note1: *1 Glass epoxy attached on PC Board (192 × 142 × 1.2mm)

Recommended Operating Conditions (Ta=25°C)

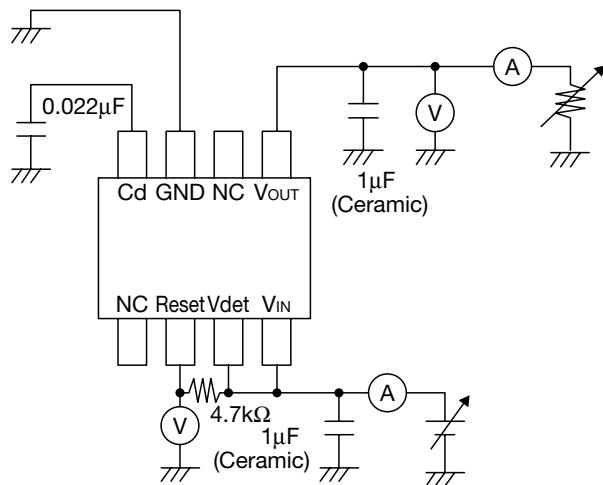
Item	Symbol	Ratings	Units
Operating temperature	T _{OP}	-40~+85	°C
Output current	I _{OUT}	0~400	mA
Operating voltage	V _{OP}	0~+10	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CONT}=1.6V)

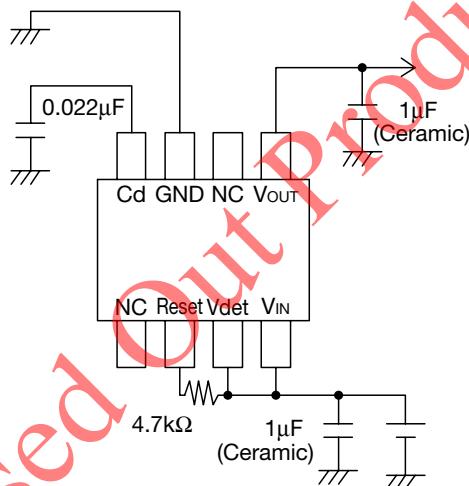
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
No-load Input current 1	I _{CCQ1}	V _{IN} =5V I _{OUT} =0mA		0.6	1.2	mA
V _{DET} pin current	I _{CCQ3}	V _{DET} =5V		20	40	μA
Regulator Block						
Output voltage	V _{OUT}	V _{IN} =5V I _{OUT} =30mA	3.234	3.30	3.366	V
Dropout voltage	V _{IO}	V _{IN} =3.1V I _{OUT} =300mA		0.25	0.50	V
Line regulation	ΔV ₁	V _{IN} =4.5V~5.5V I _{OUT} =30mA		10	20	mV
Load regulation	ΔV ₂	V _{IN} =5V I _{OUT} =0mA~300mA		20	120	mV
V _{OUT} temperature coefficient *1	ΔV _{OUT} /<ΔT	T _J =-40~+85°C V _{IN} =5V I _{OUT} =30mA		100		ppm/°C
Ripple rejection *1	R _R	V _{IN} =5V f=1kHz V _{RIPPLE} =1V I _{OUT} =30mA	50	80		dB
Output noise voltage *1	V _N	V _{IN} =5V f=20~80kHz I _{OUT} =30mA		40	120	μVrms
Reset Block						
Detecting voltage	V _S	V _{IN} =H→L	3.626	3.70	3.774	V
V _S temperature coefficient *1	ΔV _S /<ΔT	T _J =-40~+85°C		100		ppm/°C
Hysteresis voltage	ΔV _S	V _{IN} =H→L→H	100		200	mV
Low level output voltage	V _{OL}	V _{IN} =V _{DET} =3.4V RL=4.7kΩ		100	200	mV
Output leakage current	I _{OH}	V _{IN} =V _{DET} =5V			±0.1	μA
Output current 1	I _{OL1}	V _{IN} =3.6V	5			mA
Output current 2 *1	I _{OL2}	V _{IN} =3.6V Ta=-20~+80°C	4			mA
H transmission delay time	t _{PLH}	Cd=OPEN		30	90	μs
Reset delay time *1	t _{PLH1}	V _{DET} =3.2~4.2V, V _{IN} =5V Cd=0.022μF	5	10	20	ms
L transmission delay time *1	t _{PHL}			30	90	μs
Threshold operating voltage	V _{OPL}	V _{OL} =0.4V		0.65	0.85	V

Note 1: *1 The parameter is guaranteed by design.

Measuring Circuit



Application Circuit

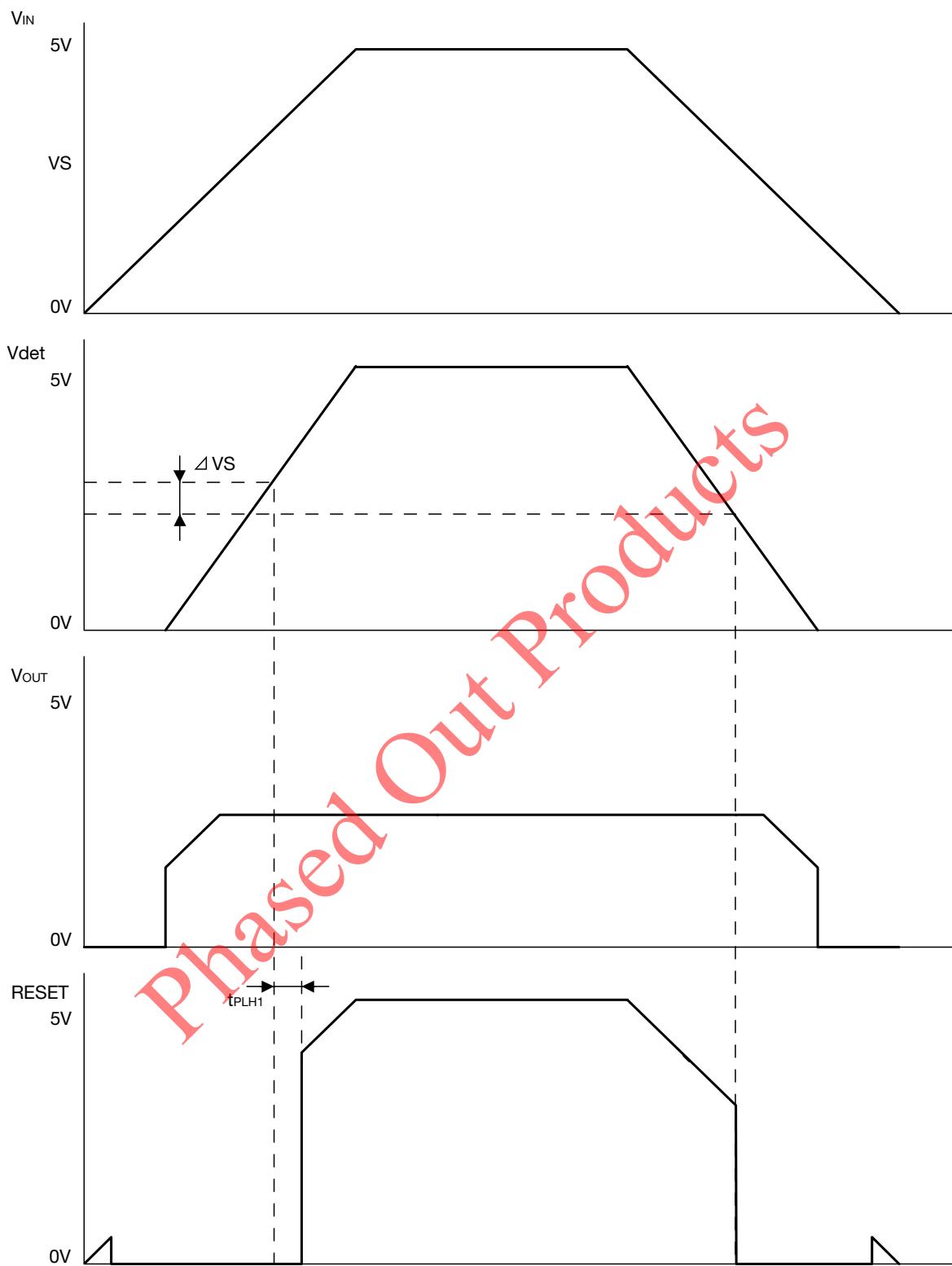


*Temperature Characteristics: B Type

Note

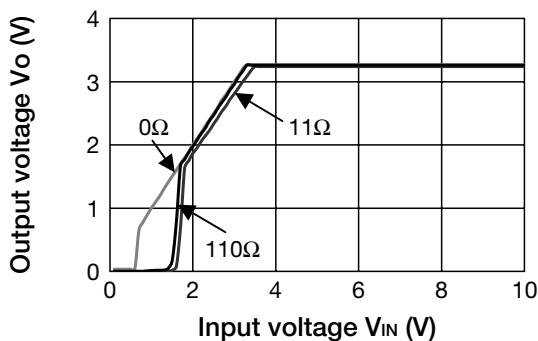
1. The output capacitor is required between output and GND to prevent the oscillation.
2. The ESR of capacitor must be defined in ESR stability area.
It is possible to use a ceramic capacitor without ESR resistance for output.
The ceramic capacitor must be used more than 1μF and B type temperature characteristics.
3. The wire of Vcc and GND is required to print full ground plane for noise and stability.
4. The input capacitor must be connected in 1cm from the input pin.
5. In case the output voltage is above the input voltage, the overcurrent flow by internal parasitic diode from output to input. In such application, the external bypass diode must be connected between output and input pin.

Timing Chart

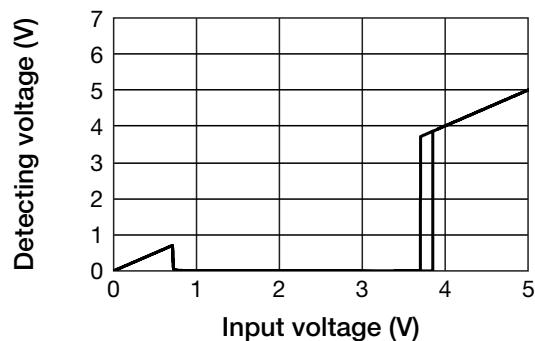


Characteristics (Except where noted otherwise, Ta=25°C, V_{IN}=5V, C_{IN}=1μF, C_O=1μF, C_D=0.022μF)

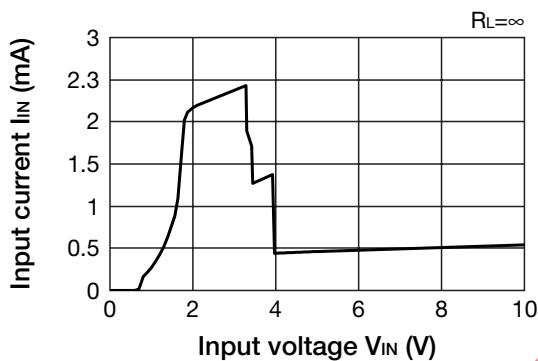
■ Output Voltage-Input Voltage



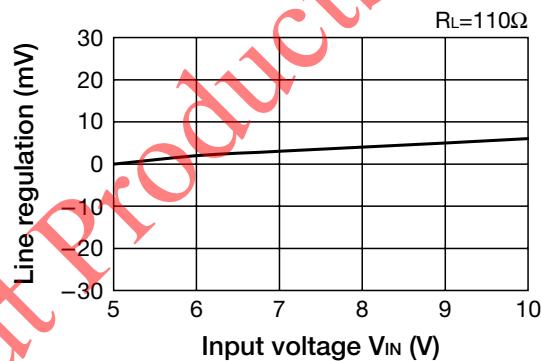
■ Detecting Voltage



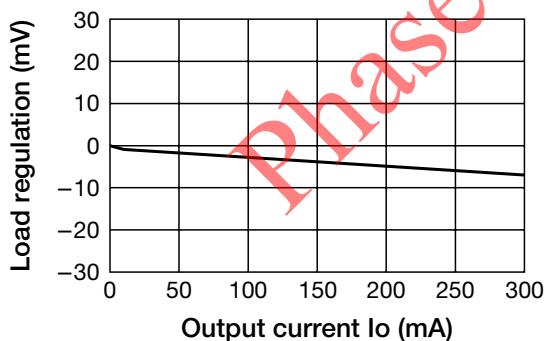
■ Input current-Input Voltage



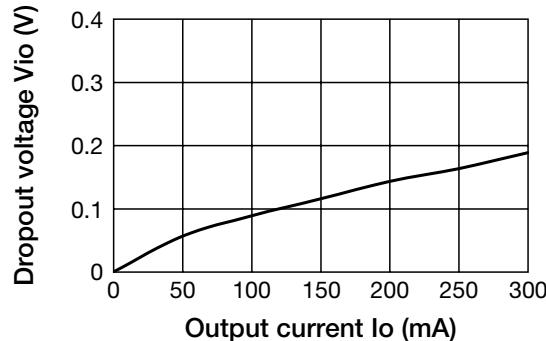
■ Line Regulation V_o



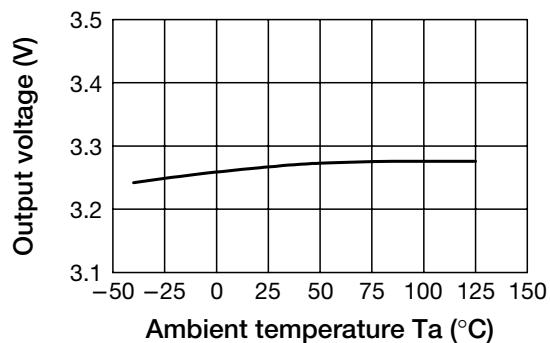
■ Load Regulation V_o



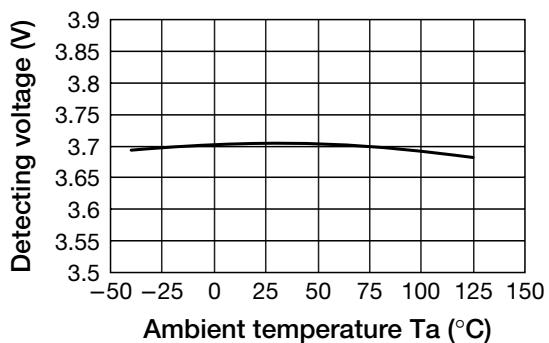
■ Dropout Voltage V_o -Output Current



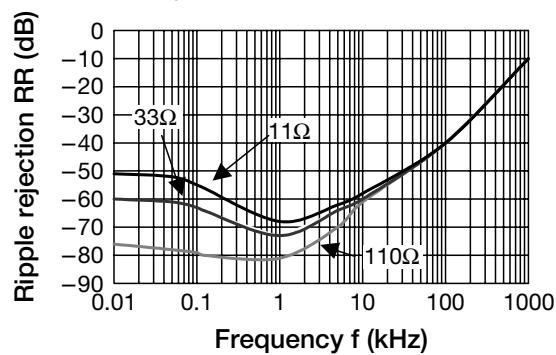
■ Output Voltage-Ambient Temperature



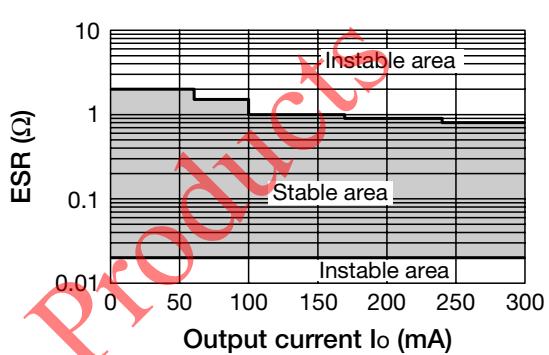
■ Detecting Voltage-Ambient Temperature



■ Ripple Rejection



■ ESR Stable Area



■ Load transient response ($I_o=0 \rightarrow 300\text{mA}$)

