

IC for System Reset Monolithic IC PST600

September 6, 2001

Outline

This IC functions in a variety of CPU systems and other logic systems, to detect supply voltage and reset the system accurately when the power is turned on or interrupted. There are other system reset ICs available such as PST572(conventional). In PST600, the circuit current increases or decreases during power-on tracking a load current. This is a low-reset type system reset IC with low-current consumption during power-on and power-off.

Features

1. Low current consumption during power-on and power-off as the circuit current increases or decreases during power-on tracking a load current
No load : $I_{CCL}=7\mu A$ typ.; $I_{CCH}=5\mu A$ typ.
2. Low operating limit voltage
0.65V typ.
3. Hysteresis voltage provided for detection voltage
50mV typ.
4. 10 ranks of detection voltages are available.

PST600	C : 4.5V typ.	H : 3.1V typ.
	D : 4.2V typ.	I : 2.9V typ.
	E : 3.9V typ.	J : 2.7V typ.
	F : 3.6V typ.	K : 2.5V typ.
	G : 3.3V typ.	L : 2.3V typ.

Packages

MMP-3A (PST600□M)

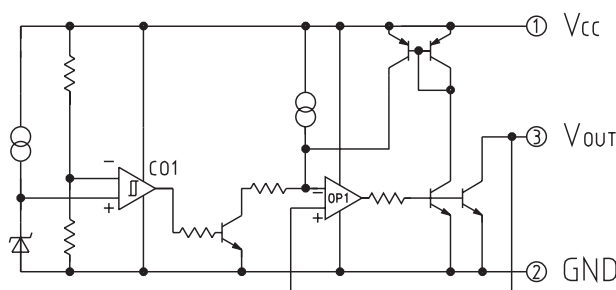
TO-92A (PST600□)

*The box represents a rank of detection voltage.

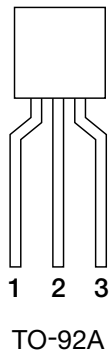
Applications

1. Reset circuits for microcomputers, CPUs and MPUs
2. Reset circuits for logic circuits
3. Battery voltage check circuits
4. Back-up power supply switching circuits
5. Level detection circuits

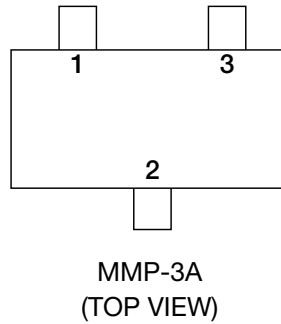
Equivalent Circuit



Pin Assignment



1	V _{CC}
2	GND
3	V _{OUT}



1	V _{CC}
2	GND
3	V _{OUT}

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	-0.3~10	V
Allowable loss	P _d	200 (MMP-3A) 300 (TO-92A)	mW

Electrical Characteristics (Ta=25°C) (unless otherwise indicated resistance unit is Ω)

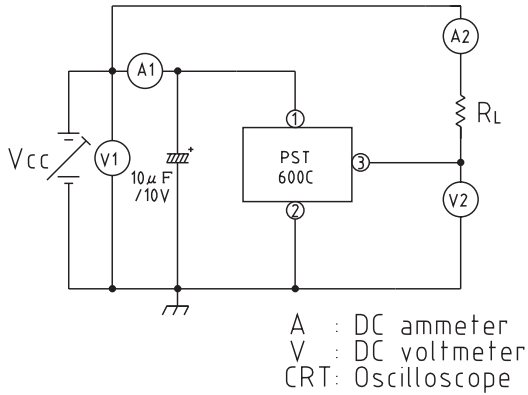
Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units	
Detection voltage	V _s	1	R _L =470 V _{OL} ≤ 0.4V V _{CC} =H→L	PST600C	4.3	4.5	4.7	V
				PST600D	4.0	4.2	4.4	
				PST600E	3.7	3.9	4.1	
				PST600F	3.4	3.6	3.8	
				PST600G	3.1	3.3	3.5	
				PST600H	2.9	3.1	3.3	
				PST600I	2.75	2.90	3.05	
				PST600J	2.55	2.70	2.85	
				PST600K	2.35	2.50	2.65	
				PST600L	2.15	2.30	2.45	
Hysteresis voltage	ΔV _s	1	R _L =470, V _{CC} =L→H→L	30	50	100	mV	
Detection voltage temperature coefficient	V _s /ΔT	1	R _L =470, Ta=-20°C~+75°C		±0.01		%/°C	
Low level output voltage	V _{OL}	1	V _{CC} =V _s min. -0.05V, R _L =470		0.3	0.4	V	
Output leak current	I _{OH}	1	V _{CC} =10V			±0.1	μA	
Circuit current for ON	I _{CC} L	1	V _{CC} =V _s min. -0.05V	I _{OL} =0mA		7	14	μA
				I _{OL} =8mA		50	130	
Circuit current for OFF	I _{CC} H	1	V _{CC} =V _s typ./0.85V, R _L =∞		5	10	μA	
H transmission delay time	t _{PLH}	2	R _L =4.7k, C _L =100pF *1	20	40	80	μs	
L transmission delay time	t _{PHL}	2	R _L =4.7k, C _L =100pF *1	10	20	40	μs	
Operating limit voltage	V _{op} L	1	R _L =4.7k, V _{OL} ≤ 0.4V		0.65	0.85	V	
Output current 1 for ON	I _{OL} 1	1	V _{CC} =V _s min. -0.05V, R _L =0	8			mA	
Output current 2 for ON	I _{OL} 2	1	Ta=-20°C~+75°C, R _L =0 *2	6			mA	

*1 t_{PLH} : V_{CC}= (V_s typ. -0.4V) → (V_s typ.+0.4V), t_{PHL} : V_{CC}= (V_s typ.+0.4V) → (V_s typ.-0.4V)

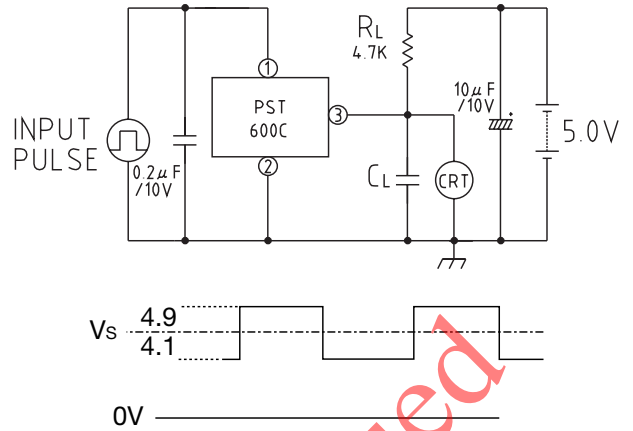
*2 V_{CC}=V_s min. -0.15V

Measurement Circuit

[1]



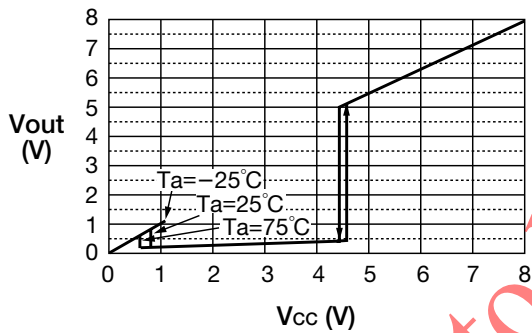
[2]



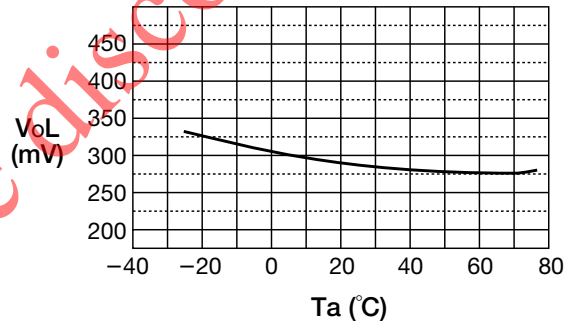
* The input model is an example of PST600C (MMP-3P).

Characteristics (PST600C is used as the representative model for characteristics examples.)

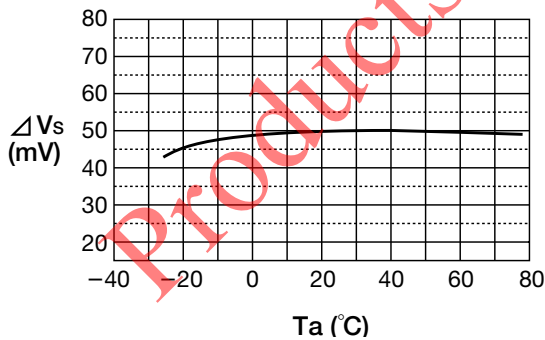
■ Vcc vs. Vout



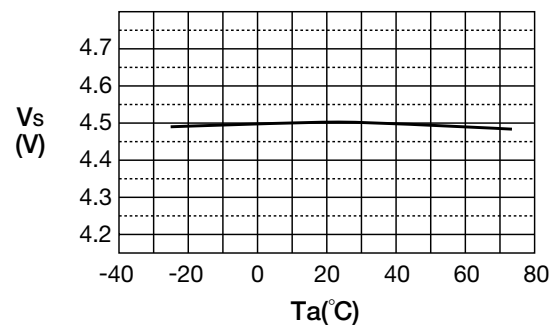
■ VoL vs. Ta



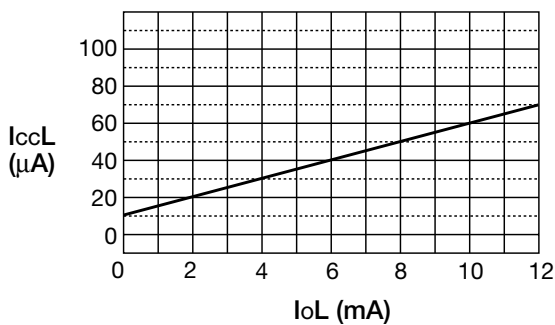
■ ΔVs vs. Ta



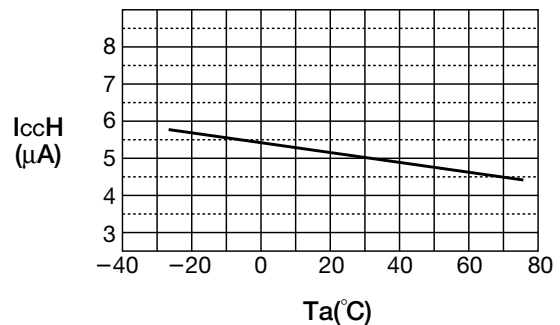
■ Vs vs. Ta



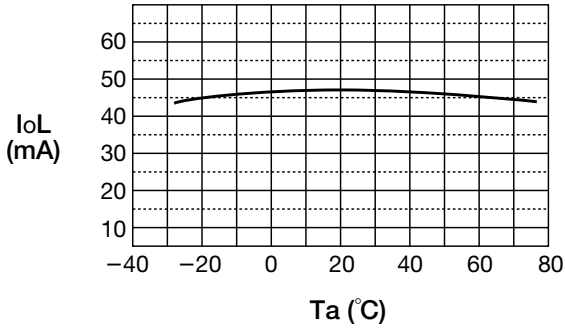
■ IccL vs. IoL



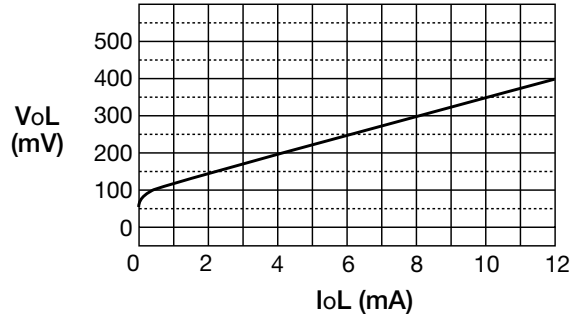
■ IccH vs. Ta



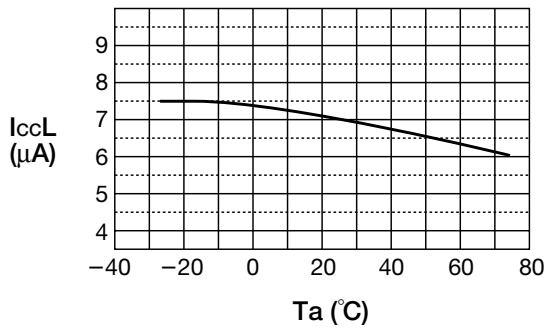
IoL vs. Ta



VoL vs. IoL

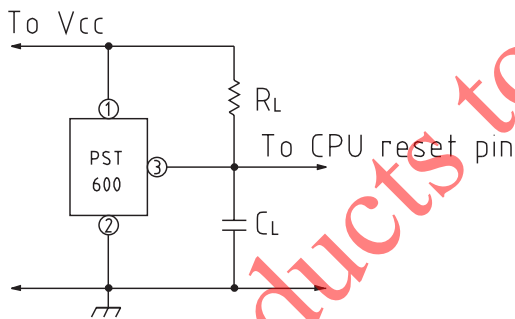


IccL (IoL=0mA) vs. Ta



Application Circuits

1. Normal hard reset



Delay Time (tPLH)

$$\approx C_L \times R_L \times \left[\ln \frac{V_{CC}}{V_{CC} - (V_{S\ CPU} + 0.2)} \right] + 0.040 \text{ (ms)}$$

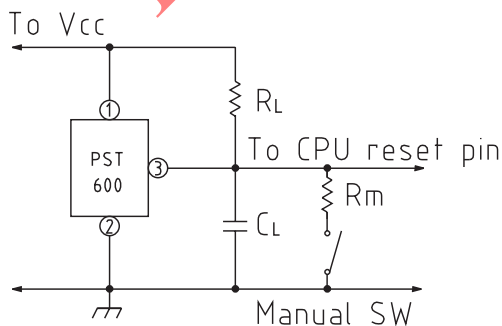
CL : µF Vs CPU : CPU, MPU reset threshold voltage

RL : kΩ

Voltage : V

Note : When VCC line impedance is high, connect a capacitor between IC Pins 1 and 2.

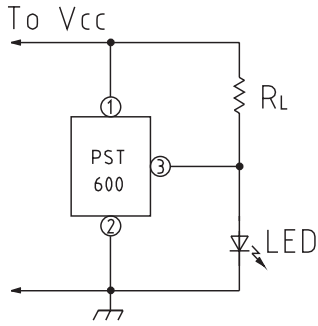
2. Manual Reset



Note : Prevent Manual SW chattering by using RL, CL and Rm. Rm setting conditions are as follows : Rm ≤ 1/20 RL

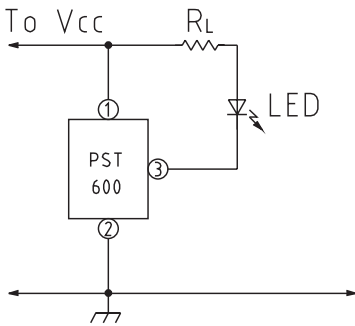
Note : When VCC line impedance is high, connect a capacitor between IC Pins 1 and 2.

3. Battery Checker (LED ON for High voltage)



Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.

4. Battery Checker (LED ON for Low voltage)



Note : When V_{CC} line impedance is high, connect a capacitor between IC Pins 1 and 2.

Products to be discontinued