High voltage Reset IC with separated sense pin and Release/Detect delay time

PST114/PST11D Series

Overview

This IC is a 40V withstand voltage 1ch voltage detection IC that is ideal for monitoring the voltage of car batteries. The voltage detection accuracy is ± 2% including temperature fluctuation, and the output form is Nch open drain output.The Current consumption is 1.7 μA (typ.) And the operating temperature range is -40 to 105 ° C.
The detection delay time and release delay time can be set with external capacitors.

Features

- High withstand voltage
- High accuracy detection
- Low current consumption
- Hysteresis voltage selectable (0.1V to 4.0V)
- Separated sense pin
- Release/Detect delay time

Main specifications

Absolute maximum rating	:	-0.3V to 40V
Operating voltage	:	2.7V to 20V
Operating ambient temperature	:	-40℃ to 105℃
Detection voltage	:	5.0V to 10.0V (0.1V step)
Detection voltage accuracy	:	±2% (Ta=-40 to 105℃)
Hysteresis voltage	:	0.1V to 4.0V
Consumption current	:	PST114: Typ. 1.7uA (VDD=3.3V, VS=16V) PST11D: Typ. 2.3uA (VDD=3.3V, VS=16V)
Output type	:	Open drain
Output Logic	:	PST114: Active L PST11D: Active H
Detect delay time	:	Typ. 10ms (VDD=3.3V, VS=13V⇒0V, CDL=9.1nF, CDH=9.1nF)
Release delay time	:	Typ. 10ms (VDD=3.3V, VS=0V⇒13V, CDL=9.1nF, CDH=9.1nF)
Additional function	:	Separated sense pin

Packages

- SOT-26B

Application

- Voltage monitor for car battery
- Voltage monitor for AC / DC converter output voltage

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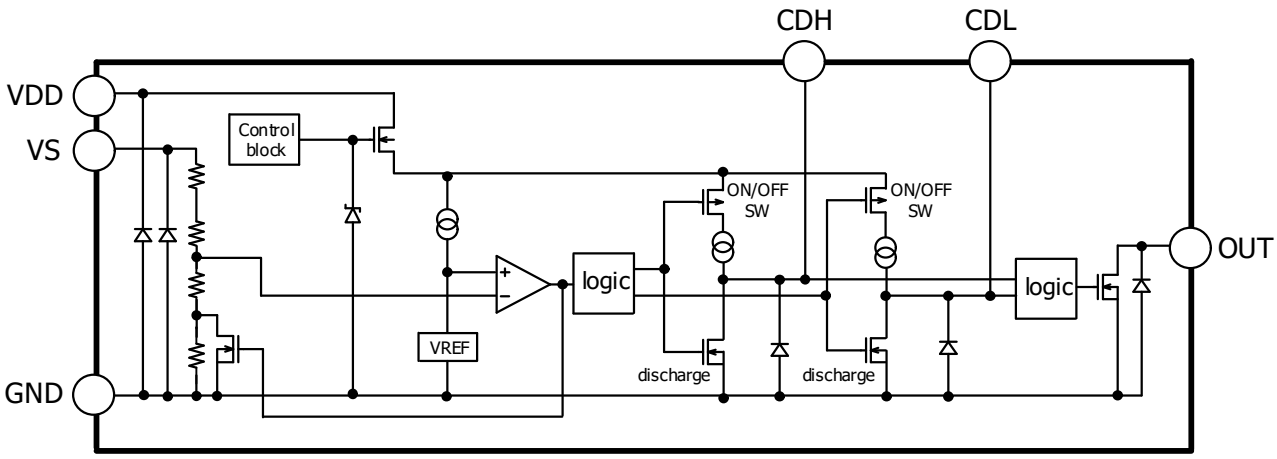
Model Name

P S T 1 1 X X X X X X X

Series name (A) (B) (C) (D) (E) (F)

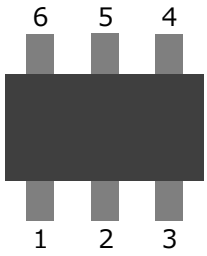
(A)	Function Type	4	Reset output logic Active L
		D	Reset output logic Active H
(B)	Hysteresis voltage	A	VTH×0.02 ≦ Hysteresis voltage(typ.) < VTH×0.03
		B	VTH×0.03 ≦ Hysteresis voltage(typ.) < VTH×0.04
		C	VTH×0.04 ≦ Hysteresis voltage(typ.) < VTH×0.05
		D	VTH×0.05 ≦ Hysteresis voltage(typ.) < VTH×0.075
		E	VTH×0.075 ≦ Hysteresis voltage(typ.) < VTH×0.1
		F	VTH×0.1 ≦ Hysteresis voltage(typ.) < VTH×0.2
		G	VTH×0.2 ≦ Hysteresis voltage(typ.) < VTH×0.3
		H	VTH×0.3 ≦ Hysteresis voltage(typ.) < VTH×0.4
		J	VTH×0.4 ≦ Hysteresis voltage(typ.) < VTH×0.5
		K	VTH×0.5 ≦ Hysteresis voltage(typ.) < VTH×0.75
		L	VTH×0.7 ≦ Hysteresis voltage(typ.) < VTH×1
		M	VTH×1 ≦ Hysteresis voltage(typ.)
		N	VTH×0.0513 = Hysteresis voltage(typ.)
(C)	Reset detection voltage	50 ≀ 00	Reset detection voltage range is 5.0V to 10.0V. When the detection voltage is 5.0 to 9.9V,specify it with "50" to "99". When the detection voltage is 10.0V,specify it with "00".
(D)	Package	N	SOT-26B
(E)	Packing specifications 1	R	R housing (Standard)
(F)	Packing specifications 2	H	Embos tape / Halogen free

Block Diagram



Pin Configuration

- SOT-26B



Top view

Pin No.	Pin name	Function
1	VDD	Power supply input pin
2	VS	Voltage sensing pin
3	OUT	Output pin
4	CDH	Release delay pin with external capacitor
5	GND	Ground pin
6	CDL	Reset delay pin with external capacitor

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage	VDD	-0.3	40	V
VS pin voltage	VS	-0.3	40	V
CDH pin voltage	VCDL	-0.3	5.5	V
CDL pin voltage	VCDH	-0.3	5.5	V
OUT pin voltage	VOUT	-0.3	40	V
OUT pin output current	IOUT	-	20	mA
Storage temperature	Tstg	-55	150	℃
Power dissipation	Pd1	-	150	mW

Recommended Operating Conditions

Item	Symbol	Min.	Max.	Unit
Operating ambient temperature	Topr	-40	105	℃
Operating voltage	Vop	2.7	20	V

Electrical Characteristics

(Ta=-40~105°C, typically value at VDD=3.3V, Ta=25°C, unless otherwise specified *Note1)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Consumption current	IDD	VDD=3.3V VS=16V	PST114	-	1.7	2.9	μA	B
			PST11D	-	2.3	3.5	μA	B
Output current	IOL	VDD=3.3V VS=0V, VOUT=0.5V	PST114	1	-	-	mA	C
		VDD=3.3V VS=20V, VOUT=0.5V	PST11D	1	-	-	mA	C
Output leakage current	ILEAK	VDD=20V VS=20V, VOUT=20V	PST114	-	-	2	μA	C
		VDD=20V VS=0V, VOUT=20V	PST11D	-	-	2	μA	C
Reset transfer delay time	TdHLC1	VDD=3.3V, VS=13V→0V CDL=open, CDH=open		35	80	230	μs	D
Reset delay time	TdHLC2	VDD=3.3V, VS=13V→0V CDL=9.1uF, CDH=9.1uF		6.9	10.0	15.7	ms	E
Release transfer delay time	TdLHC1	VDD=3.3V, VS=0V→13V CDL=open, CDH=open		20	60	200	μs	D
Release delay time	TdLHC2	VDD=3.3V, VS=0V→13V CDL=9.1uF, CDH=9.1uF		6.9	10.0	15.7	ms	E
VS pin resistance	RVS1	VDD=3.3V VS=14V		30	60	200	MΩ	E

*Note1:Final inspection is tested Ta=25°C only. Temperature ranges other than 25 °C is guaranteed by design.

Electrical Characteristics

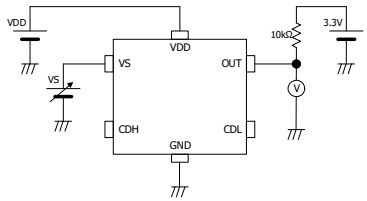
(Ta=-40~105°C, typically value at VDD=3.3V, Ta=25°C, unless otherwise specified *Note1)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Reset voltage	VTH	VDD=3.3V VS:H→L		VTH × 0.98	VTH	VTH × 1.02	V	A
Hysteresis voltage	ΔVTH	VDD=3.3V ΔVTH=VRE-VTH		-	ΔVTH	-	V	A
Release voltage	VRE	VDD=3.3V VS:L→H	ΔVTH<0.1V	VTH×0.98 + (ΔVTH-0.1)	VTH + ΔVTH	VTH×1.02 + (ΔVTH+0.1)	V	A
			ΔVTH≧0.1V	VTH×0.98 + (ΔVTH*0.9)	VTH + ΔVTH	VTH×1.02 + (ΔVTH*1.1)	V	A

*Note1:Final inspection is tested Ta=25°C only. Temperature ranges other than 25 °C is guaranteed by design.

Test Circuit

(A)



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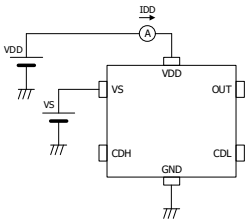

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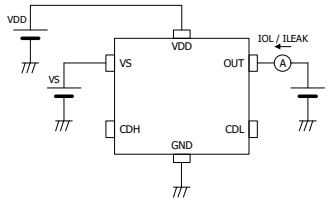

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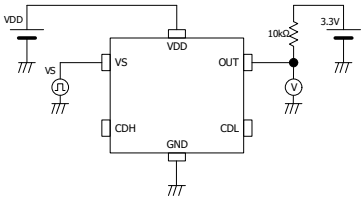
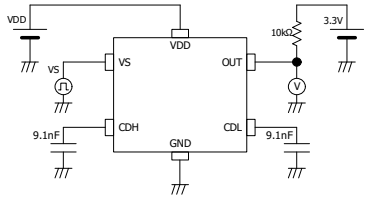


(E)



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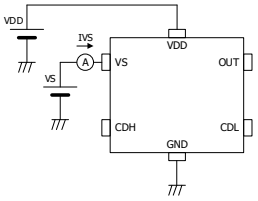
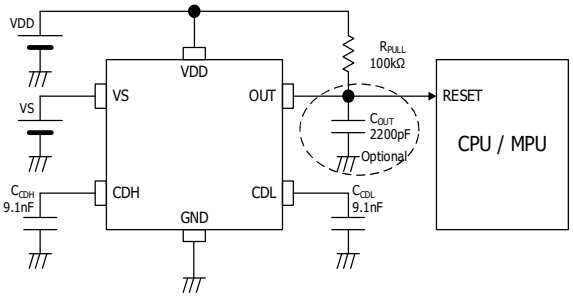


Application Circuit



Note

1. The typical application circuit is not guaranteed for a set applications. It has to test sufficiently in a set applications.

2. In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi shall not be liable for any such problem, nor grant a license therefore.

3. For Surge and over voltage protection, recommend to use ESD protection device such as baristor at battery pin (ex. VDD, VS).

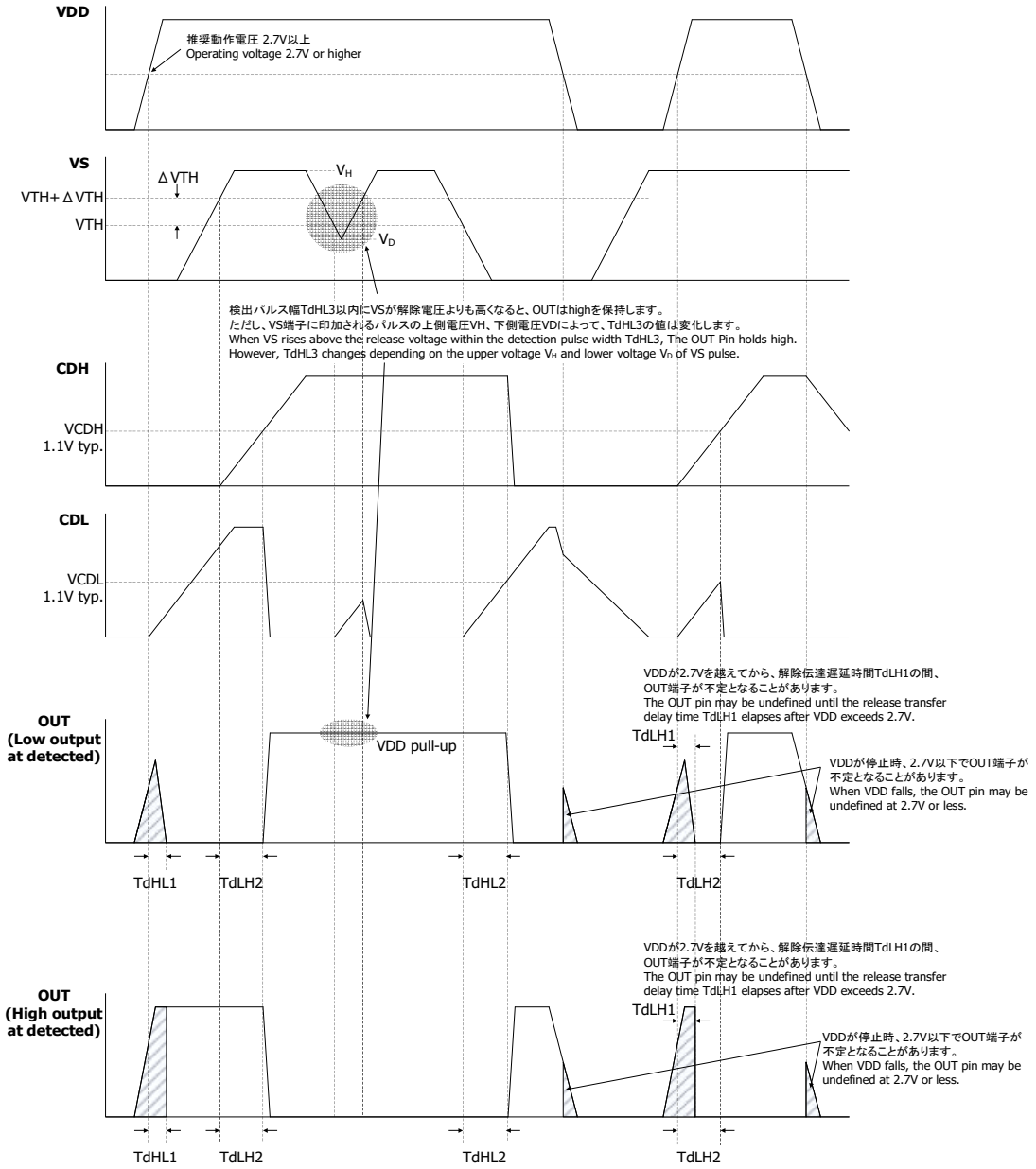
4. If the hysteresis voltage is small, the OUT pin may chatter. It is recommended to connect a about 2200pF capacitor to the OUT pin to prevent chattering.

5. At VDD start-up, the output may be undefined during the transfer delay. After VDD exceeds 2.7V, It is recommended to set the output to wait during reset and release transfer delay time. When VDD falls, the OUT pin may be undefined at 2.7V or less.

6. It is recommended to connect a 100pF～47000pF capacitor to the CDH pin and CDL pin.

7. Between next to each other pin of PST1xx (SOT-26B), it has parasitic capacitance due to Package and IC round, max 0.2pF . Because of next to VS pin and OUT pin, when it happened VS pin voltage is changing rapidly, it afford between pin, it happened over / under shoot.
   To decrease of over / under shoot ,it recommend to connect the capacitor COUT at OUT pin.
   When it may have parasitic capacitance to OUT pin round at set board, it improves layout pattern, separating from changing rapidly node or adding shield of ground.

Timing Chart



* TdHL3 can be calculated by the following formula.

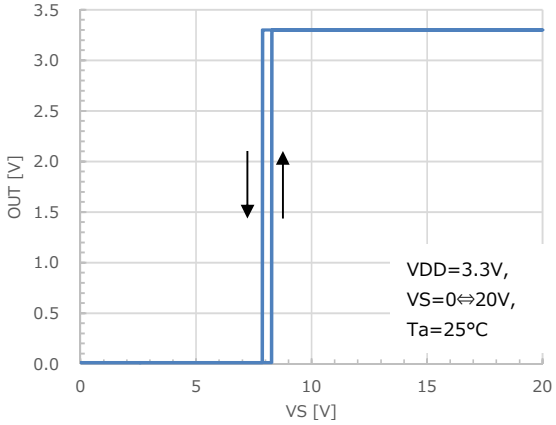
TdHL3 [ms] = KHL x CCDL [nF]

KHL is the detection delay time coefficient.
CCDL is the capacitance value of the capacitor connected to the CDL terminal.
KHL is Min. 0.76、Typ. 1.09、Max. 1.70.

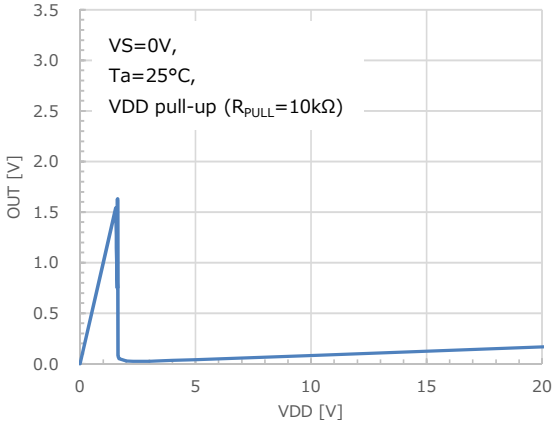
Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

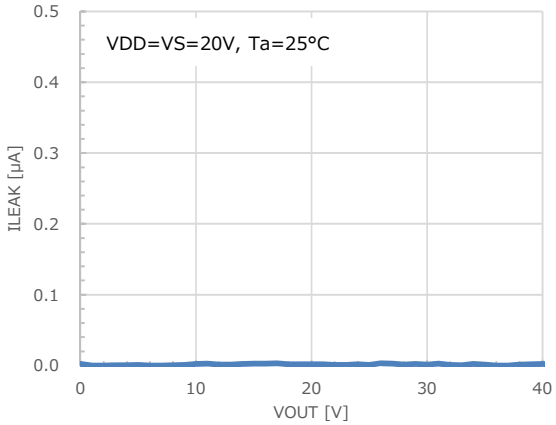
■ Reset voltage - VS



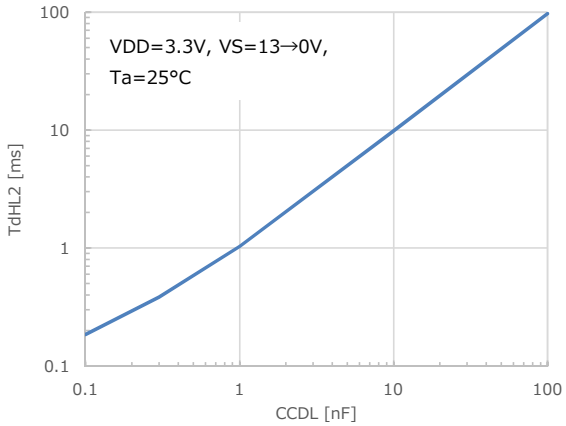
■ OUT pin voltage - VDD



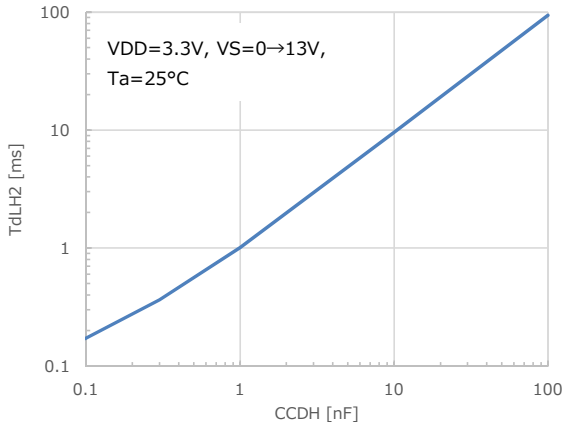
■ Output leakage current - OUT



■ Reset delay time - CDL capacitor C_{CDL}



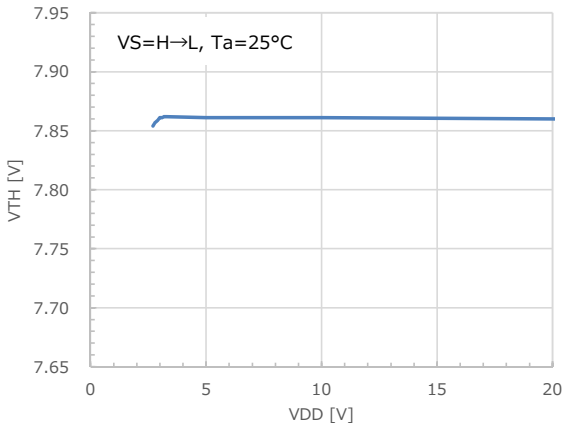
■ Release delay time - CDH capacitor C_{CDH}



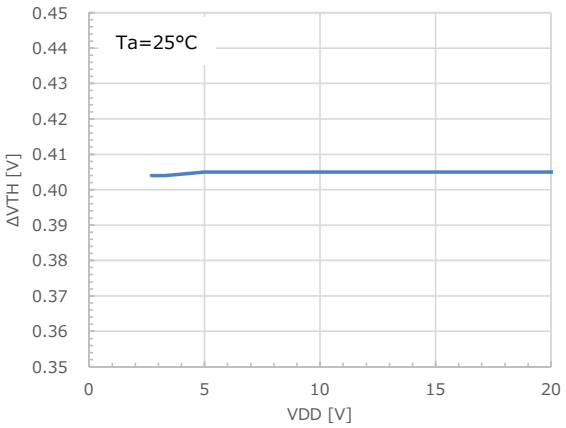
Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

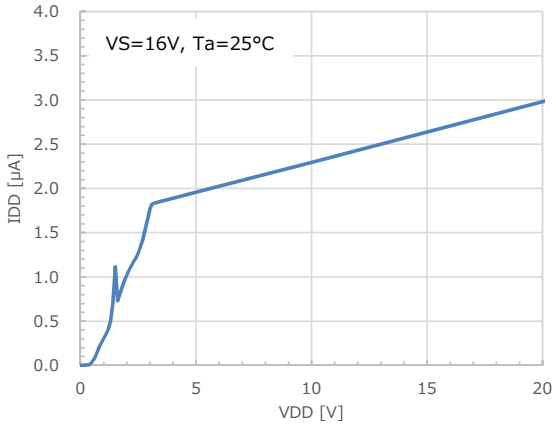
■ Reset voltage - VDD



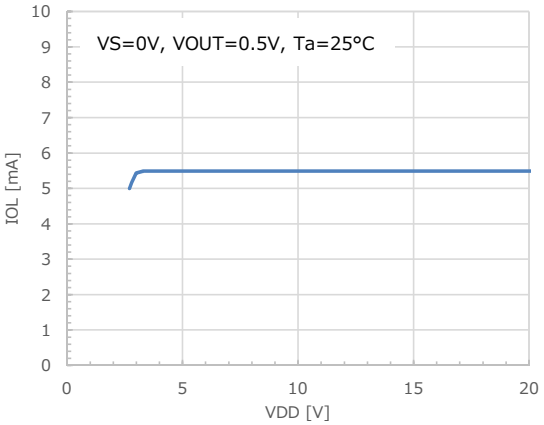
■ Hysteresis voltage - VDD



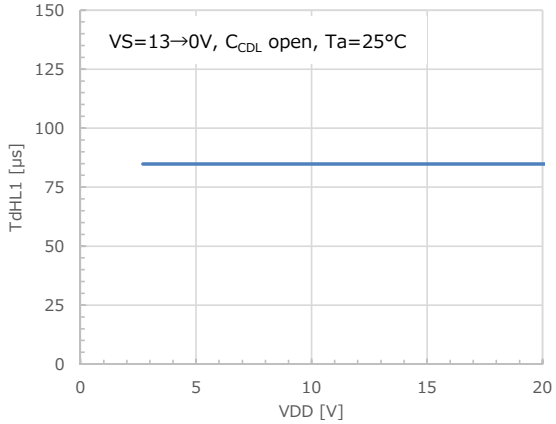
■ Supply current - VDD



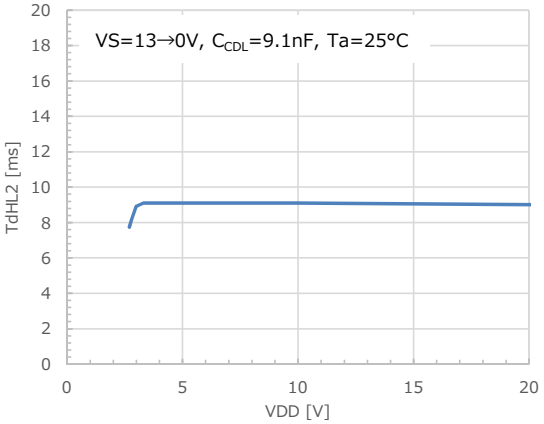
■ Output current - VDD



■ Reset transfer delay time - VDD



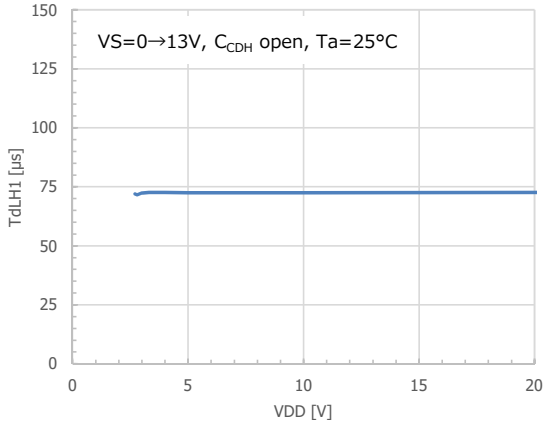
■ Reset delay time - VDD



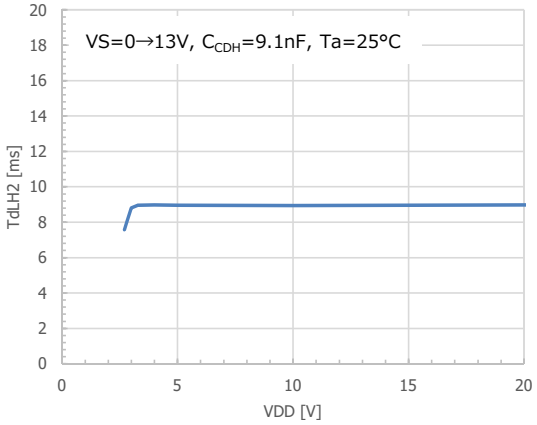
Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

■ Release transfer delay time - VDD



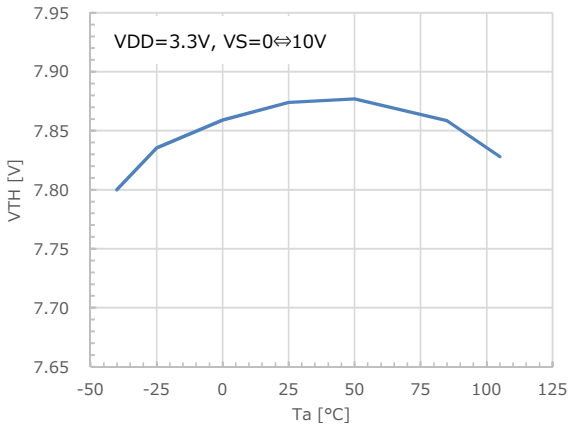
■ Release delay time - VDD



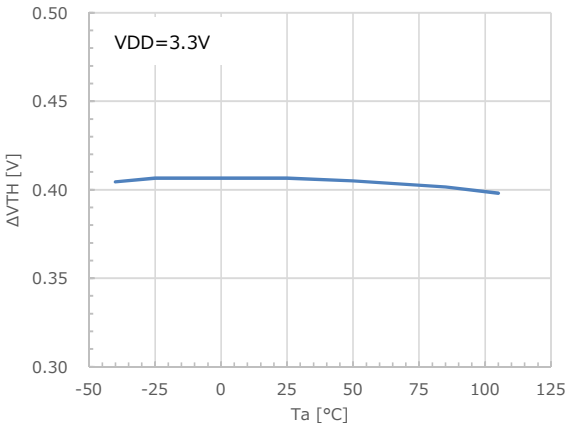
Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

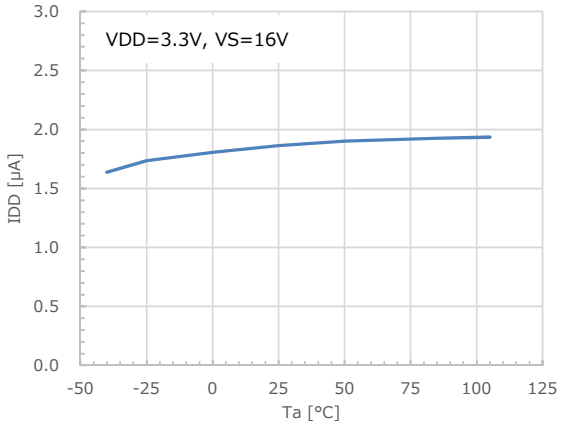
■ Reset voltage - Temperature



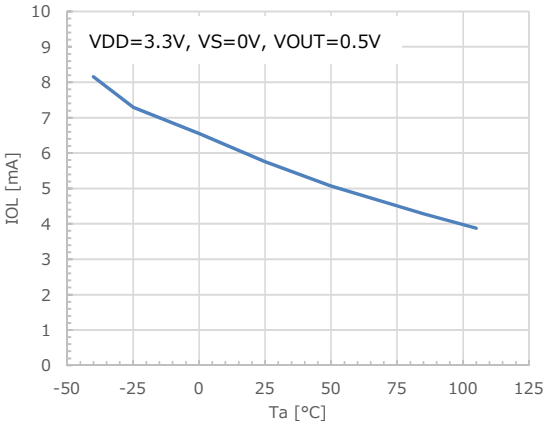
■ Hysteresis voltage - Temperature



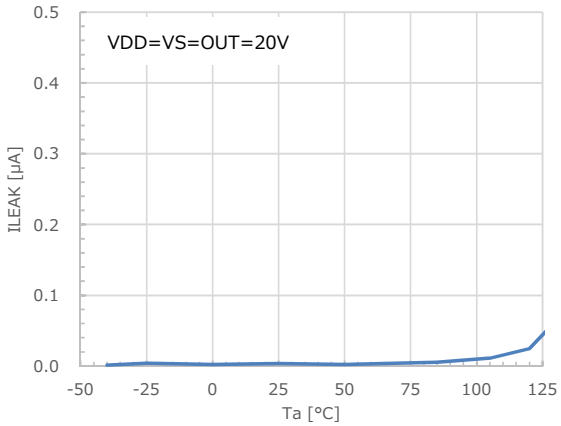
■ Supply current - Temperature



■ Output current - Temperature



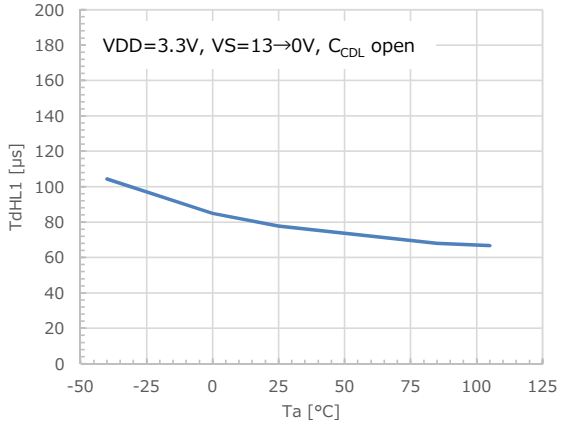
■ Output leakage current - Temperature



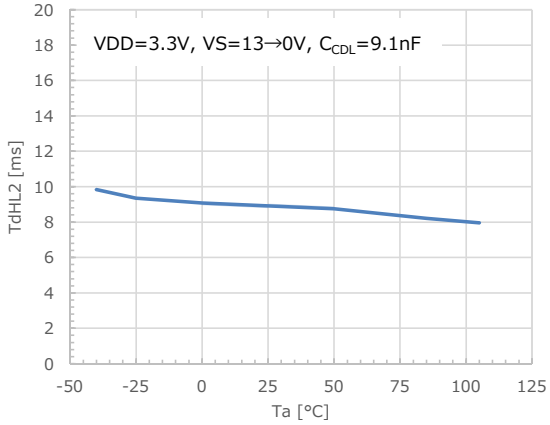
Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

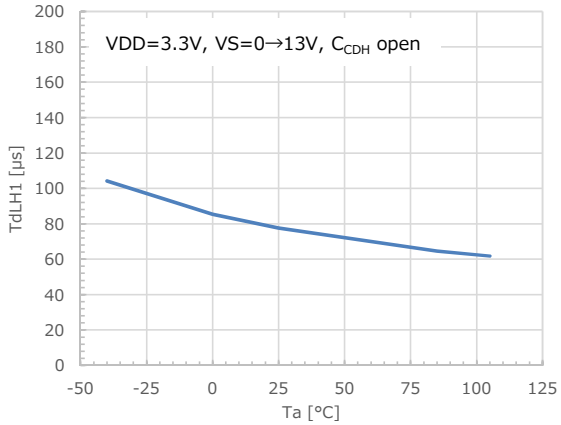
■ Reset transfer delay time - Temperature



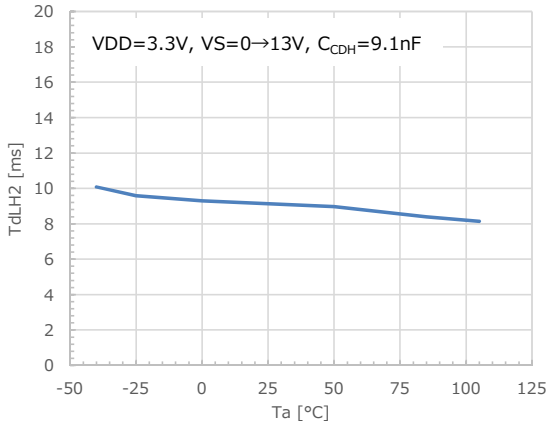
■ Reset delay time - Temperature



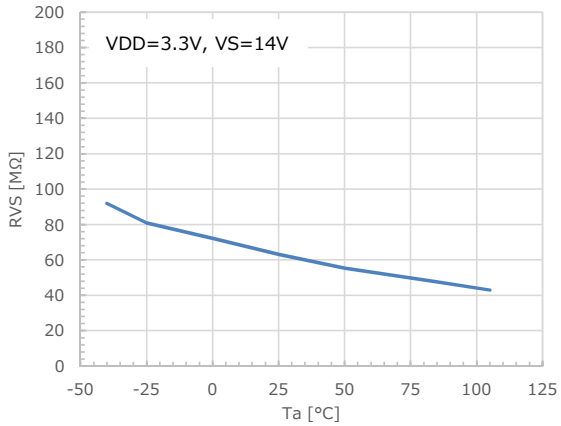
■ Release transfer delay time - Temperature



■ Release delay time - Temperature



■ VS pin resistance - Temperature

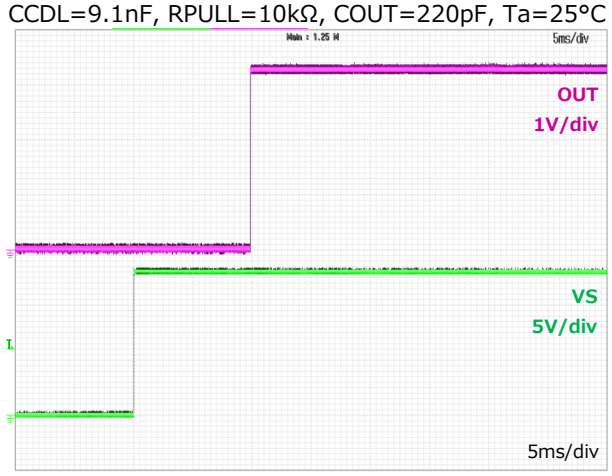


Typical Performance Characteristics

PST114N78N : VTH=7.8V, ΔVTH=0.4V

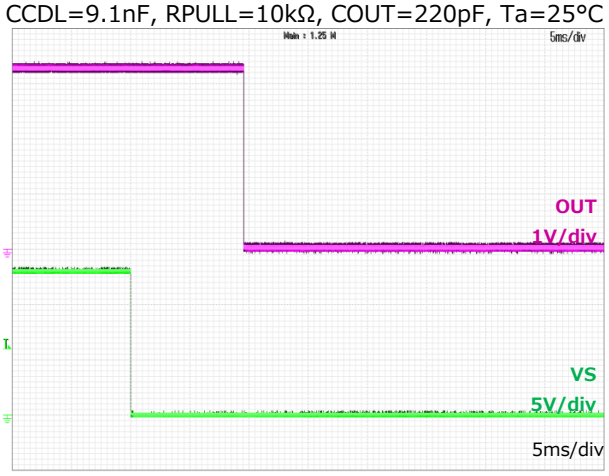
■ Waveform (VS rising)

VDD=3.3V, VS=0→13V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C



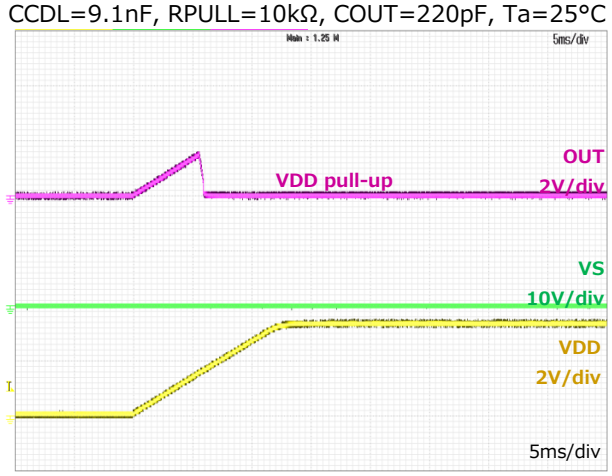
■ Waveform (VS falling)

VDD=3.3V, VS=13→0V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C



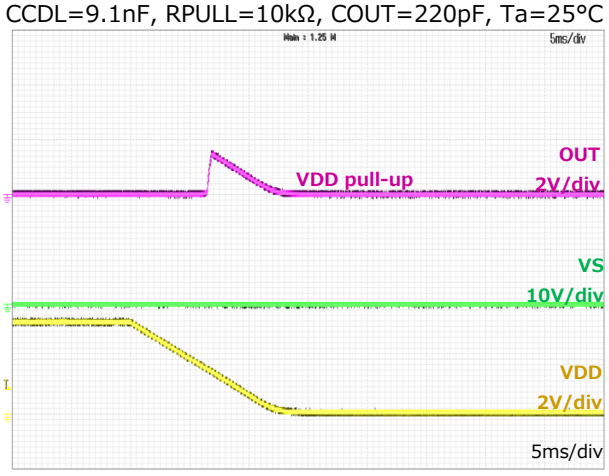
■ Waveform (VDD rising VS=0V)

VDD=0→3.3V, VS=0V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C



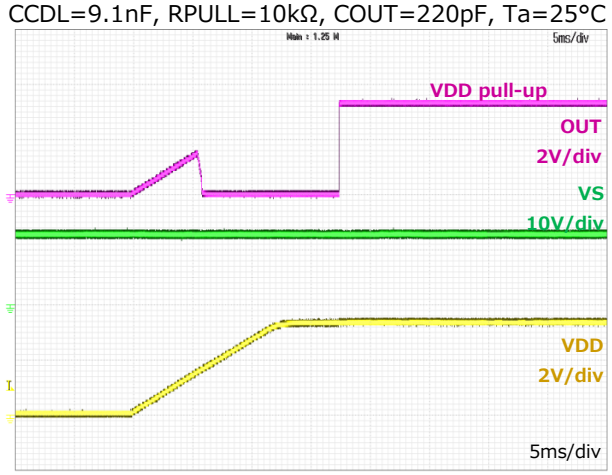
■ Waveform (VDD falling VS=0V)

VDD=3.3→0V, VS=0V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C



■ Waveform (VDD rising VS=13V)

VDD=0→3.3V, VS=13V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C



■ Waveform (VDD falling VS=13V)

VDD=3.3→0V, VS=13V, CCDH=9.1nF,
CCDL=9.1nF, RPULL=10kΩ, COUT=220pF, Ta=25°C