System Reset IC built-in delay time circuit
Monolithic IC PST803~810 series

Outline

These IC series are a system reset IC built-in delay time circuit.
The IC is a small space on PCB by no external capacitor and small package.
The IC is compatible with a standard Reset "809 series", and can choose a detective voltage at 0.1V steps.

Features

1. Operating Supply Voltage		1.0~6.0V (Ta=0~70°C)
2. Supply Current		0.5μA typ.
3. Reset Threshold Range		1.6~5.0V (2.63/2.93/3.08/4.38/4.63V)
4. Reset Threshold Accuracy		±1.0%
5. Reset Temperature Coefficient		30ppm/°C typ.
6. Reset Active Timeout Period		50/100/200/240/400ms
7. Output Voltage L		0.4V max. (Isink=3.2mA)
8. Output Voltage H		VDD−1.5V min. (Isource=800μA)
9. Output type	Open Drain Output + Active L	PST803, PST805
	Open Drain Output + Active H	PST804, PST806
	CMOS Output + Active L	PST807, PST809
	CMOS Output + Active H	PST808, PST810

Package

SOT-23A

Applications

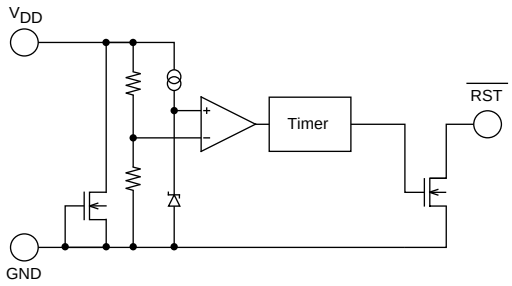
1. The reset circuits of CPU and MPU.
2. The reset circuits of logic circuit.
3. Battery voltage check circuits.
4. The change circuit of a backup circuits.
5. Level detection circuits.
6. Level detector.

Block Diagram

Open Drain Output

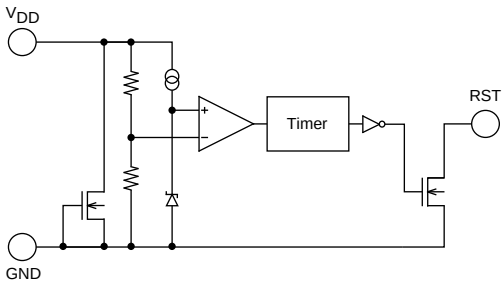
- PST803
- PST805

active-low output



- PST804
- PST806

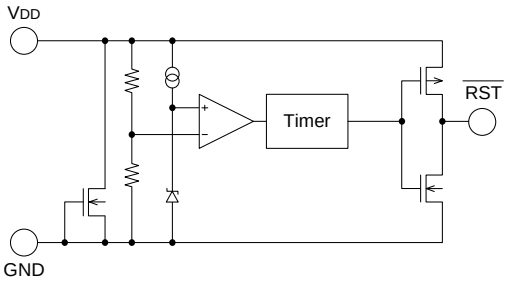
active-high output



CMOS Output

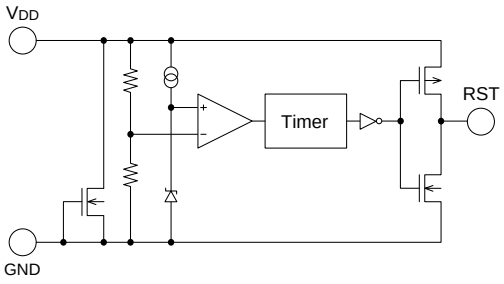
- PST807
- PST809

active-low output



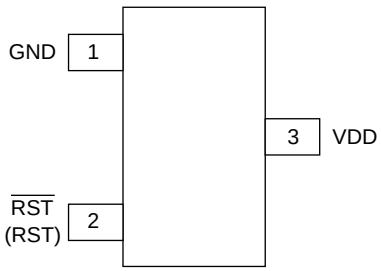
- PST808
- PST810

active-high output

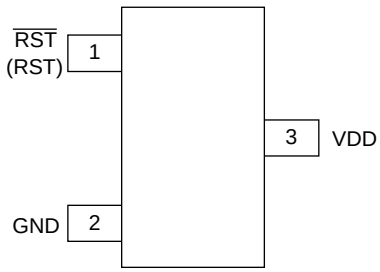


Pin Assignment

PST803, 804, 809, 810



PST805, 806, 807, 808



Pin Description

Pin name	Functions	Internal Equivalent Circuit
GND	GND Pin	Refer to BLOCK DIAGRAM.
RST, $\overline{\text{RST}}$	Reset Signal Output Pin	
VDD	Power Supply Pin / Voltage Detect Pin	

Model Name

P S T 8 0 9 A □ □ □ N □

a b c d e

a			
Function Type			
803	Open drain OUTPUT	Active-Low	SOT-23A 1 : GND 2 : $\overline{RST}$ 3 : VDD
804		Active-High	SOT-23A 1 : GND 2 : RST 3 : VDD
805	Open drain OUTPUT	Active-Low	SOT-23A 1 : $\overline{RST}$ 2 : GND 3 : VDD
806		Active-High	SOT-23A 1 : RST 2 : GND 3 : VDD
807	CMOS OUTPUT	Active-Low	SOT-23A 1 : $\overline{RST}$ 2 : GND 3 : VDD
808		Active-High	SOT-23A 1 : RST 2 : GND 3 : VDD
809	CMOS OUTPUT	Active-Low	SOT-23A 1 : GND 2 : $\overline{RST}$ 3 : VDD
810		Active-High	SOT-23A 1 : GND 2 : RST 3 : VDD

b		c		d		e	
TDEL		VTH		PKG		PACKING SPECIFICATIONS	
A	240ms	160	1.60V	N	SOT-23A	R	R HOUSING, Halogen-contained
B	50ms					L	L HOUSING, Halogen-contained
C	100ms	〃	〃			M	R HOUSING, Halogen-free
D	200ms	500	5.00V			H	L HOUSING, Halogen-free
E	400ms						

Absolute Maximum Ratings

Item	Symbol	Ratings	Units
Supply Voltage	V_{DD} max.	7	V
Output Voltage	RST, $\overline{RST}$	GND-0.3 ~VDDmax+0.3 (CMOS Type) GND-0.3 ~7 (Open Drain Type)	V
Input Current (VDD)	I_{DD}	20	mA
Output Current	I_{OUT}	20	mA
Power Dissipation	P_D	150 (Not attached PCB)	mW
Operating Temperature	Topr	−40~+105	°C
Storage Temperature	Tstg	−65~+150	°C

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating Ambient Temperature	Topr	−40~+105	°C

Electrical Characteristics (Except where noted otherwise Ta=25°C)

Item	Symbol	Test conditions		Min.	Typ.	Max.	Units	Circuit
Operating Voltage	V_{DD}	Ta=0 to 70°C		1.0		6.0	V	①
		Ta=−40 to 105°C		1.1		6.0		
Supply Current	I_{DD}	VDD=V_{TH}+1V			0.5	2.0	μA	②
Reset Threshold	V_{TH}	V_{TH}=4.63V	Ta=25°C	4.584	4.630	4.676	V	①
			Ta=−40 to 85°C	4.500		4.750		
			Ta=85 to 105°C	4.400		4.860		
		V_{TH}=4.38V	Ta=25°C	4.336	4.380	4.424		
			Ta=−40 to 85°C	4.250		4.500		
			Ta=85 to 105°C	4.160		4.560		
		V_{TH}=3.08V	Ta=25°C	3.049	3.080	3.111		
			Ta=−40 to 85°C	3.000		3.150		
			Ta=85 to 105°C	2.920		3.230		
		V_{TH}=2.93V	Ta=25°C	2.901	2.930	2.959		
			Ta=−40 to 85°C	2.850		3.000		
			Ta=85 to 105°C	2.780		3.080		
		V_{TH}=2.63V	Ta=25°C	2.604	2.630	2.656		
			Ta=−40 to 85v	2.550		2.700		
			Ta=85 to 105°C	2.500		2.760		
		V_{TH}=1.6~5.0V (0.1V step)	Ta=25°C	−1.0		+1.0	%	
			Ta=−40 to 85°C	−2.5		+2.5		
			Ta=85 to 105°C	−5.0		+5.0		
Reset Threshold Temp. Coefficient	$V_{TH}/\Delta T$				30		ppm/°C	①
RST output voltage Low (active L type)	V_{OL}	VDD=V_{TH}−0.1V, Isink=1.2mA V_{TH}≦3.08V				0.3	V	③
		VDD=V_{TH}−0.1V, Isink=3.2mA V_{TH}>3.08V				0.4		
RST output voltage High (active H type)	V_{OH}	VDD=V_{TH}+1V, Isink=500μA V_{TH}≦3.08V		0.8*VDD			V	
		VDD=V_{TH}+1V, Isink=800μA V_{TH}>3.08V		VDD-1.5				
RST output voltage low (active L type)	V_{OL}	VDD=V_{TH}+1V, Isink=1.2mA V_{TH}≦3.08V				0.3	V	
		VDD=V_{TH}+1V, Isink=3.2mA V_{TH}>3.08V				0.4		
RST output voltage High (active H type)	V_{OH}	VDD=V_{TH}−0.1V, Isink=500μA V_{TH}≦3.08V		0.8*VDD			V	
		VDD=V_{TH}−0.1V, Isink=800μA V_{TH}>3.08V		VDD-1.5				

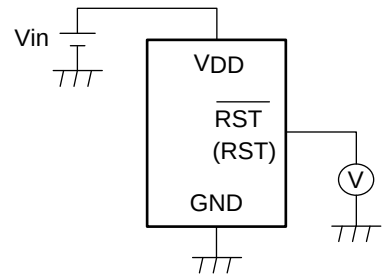
Note1 : This device is tested at Ta=25°C, over temperature limits guaranteed by design only.
Note2 : The parameter is guaranteed by design.

Item	Symbol	Test conditions		Min.	Typ.	Max.	Units	Circuit
Reset Active Timeout Period	tdel	A	Ta=−40 to 85°C	140	240	310	ms	④
			Ta=85 to 105°C	100		840		
		B	Ta=−40 to 85°C	35	50	65		
			Ta=85 to 105°C	25		98		
		C	Ta=−40 to 85°C	70	100	130		
			Ta=85 to 105°C	49		195		
		D	Ta=−40 to 85°C	140	200	260		
			Ta=85 to 105°C	98		390		
		E	Ta=−40 to 85°C	280	400	520		
			Ta=85 to 105°C	196		780		
VDD to Reset Delay	t_{TH}	VDD=(V_{TH}+1V) to (V_{TH}-100mV) (Note2)			20		µs	④
Output Leakage Current (Active L, Open Drain Type)	I_{LEAK}	VDD=V_{RST}=7V				0.1	µA	⑤

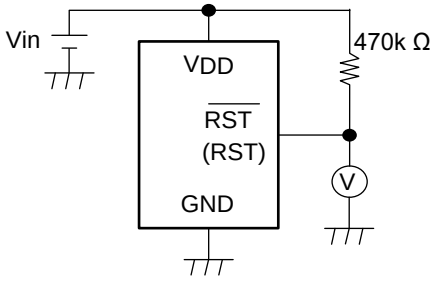
Note1 : This device is tested at Ta=25°C, over temperature limits guaranteed by design only.
Note2 : The parameter is guaranteed by design.

Test Circuit

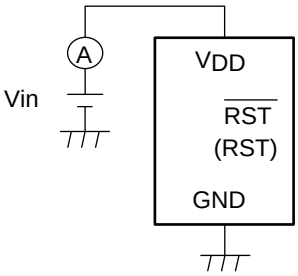
① -a CMOS output type



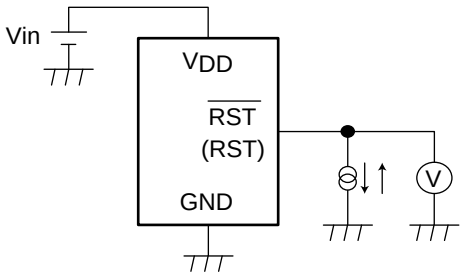
① -b open dain output type



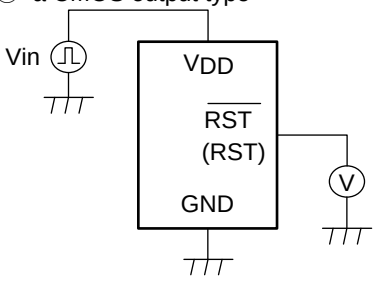
②



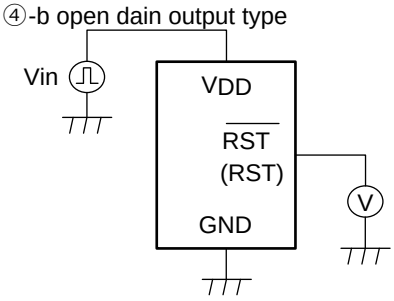
③

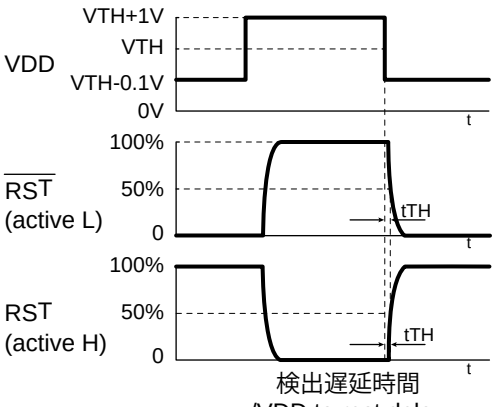


④ -a CMOS output type

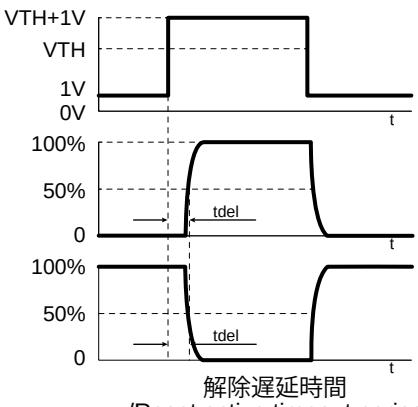


④-b open dain output type



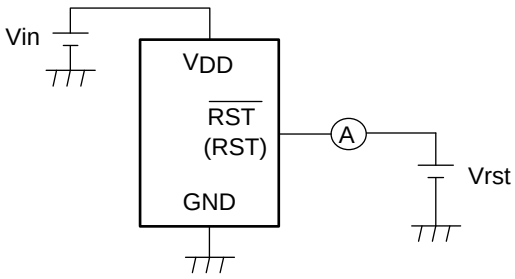


検出遅延時間
/VDD to rest delay



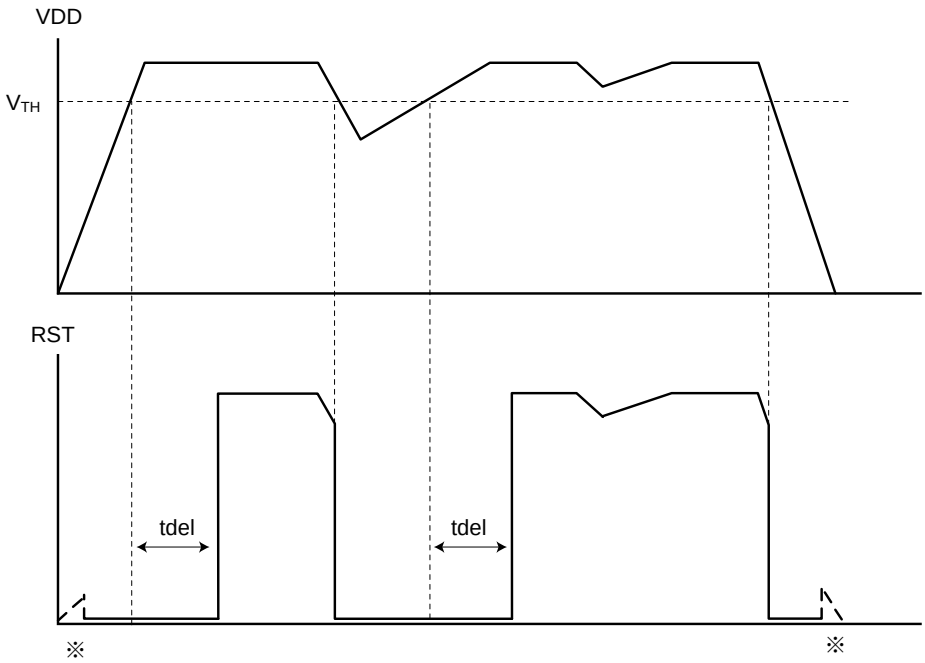
解除遅延時間
/Reset active timeout period

⑤



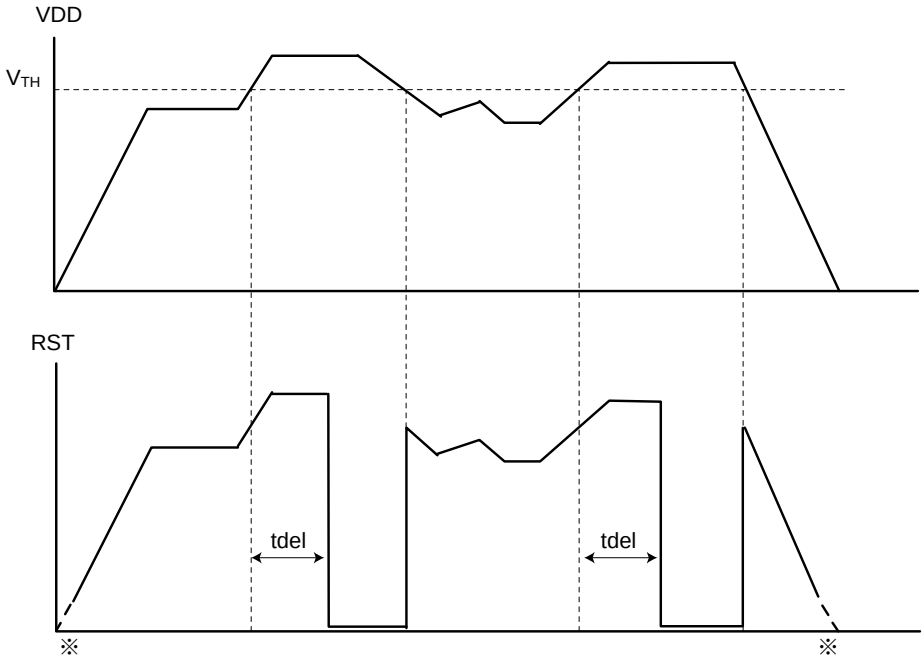
Timing Chart

PST803, 805, 807, 809 Active-Low Output Type



※VDD<1V region is, it will be operating limits. The output is undefined.

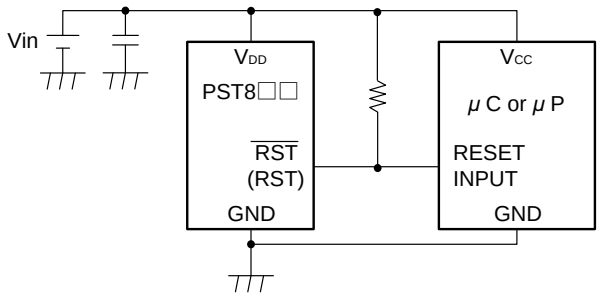
PST804, 806, 808, 810 Active-High Output Type



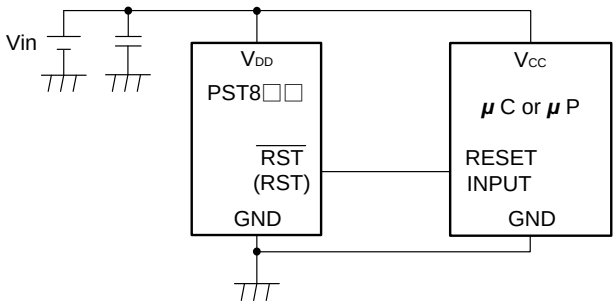
※VDD<1V region is, it will be operating limits. The output is undefined.

Application Circuit

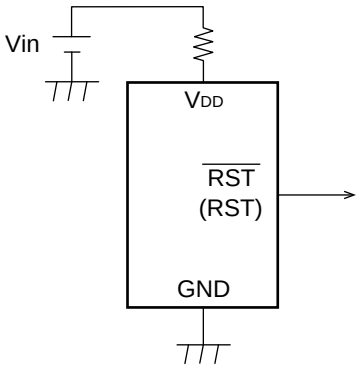
PST803, 804, 805, 806



PST807, 808, 809, 810



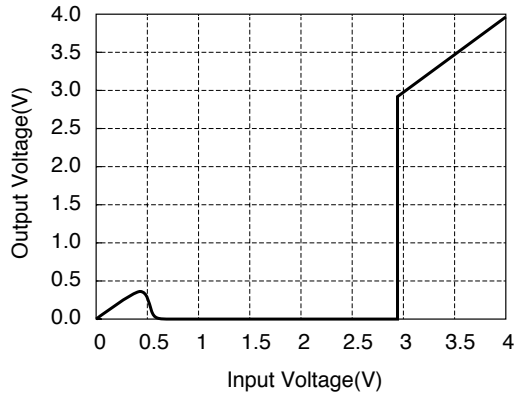
· Note



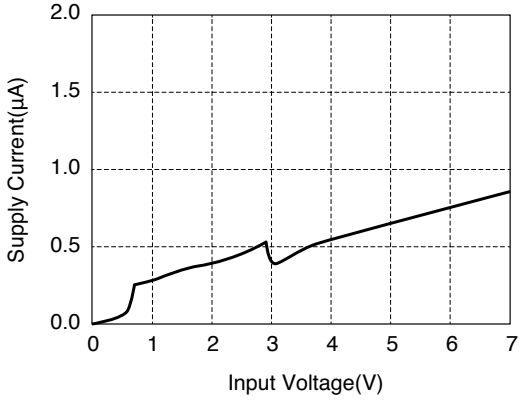
1. Please note that there is any possibility of circuit oscillation when resistance put in the line VIN.
2. Current and load resistance should be adjusted, which not over power dissipation level.
   PD ＞ (VDD-VOH) · IOH
   PD ＞ VOL · IOL
3. We shall not be liable for any trouble or damage caused by using this circuit.
4. In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefore.

Characteristics (2.93V, active L)

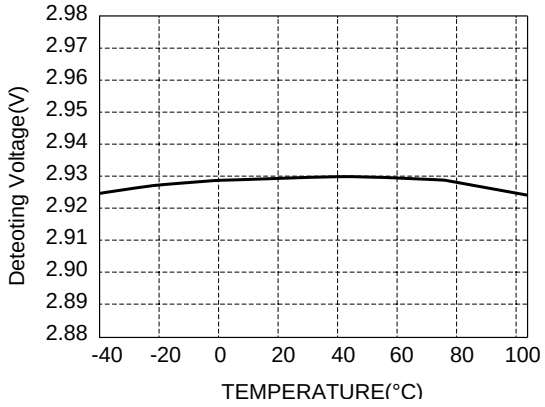
■ DETECTING VOLTAGE



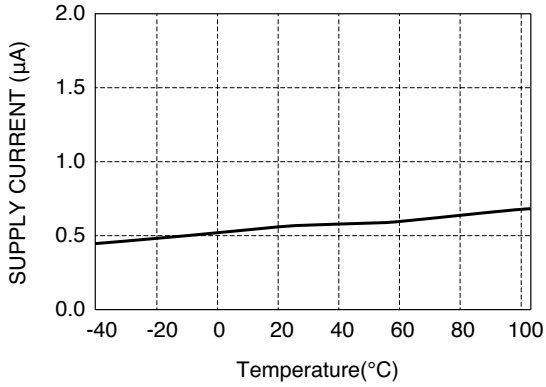
■ SUPPLY CURRENT



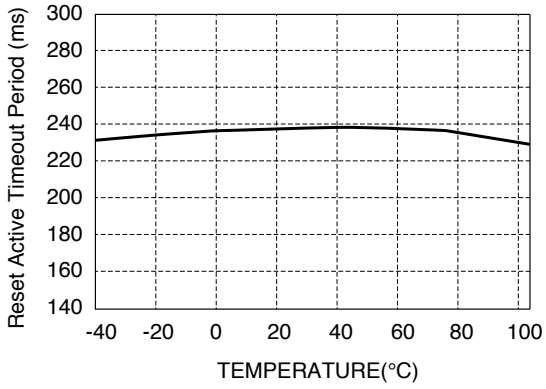
■ DETECTING VOLTAGE VS TEMPERATURE



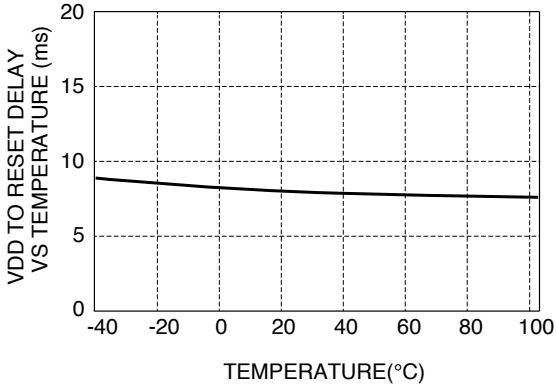
■ SUPPLY CURRENT VS TEMPERATURE



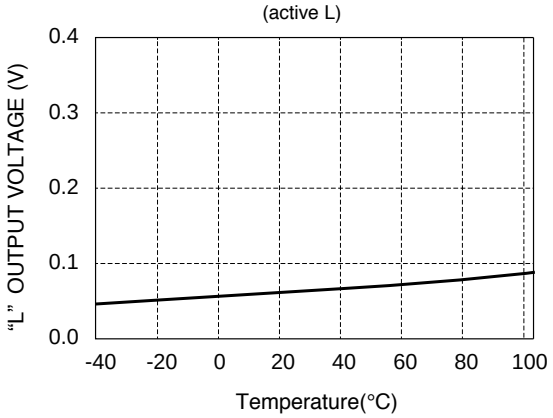
■ RESET ACTIVE TIMEOUT PERIOD VS TEMPERATURE



■ VDD TO RESET DELAY VS TEMPERATURE



■ “L” OUTPUT VOLTAGE VS TEMPERATURE



■ “H” OUTPUT VOLTAGE VS TEMPERATURE