IC for CMOS System Reset
Monolithic IC PST4XXAXXXN Series

Outline

This is a system reset IC developed using the CMOS process. The CMOS process allows ultra-low current consumption of 1.5μA(typ.). Further, a fixed delay timer is built in, so that supply voltage is verified when the power is turned on or interrupted to reset the system accurately.

Features

1. Detection voltage accuracy ±1.5% (25°C, V_{DD} = V_{DET} + 0.1)
2. Low current consumption SOT-23 : 1.5μA
3. No external capacitor for delay timer required
   Built-in delay timer SOT-23 : 50/100/200/240/400ms
4. Enhanced rank lineup available for detection voltage, package, output configuration and delay timer.
5. Wide operating temperature range −40 ~ +105°C.

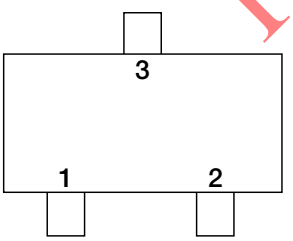
Package

SOT-23A

Applications

1. Reset circuits for microcomputers, CPUs and MPUs
2. Reset circuits for logic circuits
3. Battery voltage check circuits
4. Back-up power supply switching circuits
5. Level detection circuits
6. Mechanical reset circuits

Pin Assignment



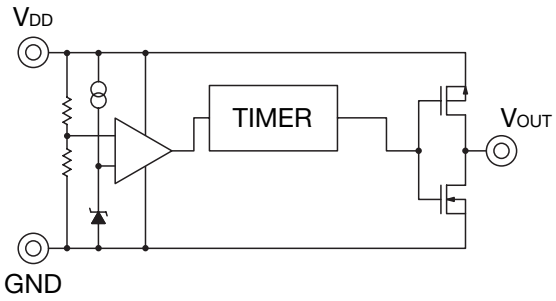
1	GND
2	V_{OUT}
3	V_{DD}

SOT-23A

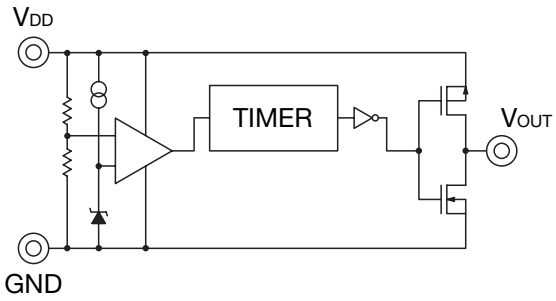
Block Diagram

CMOS Output

PST41□A□□□N□ Active-Low Output

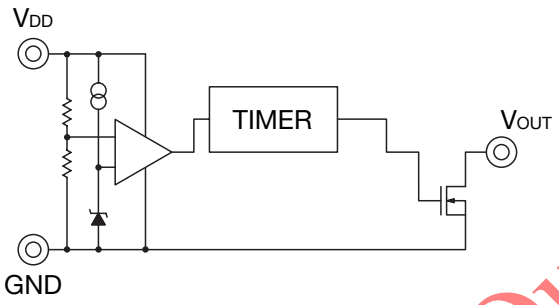


PST43□A□□□N□ Active-High Output

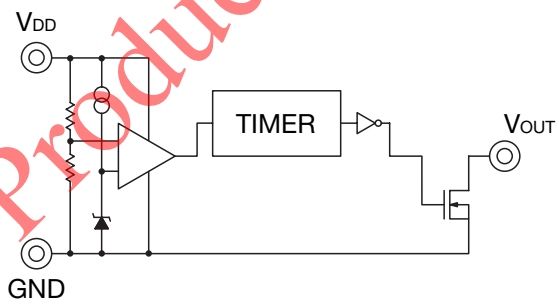


N-ch Open Drain Output

PST42□A□□□N□ Active-Low Output



PST44□A□□□N□ Active-High Output



Pin Explanations

Pin No.	Pin Name	Function
1	GND	GND Pin
2	VOUT	Reset Signal Output Pin
3	VDD	Power Supply Pin/Voltage Detect Pin

Pin Explanations

PST4□□A□□□N□
a b d f

a		b		d		f	
Output Type		TDEL Rank		VDET Rank		Packing Specifications	
1	CMOS Output Active-Low Output	1	50ms	160	VDET=1.60V	R	R Housing
2	N-ch Open Drain Output Active-Low Output	2	100ms	〃	〃	L	L Housing
3	CMOS Output Active-High Output	3	200ms	480	VDET=4.80V		
4	N-ch Open Drain Output Active-High Output	4	240ms				
		5	400ms				

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Operating Temperature	T_{OPR}	−40~+105	°C
Storage Temperature	T_{STG}	−65~+160	°C
Supply Voltage	V_{DD} max.	6.5	V
Output Voltage	V_{OUT}	GND-0.3~VDD max.+0.3(CMOS Type) GND-0.3~6.5(N-ch Open Drain Type)	V
Output Current	I_{OUT}	20	mA
Power Dissipation	P_D	150	mW

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Operating Temperature	T_{OPR}	−40~+105	°C

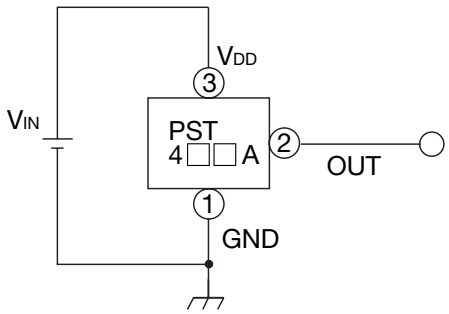
Electrical Characteristics (Unless otherwise specified, Ta=25°C)

Item	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
V_{DD} Range	V_{DD}	Test Circuit 1		1.0		6.0	V
Detecting Voltage	V_{DET}	Test Circuit 1		−1.5%	1.6V~4.8V (0.1V STEP)	+1.5%	V
Detecting Voltage Temp. Coefficient	$V_{DET}/\Delta T$	−40°C≦T_{OPR}≦105°C Test Circuit1			±30		ppm/°C
Supply Current	I_{SS}	V_{DD}=V_{DET}+0.1 Test Circuit 2			1.5	3.5	µA
"H" Out put Voltage (PST41□A /42□A)	V_{OH}	PST4□□□160N□~ PST4□□□230N□	V_{DD}=V_{DET}−0.1V I_{OUT}=150µA	0.8V_{DD}			V
		PST4□□□240N□~ PST4□□□350N□	V_{DD}=V_{DET}−0.1V I_{OUT}=500µA				
		PST4□□□360N□~ PST4□□□480N□	V_{DD}=V_{DET}−0.1V I_{OUT}=800µA				
		Test Circuit 6					
"L" Out put Voltage (PST41□A /42□A)	V_{OL}	PST4□□□160N□~ PST4□□□350N□	V_{DD}=V_{DET}+0.1V I_{OUT}=1.2mA			0.3	V
		PST4□□□360N□~ PST4□□□480N□	V_{DD}=V_{DET}+0.1V I_{OUT}=3.2mA			0.4	V
		Test Circuit 7					
"H" Out put Voltage (PST43□A /44□A)	V_{OH}	PST4□□□160N□~ PST4□□□230N□	V_{DD}=V_{DET}+0.1V I_{OUT}=150µA	0.8V_{DD}			V
		PST4□□□240N□~ PST4□□□350N□	V_{DD}=V_{DET}+0.1V I_{OUT}=500µA				
		PST4□□□360N□~ PST4□□□480N□	V_{DD}=V_{DET}+0.1V I_{OUT}=800µA				
		Test Circuit 6					
"L" Out put Voltage (PST43□A /44□A)	V_{OL}	PST4□□□160N□~ PST4□□□350N□	V_{DD}=V_{DET}−0.1V I_{OUT}=1.2mA			0.3	V
		PST4□□□360N□~ PST4□□□480N□	V_{DD}=V_{DET}−0.1V I_{OUT}=3.2mA			0.4	V
		Test Circuit 7					
Reset Active Timeout Period	T_{DEL}	Test Circuit 8		35	50	65	ms
				70	100	130	
				140	200	260	
				170	240	310	
				280	400	520	
V_{DD} to Reset Delay	T_{DET}	Test Circuit 8			20		µs
Output Leakage Current (PST42□A /44□A)	I_{LEAK}	Test Circuit 5				0.1	µA

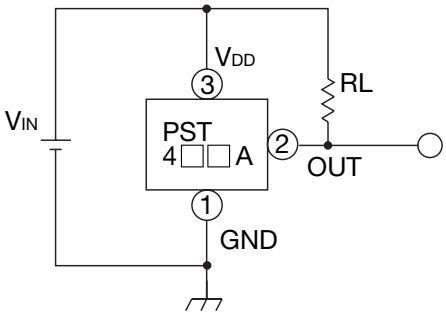
Note 1: This device is tested at only normal temperature. Over temperature limit guaranteed by desigh only.
Note 2: This device has no Hysteresis Voltage.

Measuring Circuit

(1)-a PST41□A / 43□A



(1)-b PST42□A / 44□A



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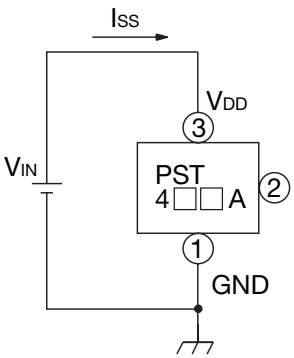

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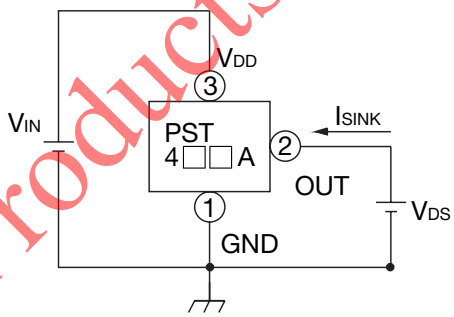

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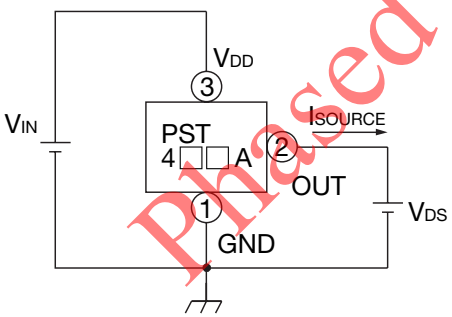

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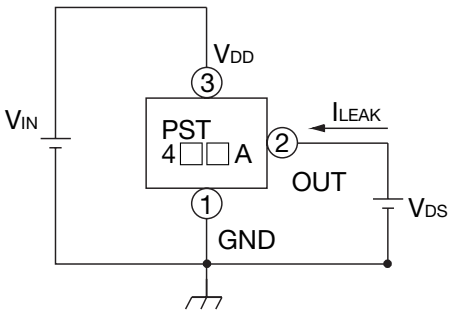
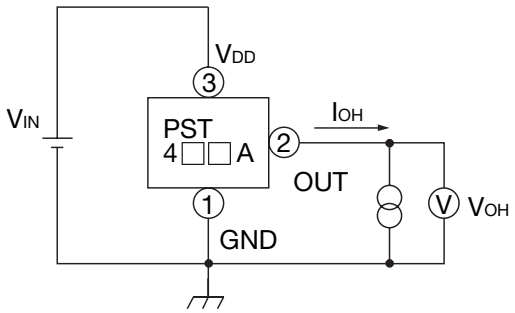


Measuring Circuit

(6)



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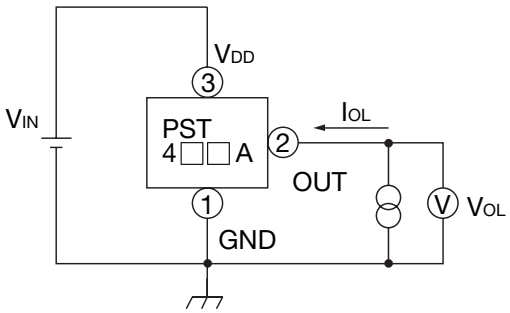
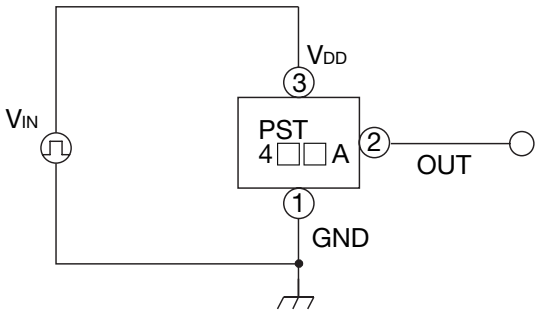
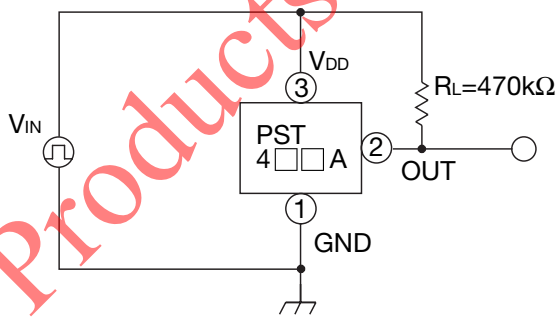
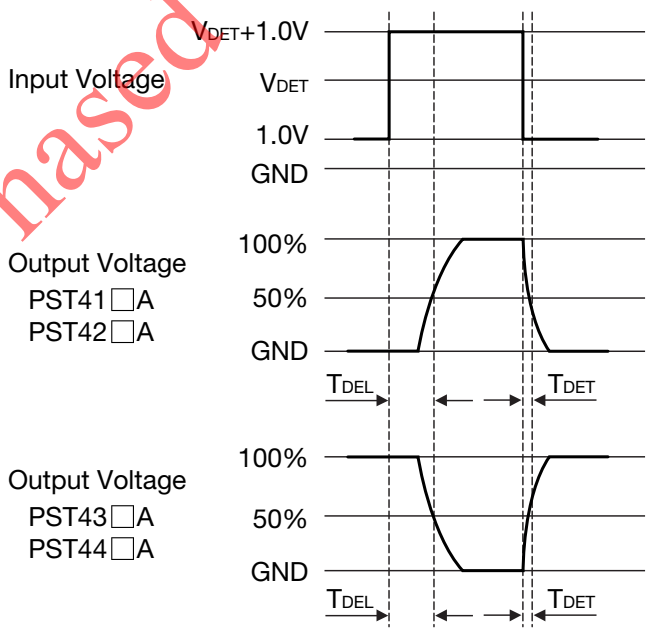


(8) PST41□A / 43□A



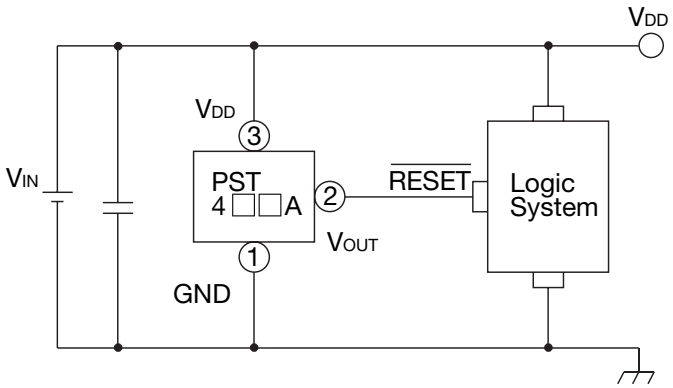
(9) PST42□A / 44□A

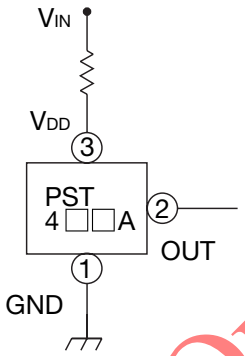




Delay Time

Application Circuits





Please note that there is any possibility of circuit oscillation when resistance put in the line VIN.

Load current and load resistance should be adjusted, which not over power dissipation level.

$PD > (V_{DD} - V_{OH}) \cdot I_{OH}$

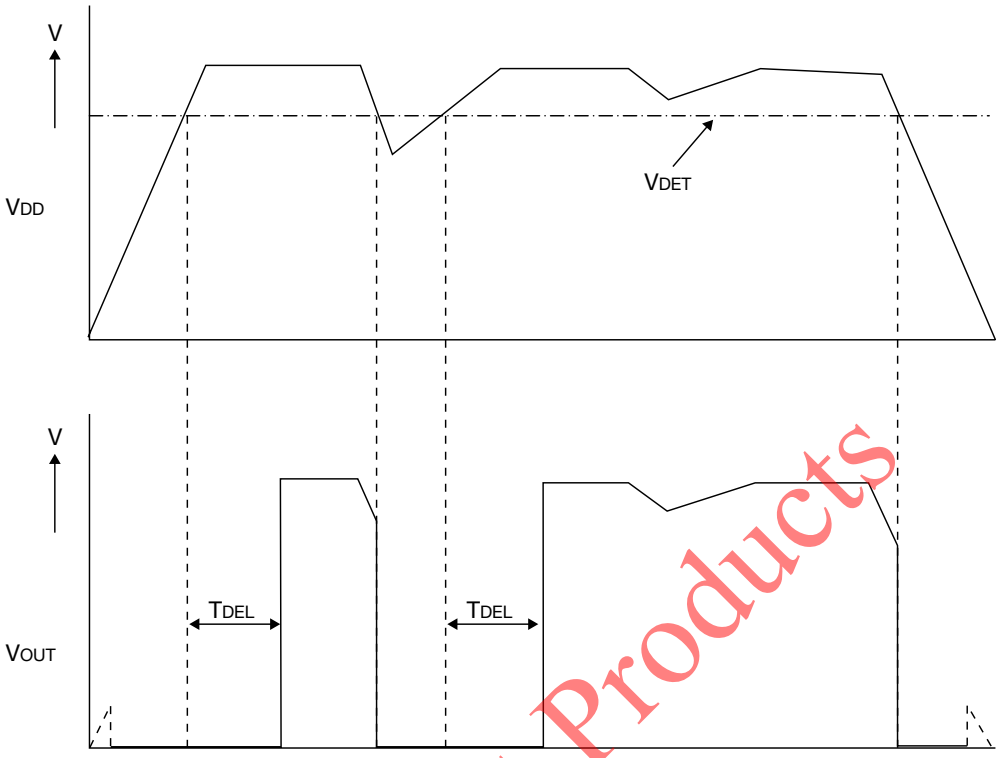
$PD > V_{OL} \cdot I_{OL}$

We shall not be liable for any trouble or damage caused by using this circuit.

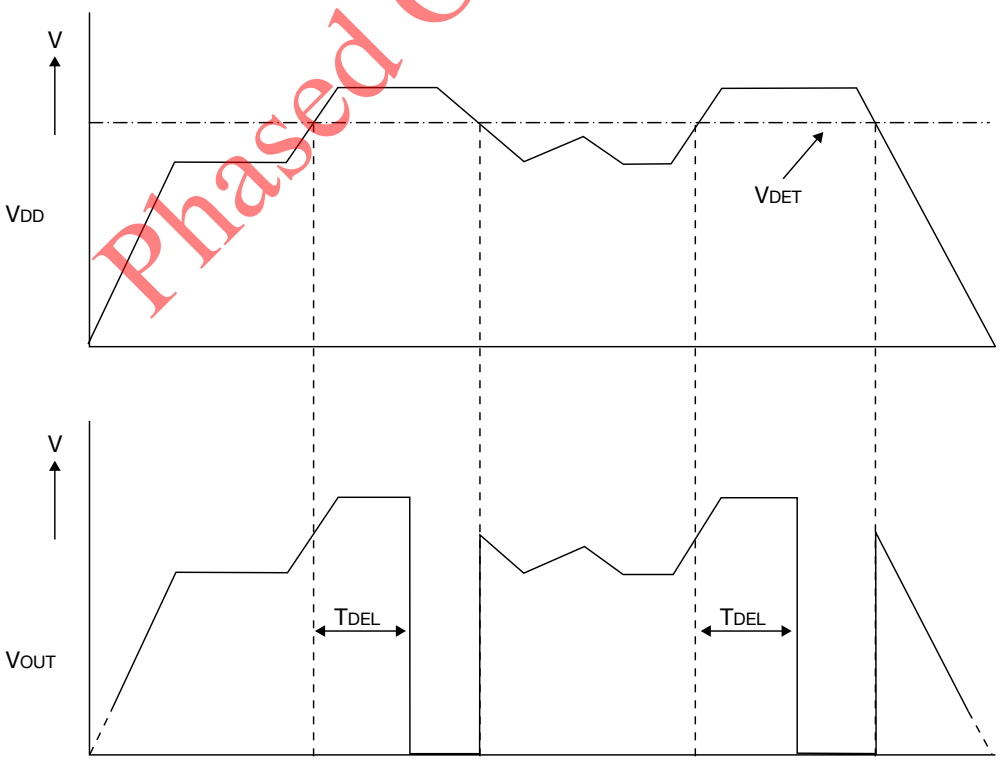
In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefore.

Timing Chart

PST41□A / 42□A Active-Low Output

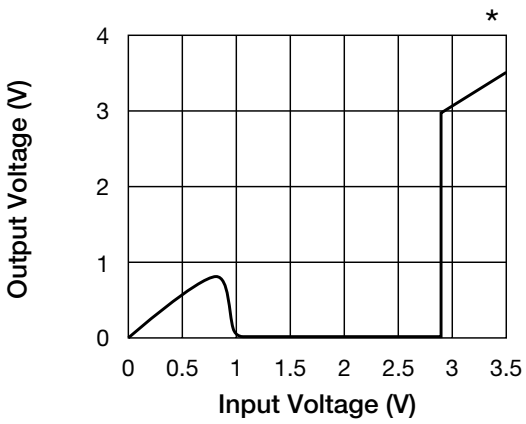


PST43□A / 44□A Active-High Output



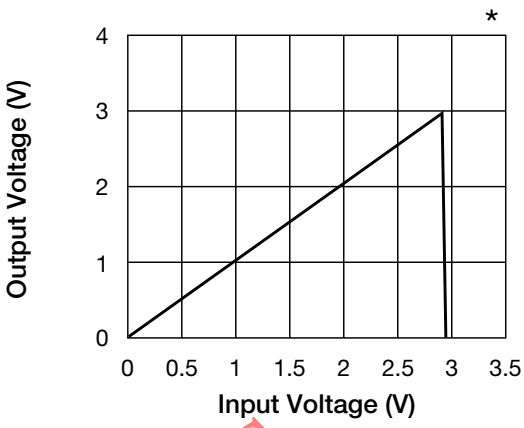
Characteristics

Detecting voltage (PST414A290N□)



Test Circuit 1-b (R_L=12kΩ)

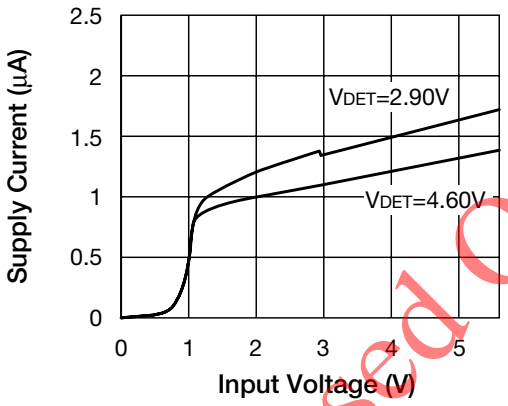
Detecting voltage (PST434A290N□)



Test Circuit 1-b (R_L=12kΩ)

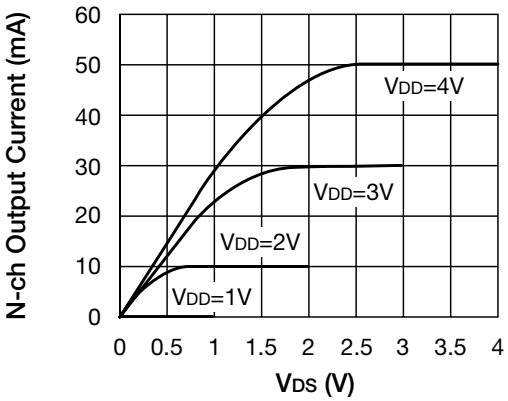
* When Input Voltage is Under 1.0V, Output Voltage is Unstable.

Supply current



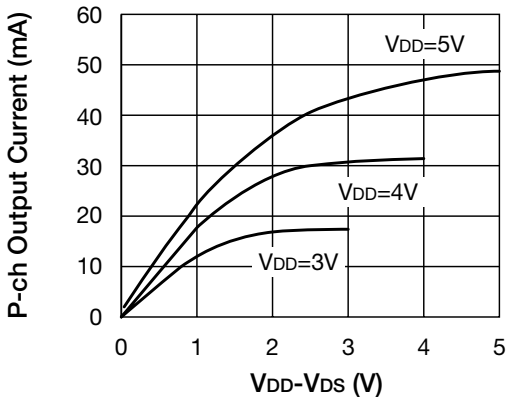
Test Circuit 2

N-ch Output current (PST414A460N□)



Test Circuit 3

P-ch Output current (PST414A290N□)

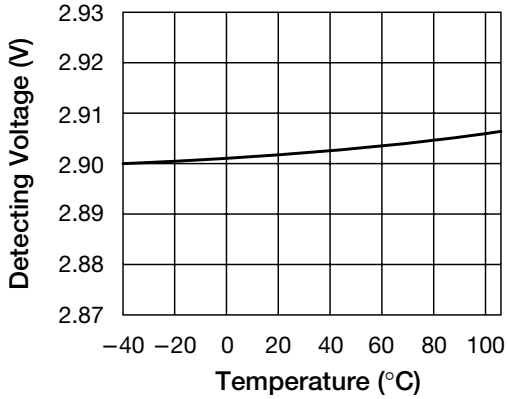


Test Circuit 4

Note: These are typical characteristics.

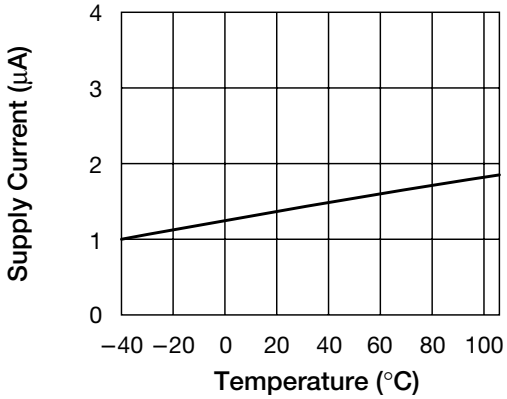
Characteristics

Detecting voltage vs temperature (PST414A290N□)



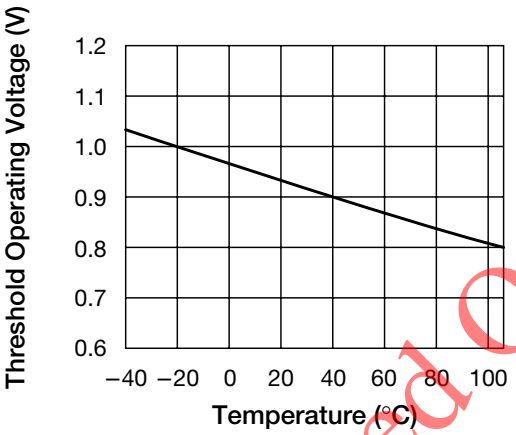
Test Circuit 1-a

Supply current vs temperature (PST414A290N□)



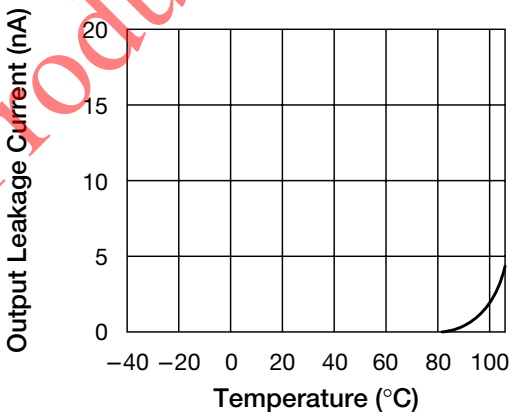
Test Circuit 2

Threshold Operating Voltage Vs temperature



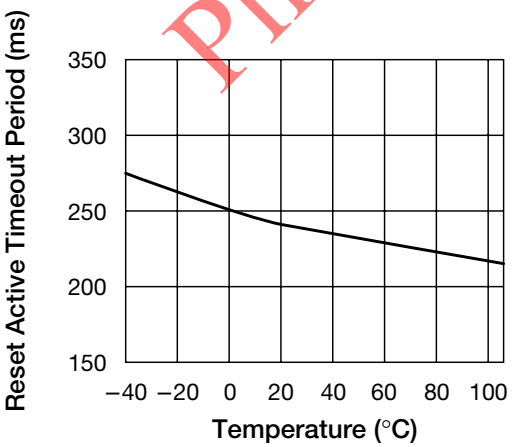
Test Circuit 7

Output leakage current vs temperature



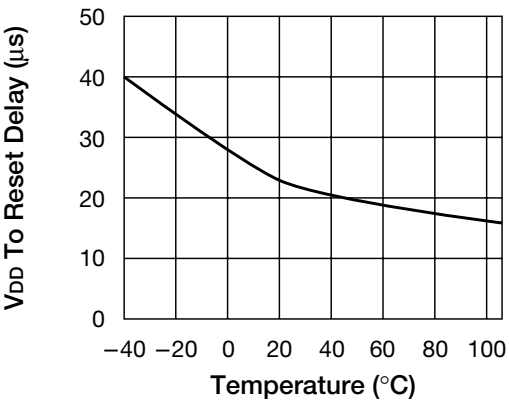
Test Circuit 5

Reset active timeout period vs temperature



Test Circuit 8

VDD to reset delay vs temperature

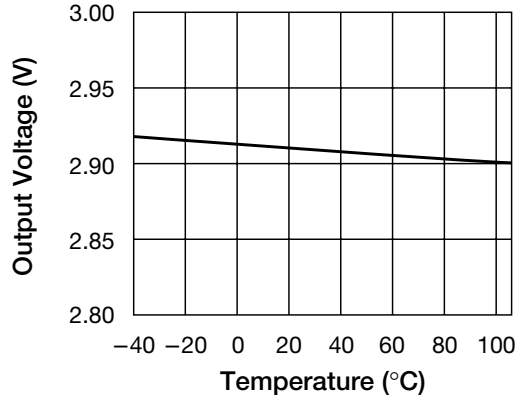


Test Circuit 8

Note: These are typical characteristics.

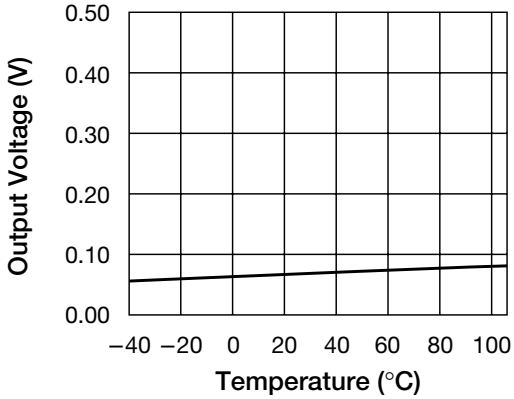
Characteristics

■ "H"Output voltage vs temperature (PST414A290N□)



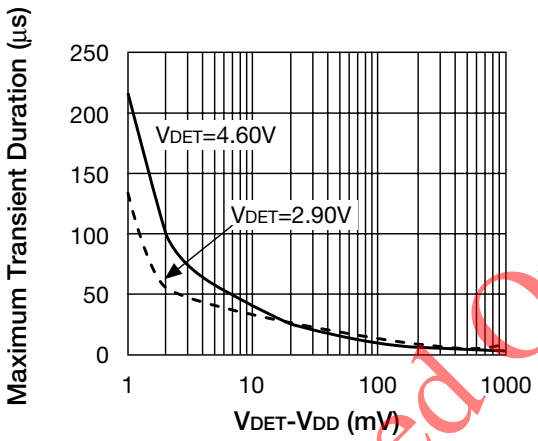
Test Circuit 6

■ "L"Output voltage vs temperature (PST414A290N□)



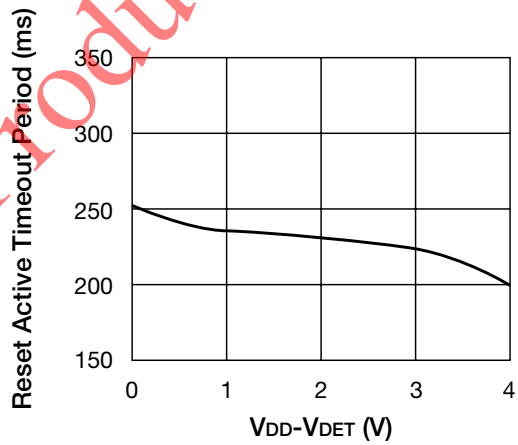
Test Circuit 7

■ Maximum transient duration vs VDET-VDD



Test Circuit 8

■ Reset active timeout period vs VDD-VDET (PST414A290N□)



Test Circuit 8

Note: These are typical characteristics.