

# 4fsc Clock Generator Monolithic IC MM1093

January 28, 1992

## Outline

This IC generates a clock used for driving the CCD that comprises a comb filter required for Y/C separation, or for sampling A/D and D/A converters that comprise a digital comb filter. It has a built-in subcarrier oscillator (3.58MHz or 4.43MHz) synchronized with the input chroma signal, and its monolithic clock oscillator. MM1093ND and -NF are available for NTSC format, and MM1093PD and -PF for PAL format.

## Features

1. Includes an fsc oscillator synchronized to the input chroma signal and 4fsc oscillator
2. Reduces external component count due to 1 pin VCXO
3. +5V single power supply

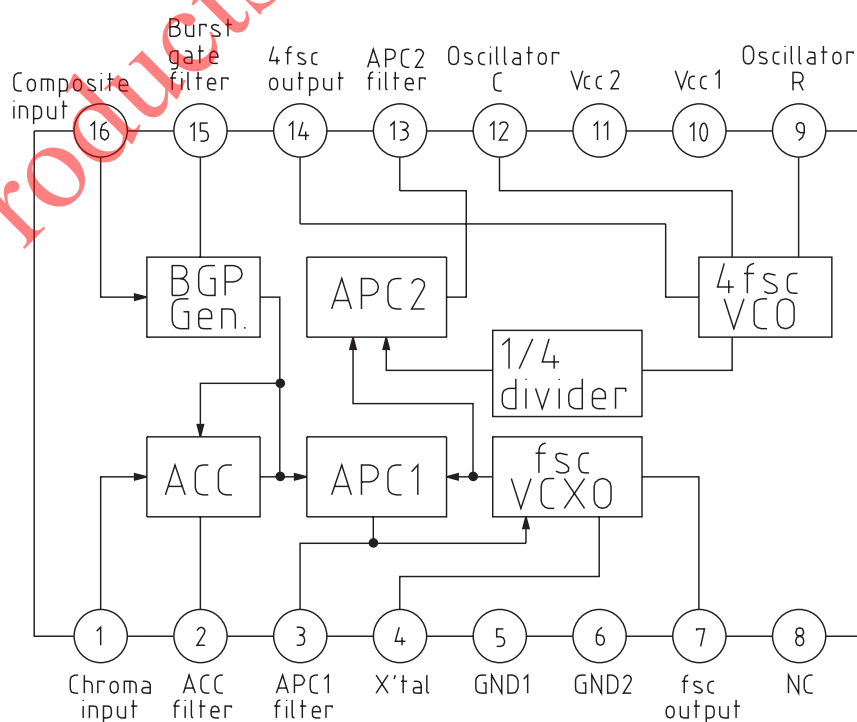
## Package

SOP-16A (MM1093NF, MM1093PF)  
DIP-16B (MM1093ND, MM1093PD)

## Applications

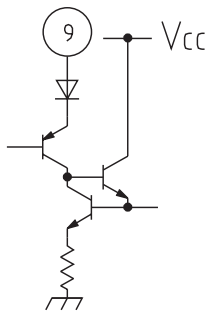
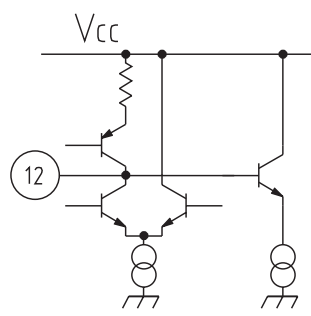
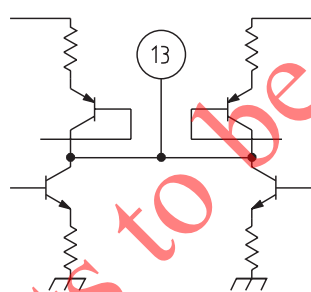
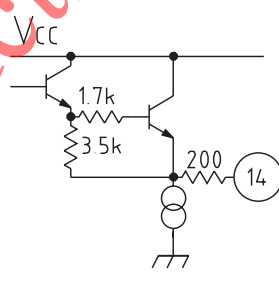
1. TVs
2. VCRs

## Equivalent Circuit Diagram

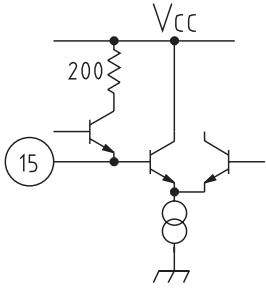
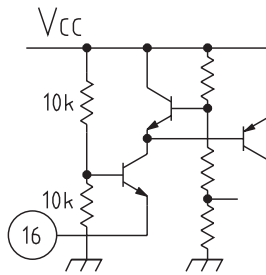


Pin Description

Pin no.	Pin name	Equivalent Circuit Diagram	Pin Description
1	Chroma input		Chroma signal input pin
2	ACC filter		ACC filter pin
3	APC1 filter		fsc APC circuit filter pin
4	X'tal		VCXO circuit X'tal pin
5	GND1		fsc GND pin
6	GND2		4fsc GND pin
7	fsc output		Outputs subcarrier synchronized to input chroma signal NTSC : 3.579545MHz PAL : 4.433619MHz

8	NC		NC pin
9	Oscillator R		Connects to resistor that determines 4fsc VCO free run frequency
10	Vcc1		fsc power supply pin
11	Vcc2		4fsc power supply in
12	Oscillator C		Connects to capacitor that determines 4fsc VCO free run frequency
13	APC2 filter		4fsc APC circuit filter pin
14	4fsc output		Outputs a 4x signal sychronized to input chroma signal.

Products to be discontinued

<p><b>15</b></p>	<p>Burst gate filter</p>		<p>This pin creates burst gate pulse.</p>
<p><b>16</b></p>	<p>Composite input</p>		<p>Composite signal input pin</p>

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub> max.	7	V
Allowable loss	P <sub>d</sub>	350	mW

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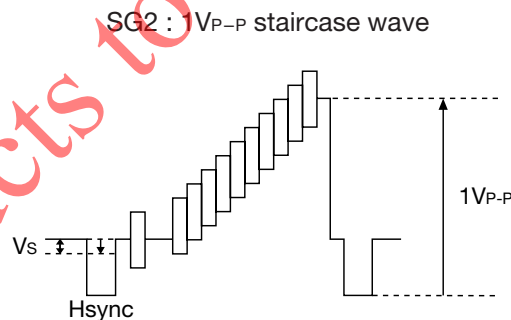
**Electrical Characteristics** (Except where noted otherwise, Ta=25°C, Vcc=5.0V, SG1, SG2 : no signal, SW1 : A)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V <sub>CC</sub>	V <sub>CC</sub>		4.7	5.0	5.3	V
Consumption current	I <sub>CC</sub>	-			24	32	mA
<b>Sync separation circuit</b>							
Sync separation level	V <sub>s</sub>	TP3	SG2 : 1V <sub>P-P</sub> staircase wave *1 SG1 : separate chroma signal SW1 : B *5	40	80	120	mV
<b>PLL circuit</b>							
ACC input amplitude range	V <sub>IN</sub>	TP1	SG1 : separate chroma signal *2 *5	15		560	mV <sub>P-P</sub>
APC1 frequency acquisition range	f <sub>c</sub>	TP2	SG1 : sine wave 143mV <sub>P-P</sub> SG2 : 1V <sub>P-P</sub> staircase wave *3	400			Hz
VCO1 free run frequency deviation	Δf <sub>0</sub>		*4	-250	0	250	Hz
fSC output level	V <sub>O1</sub>	TP2	SG1 : separate chroma signal SG2 : 1V <sub>P-P</sub> staircase wave *5	0.8	1.0	1.2	V <sub>P-P</sub>
fSC output duty	D <sub>O1</sub>		SG1 : separate chroma signal SG2 : 1V <sub>P-P</sub> staircase wave *5	45	50	55	%
<b>4fSC circuit</b>							
4fSC output level	V <sub>O2</sub>	TP3	SG1 : separate chroma signal SG2 : 1V <sub>P-P</sub> staircase wave SW1 : B *5	0.8	1.0	1.2	V <sub>P-P</sub>
4fSC output DT	D <sub>O2</sub>		SG1 : separate chroma signal SG2 : 1V <sub>P-P</sub> staircase wave SW1 : B *5	45	50	55	%
fSC leakage	L <sub>fsc</sub>		SG1 : separate chroma signal SG2 : 1V <sub>P-P</sub> staircase wave SW1 : B *5		50		dB

Notes:

\*1 Sync separation level

Measure the level where SG1 input signal and TP3 output signal synchronize when 1V<sub>P-P</sub> staircase wave sync signal level is raised from 0V.



\*2 ACC input amplitude range

Defined as separate chroma signal burst signal amplitude that can be input to chroma input.

\*3 APC1 frequency pull-in range

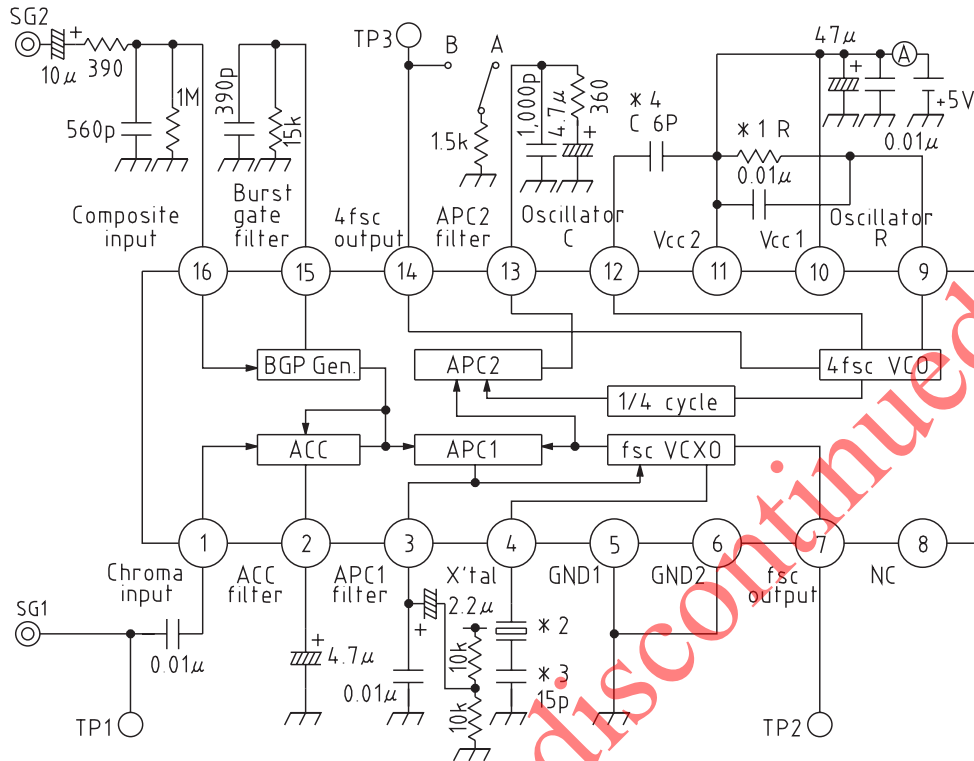
Defined as the smaller of the differences when input signal frequency is changed from high to f<sub>0</sub> and from low to f<sub>0</sub> when TP2 output is not synchronized to SG1 input signal and when it is synchronized.

\*4 VCO1 free run frequency deviation

Defined as the difference between TP2 output signal frequency and f<sub>0</sub>.

\*5 The standard for the separate chroma signal is burst signal 143mV<sub>P-P</sub>.

Measuring Circuit



Notes:

\*1 NTSC : R=5.6k

PAL : 4.3k

\*2 Recommended crystal oscillator

Tokyo Dempa, TR-49 or equivalent

NTSC : 3.579545MHz

PAL : 4.433619MHz

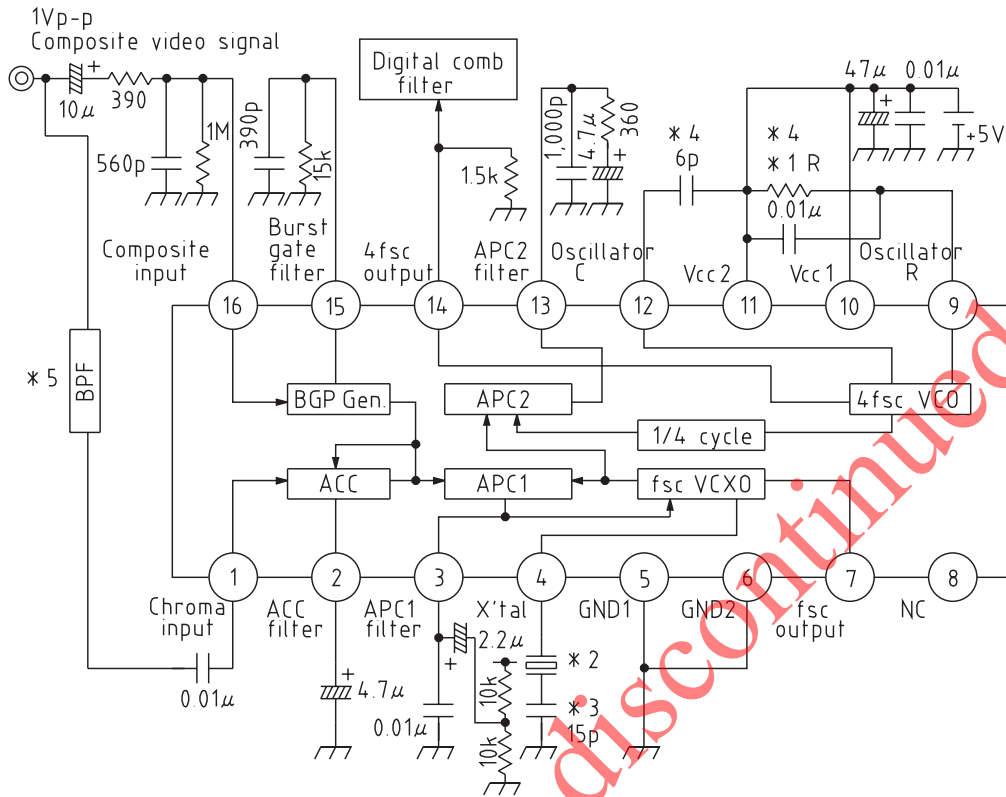
\*3 Use part with precision within  $\pm 5\%$  and temperature characteristic CH.

\*4 R and C change according to board floating capacitance, etc.

Select R and C so that Pin 13 voltage is approximately 2V for VCO lock. Also, C should be 4PF or higher, and R should be 3.3k $\Omega$  or higher.

Product to be discontinued

Application Circuits



Notes:

- \*1 NTSC : R=5.6k  
PAL : R=4.3k
- \*2 Recommended crystal oscillator  
Tokyo Dempa, TR-49 or equivalent  
NTSC : 3.579545MHz  
PAL : 4.433619MHz
- \*3 Use part with precision within  $\pm 5\%$  and temperature characteristic CH.
- \*4 R and C change according to board floating capacitance, etc.  
Select R and C so that Pin 13 voltage is approximately 2V for VCO lock. Also, C should be 4PF or higher, and R should be 3.3k $\Omega$  or higher.
- \*5 BPF Reference circuit

