I²C Bus Controlled 4-Input 1-Output AV Switch
Monolithic IC MM1311

June 17, 1999

Outline

This IC is an I²C bus controlled AV switch IC with 4-input 1-output developed for TVs.

Features

1. Serial control by I²C bus
2. 4 inputs and 1 output
3. Video and audio switches can be controlled independently.
4. Includes a 6dB amp in the video channel
5. Incorporates a Y/C mix circuit
6. Slave address can be changed to 90H or 92H.
7. Enables audio mute with an external pin
8. I²C bus lines (SDA, SCL) maintain high impedance during power-off.
9. Includes a tri-stated detection function
10. Includes a power-on reset function
11. Two types of audio input impedance are available ; 60kΩ and 30kΩ
    MM1311AD : 60kΩ MM1311BD : 30kΩ

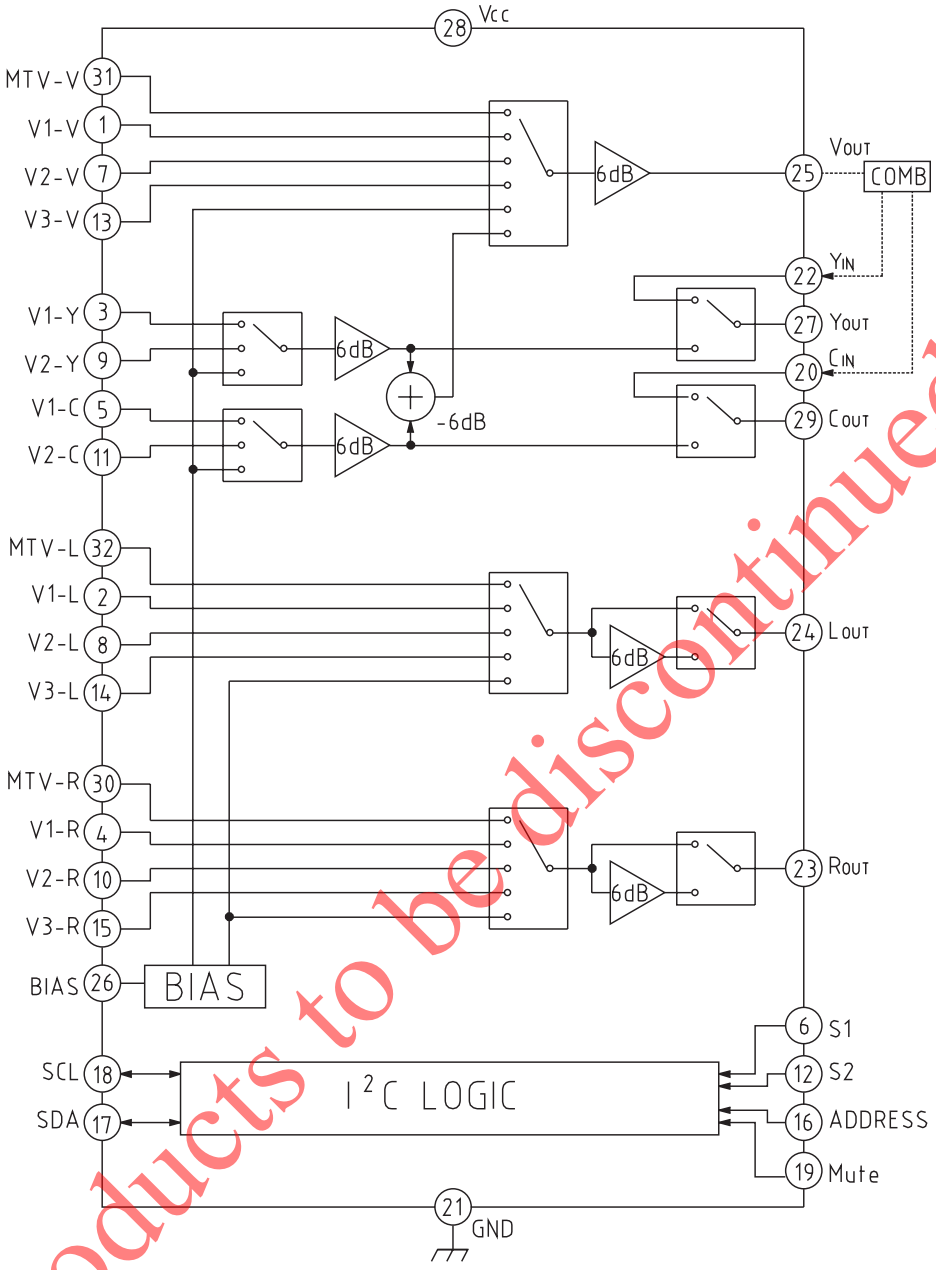
Package

SDIP-32A (MM1311AD, MM1311BD)

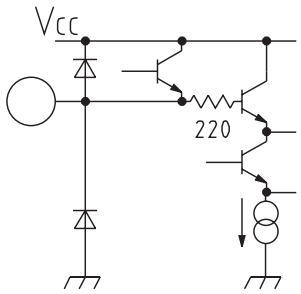
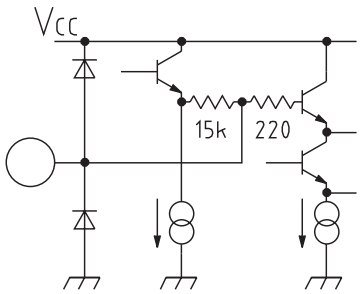
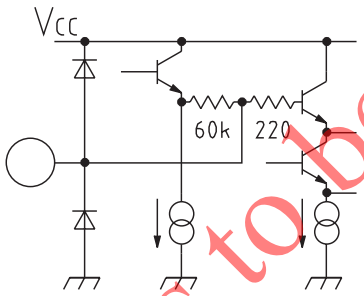
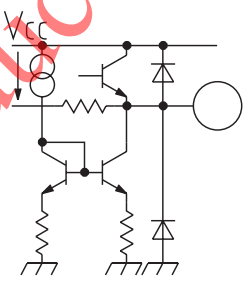
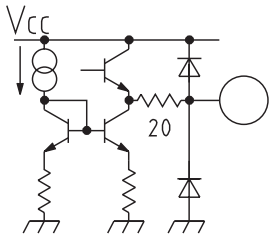
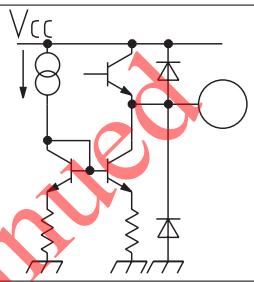
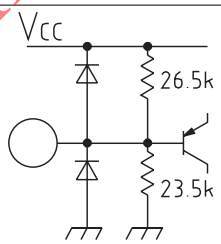
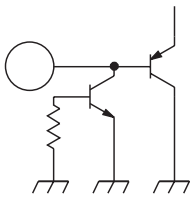
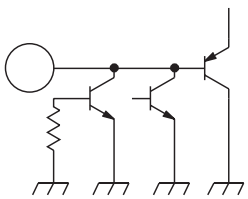
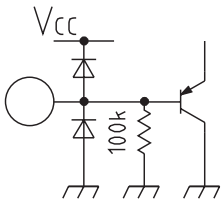
Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram



Pin Description

Pin No.	Name	Internal equivalent circuit diagram
31 1 7 13 3 9 22	MTV–V V1–V V2–V V3–V V1–Y V2–Y YIN	
5 11 20	V1–C V2–C CIN	
32 2 8 14 30 4 10 15	MTV–L V1–L V2–L V3–L MTV–R V1–R V2–R V3–R	
25	VOUT	
27 29	YOUT COUT	
24 23	LOUT ROUT	
26	BIAS	
18	SCL	
17	SDA	
6 12 16 19	S1 S2 ADR Mute	

Absolute Maximum Ratings (Ta=25°C)

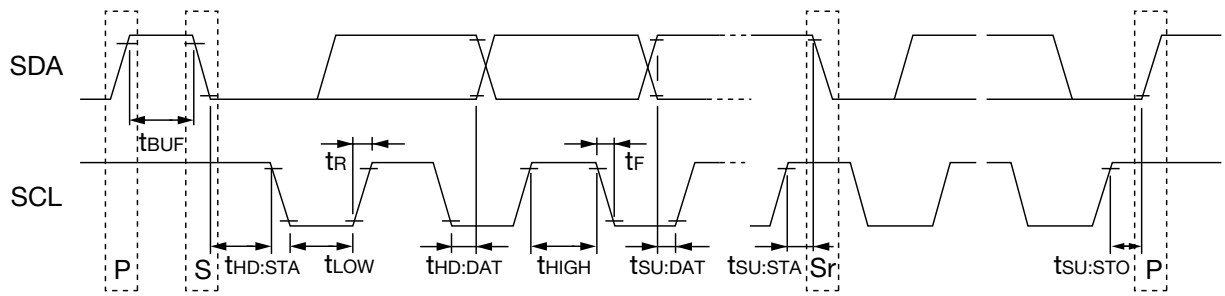
Item	Symbol	Ratings	Units
Storage temperature	TSTG	–40~+125	°C
Operating temperature	TOPR	–20~+75	°C
Power supply voltage	VCC	12	V
Allowable power dissipation	Pd	1500	mW

Electrical Characteristics (Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}			8	9	10	V
Current consumption	I_{CC}	28	V_{CC}=9V, no signal, no load		27	35	mA
V_{OUT} output							
Voltage gain	G_V	TP1	Sine wave, 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_V	TP1	Sine wave, 1.0V_{P-P}, 10MHz/100kHz	–1.0	0	1.0	dB
Differential gain	DG_V	TP1	Vn–V : Staircase, 1V_{P-P} APL=10~90% Vn–Y : Staircase (luminance signal) 1V_{P-P} Vn-C : Chroma signal 0.3V_{P-P} APL=10~90%	–3	0	3	%
Differential phase	DP_V	TP1	Vn–V : Staircase, 1V_{P-P} APL=10~90% Vn–Y : Staircase (luminance signal) 1V_{P-P} Vn–C : Chroma signal 0.3V_{P-P} APL=10~90%	–3	0	3	deg
Input dynamic range	D_{V1}	SG 1~3	Sine wave, 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
Y_{OUT} output							
Voltage gain	G_{Y1}	TP2	Vn–Y : Sine wave, 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{Y2}	TP2	Y_{IN} : Sine wave, 2.0V_{P-P}, 100kHz	–0.5	0	0.5	
Frequency characteristics	F_{Y1}	TP2	Vn–Y : Sine wave, 1.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	dB
	F_{Y2}	TP2	Y_{IN} : Sine wave, 2.0V_{P-P}, 10MHz/100kHz	–1.0	0	1.0	
Differential gain	DG_Y	TP2	Vn–Y : Staircase, 1V_{P-P} APL=10~90% Y_{IN} : Staircase, 2V_{P-P}, APL=10~90%	–3	0	3	%
Differential phase	DP_Y	TP2	Vn–Y : Staircase, 1V_{P-P} APL=10~90% Y_{IN} : Staircase, 2V_{P-P}, APL=10~90%	–3	0	3	deg
Input dynamic range	D_{Y1}	SG2	Vn–Y : Sine wave100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
	D_{Y2}	SG4	Y_{IN} : Sine wave, 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	Z_{OY}				50		Ω
C_{OUT} output							
Voltage gain	G_{C1}	TP3	Vn–C : Sine wave, 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_{C2}	TP3	C_{IN} : Sine wave, 2.0V_{P-P}, 100kHz	–0.5	0	0.5	
Frequency characteristics	F_{C1}	TP3	Vn–C : Sine wave, 1.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	dB
	F_{C2}	TP3	C_{IN} : Sine wave, 2.0V_{P-P}, 10MHz/100kHz	–1.0	0	1.0	
Differential gain	DG_C	TP3	C_{IN} : Staircase, 2V_{P-P}, APL=10~90%	–3	0	3	%
Differential phase	DP_C	TP3	C_{IN} : Staircase, 2V_{P-P}, APL=10~90%	–3	0	3	deg
Input dynamic range	D_{C1}	SG3	Vn–C : Sine wave, 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V_{P-P}
	D_{C2}	SG5	C_{IN} : Sine wave, 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z_{IC}		Vn–C, C_{IN}	10	15	20	kΩ
Output impedance	Z_{OC}				50		Ω
L_{OUT} output							
Voltage gain	G_{L1}	TP4	b7=0, Sine wave, 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_{L2}	TP4	b7=1, Sine wave, 2.5V_{P-P}, 1kHz	–0.5	0	0.5	
Frequency characteristics	F_L	TP4	Sine wave, 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB

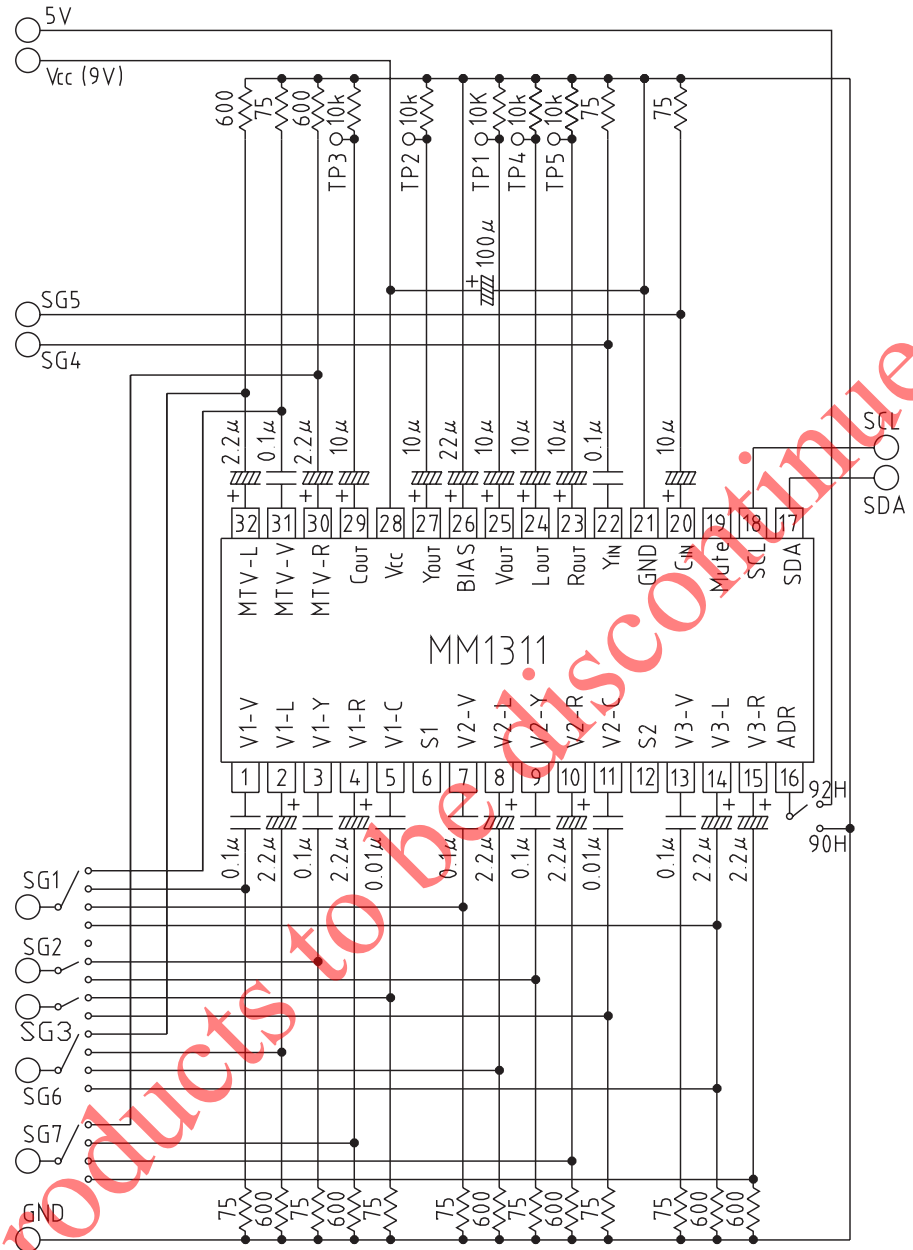
Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Total higher harmonic distortion	THDL	TP4	Sine wave, 2.5VP-P, 1kHz		0.03	0.1	%
Input dynamic range	DL	SG6	Sine wave, 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	VOFFL	24	LOUT pin DC difference during SW switching		0	±15	mV
Input impedance	ZIL			42	60	78	kΩ
Output impedance	ZOL				120		Ω
ROUT output							
Voltage gain	GR1	TP5	b7=0, Sine wave, 2.5VP-P, 1kHz	–6.5	–6.0	–5.5	dB
	GR2	TP5	b7=1, Sine wave, 2.5VP-P, 1kHz	–0.5	0	–0.5	
Frequency characteristics	FR	TP5	Sine wave, 2.5VP-P, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THDR	TP5	Sine wave, 2.5VP-P, 1kHz		0.03	0.1	%
Input dynamic range	DR	SG7	Sine wave, 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	VOFFR	23	ROUT pin DC difference during switching		0	±15	mV
Input impedance	ZIR			42	60	78	kΩ
Output impedance	ZOR				120		Ω
Crosstalk							
VOUT	CTV	TP1	Measurement Circuit Figure 2		–60	–53	dB
YOUT	CTY	TP2	SG1 input : 4.43MHz, 1VP-P		–60	–53	dB
COUT	CTC	TP3	SG2 input : 4.43MHz, 0.5VP-P		–60	–53	dB
LOUT	CTL	TP4	Measurement Circuit Figure 2		–90	–80	dB
ROUT	CTR	TP5	1kHz, 2.5VP-P		–90	–80	dB
Video I/O Pin Voltage							
Input pin voltage	VVIP		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	VVOP		VOUT pin, No signal, no load	4.1	4.4	4.7	V
	VSOP		YOUT pin, COUT pin, No signal, no load	3.3	3.6	3.9	V
Audio I/O Pin Voltage							
Input pin voltage	VAIP		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	VAOP		No signal, no load	3.9	4.2	4.5	V
Logic section (Refer to figure below)							
Input voltage L	VIL		I²C logic low level discrimination value	0.0		1.5	V
Input voltage H	VIH		I²C logic high level discrimination value	3.0		5.0	V
Low level output voltage (SDA)	VOL		SDA for 3mA inflow	0.0		0.4	V
High level input current	IIH		when SDA, SCL=4.5V impressed	–10		+10	µA
Low level input current	IIL		when SDA, SCL=0.4V impressed	–10		+10	µA
Clock frequency	fSCL					100	kHz
Data transmission waiting time	tBUF			4.7			µs
SCL start hold time	tHD : STA			4.0			µs
SCL low level hold time	tLOW			4.7			µs
SCL high level hold time	tHIGH			4.0			µs
SCL start set-up time	tSU : STA			4.7			µs
SDA data hold time	tHD : DAT			200			ns
SDA data set-up time	tSU : DAT			250			ns
SCL rise time	tR					1000	ns
SCL fall time	tF					300	ns
SCL stop set-up time	tSU : STO			4.0			µs

I²C BUS Control Signal

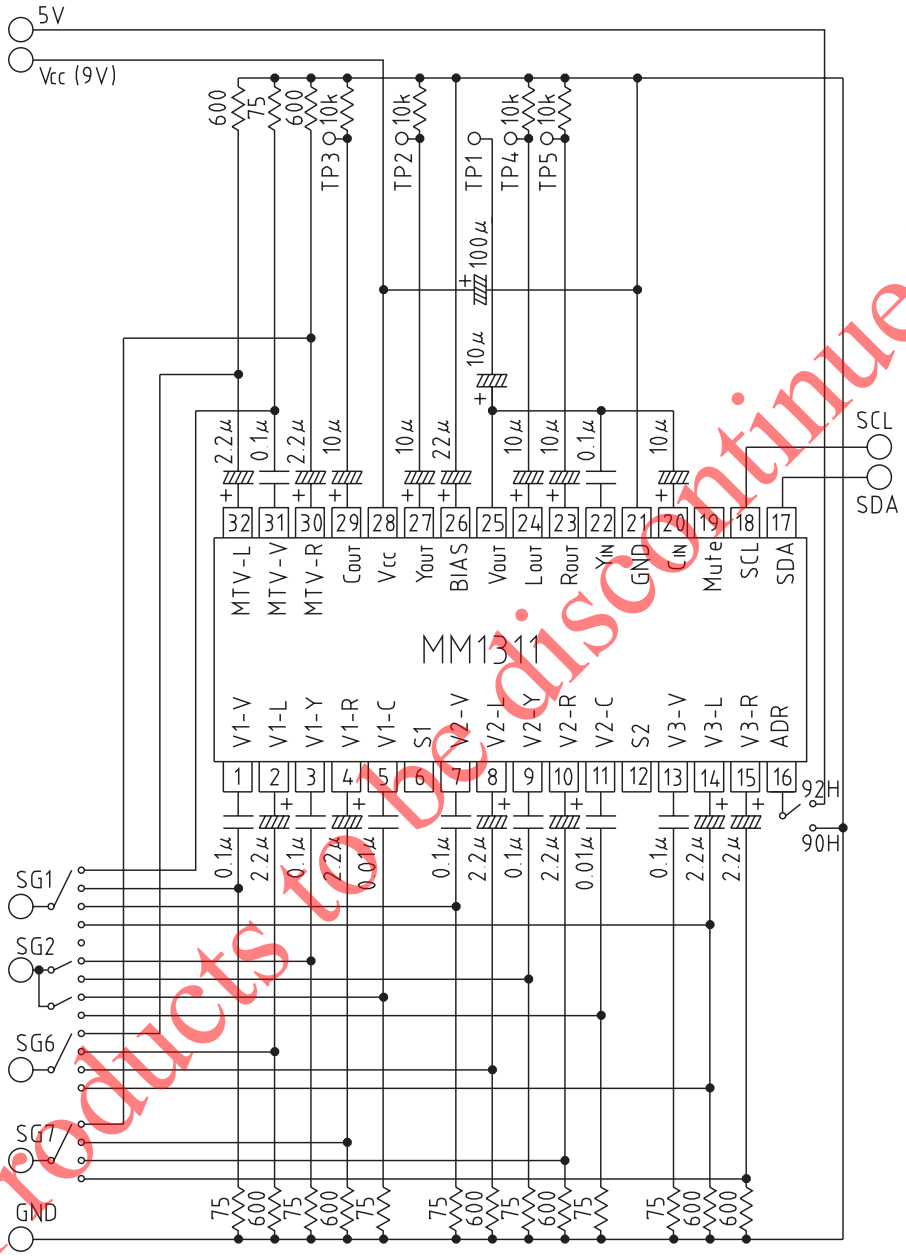


Measurement Circuit

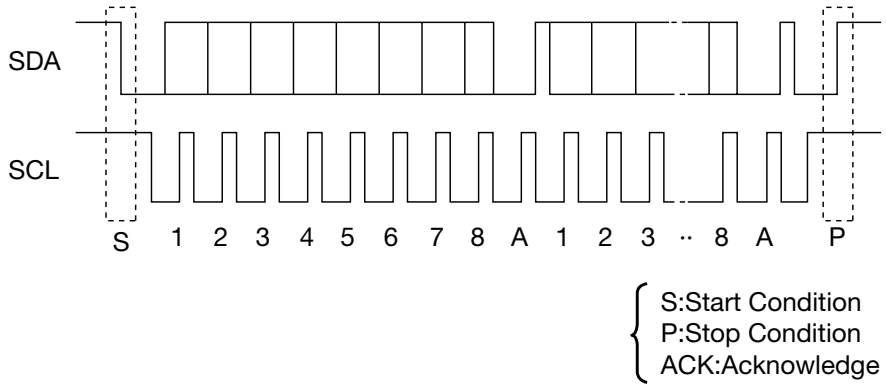
Measurement Circuit 1



Measurement Circuit 2 (Crosstalk measurement)



I²C BUS



The I²C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

Control Register

The control register contains data sent from the master in order to determine the status of each switch.

S	Slave address							R/W	A	Control register								A	P
	1	0	0	1	0	0	0/1	0		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Control data									

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.

The MM1311 slave address can be selected as 90H/92H depending on the status of the ADR pin. When the ADR pin is low it is 90H. The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio Gain	S/Comp Select	Video–Select			Audio–Select		

The control register bits are reset to 0 when power is applied.

MM1311 control is carried out by the 2-byte structure of the 1 address byte and 1 control data byte. All of the remaining data (third byte and after) are ignored.

Refer to the separate tables for details on switch control.

Status Register

The status register contains data for sending device status to the master.

S	Slave address							R/W	A	Control register								NA	P
	1	0	0	1	0	0	0/1	1		b7	b6	b5	b4	b3	b2	b1	b0		
	Address byte									Control data									

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1311 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge. The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.
S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open
S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

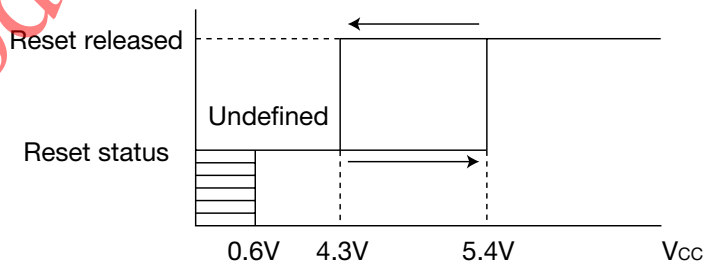
S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

Power On Reset

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.



Switch Control Table

1. Video Output

b6	b5	b4	b3	VOUT	YOUT	COUT
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV–V	YIN	CIN
0	0	1	0	V1–V	YIN	CIN
0	0	1	1	V2–V	YIN	CIN
0	1	0	0	V3–V	YIN	CIN
0	1	0 ~ 1	1 ~ 1	Mute	Mute	Mute
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV–V	YIN	CIN
1	0	1	0	V1–Y+C	V1–Y	V1–C
1	0	1	1	V2–Y+C	V2–Y	V2–C
1	1	0	0	V3–V	YIN	CIN
1	1	0 ~ 1	1 ~ 1	Mute	Mute	Mute

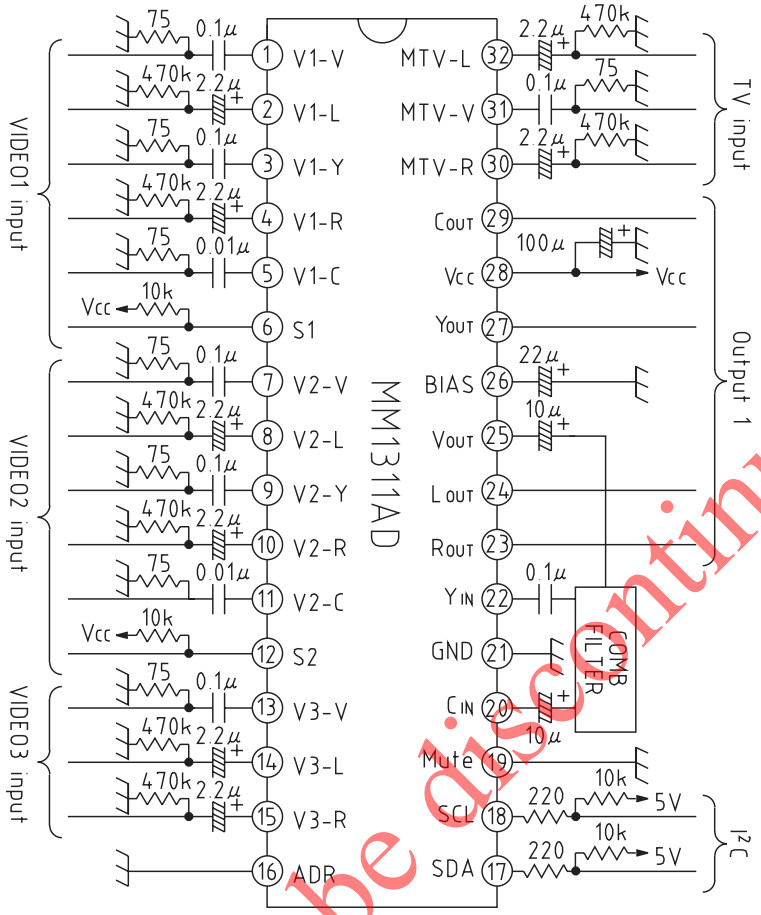
2. Audio Output

Mute pin	b2	b1	b0	LOUT	ROUT
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0 ~ 1	1 ~ 1	Mute	Mute
3.0V or more	—	—	—	Mute	Mute

3. Audio Gain Switching

b7	Output gain
0	–6dB output
1	0dB output

Example of Application Circuit



Notes 1 : V_{OUT} is set at 4.4V and C_{IN} at 4.3V.
Please note that capacitance polarity may vary depending on comb filter bias.

Notes 2 : Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.