Component Input Video Swich with I²C Bus
Monolithic IC MM1519

February 21, 2000

Outline

This IC is a color difference input video switch IC with I²C bus control developed for high-resolution TVs. It can support PIP TVs, monitor output, decoder output, etc. as it provides 3 outputs.

Features

1. Serial control by I²C bus
2. 4 color difference inputs and 3 outputs (3 inputs comply with the D-pin standard)
3. Includes a 6dB amp
4. Slave address can be changed to 94H or 96H.
5. High-band video SW supporting D4 input (Y: 50MHz/P_B, P_R: 25MHz)
6. The OUT2 and OUT3 pins have a power-save function.
7. Includes one output chennnel which can be controlled by I²C bus (optional)

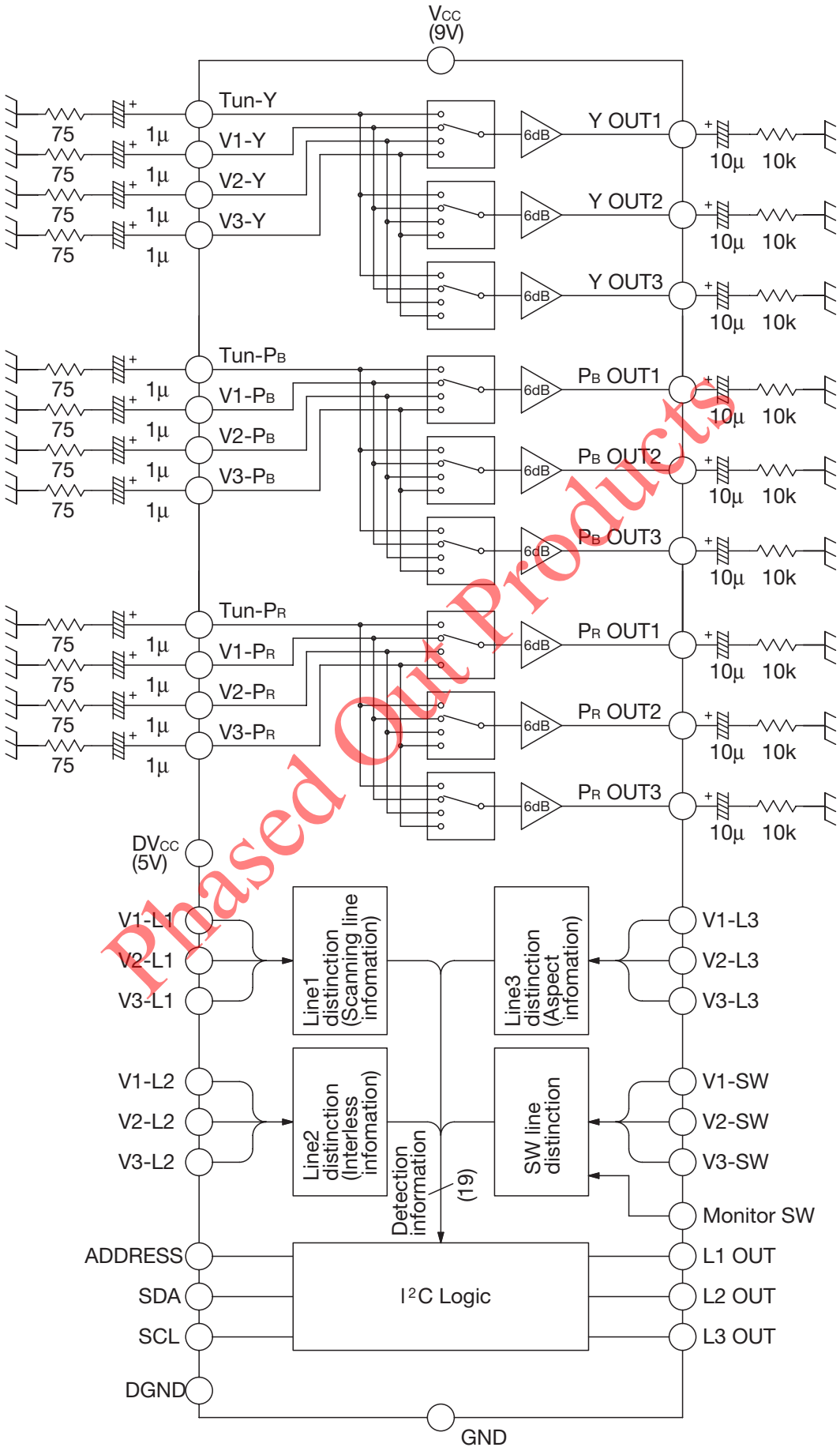
Package

QFP-64B

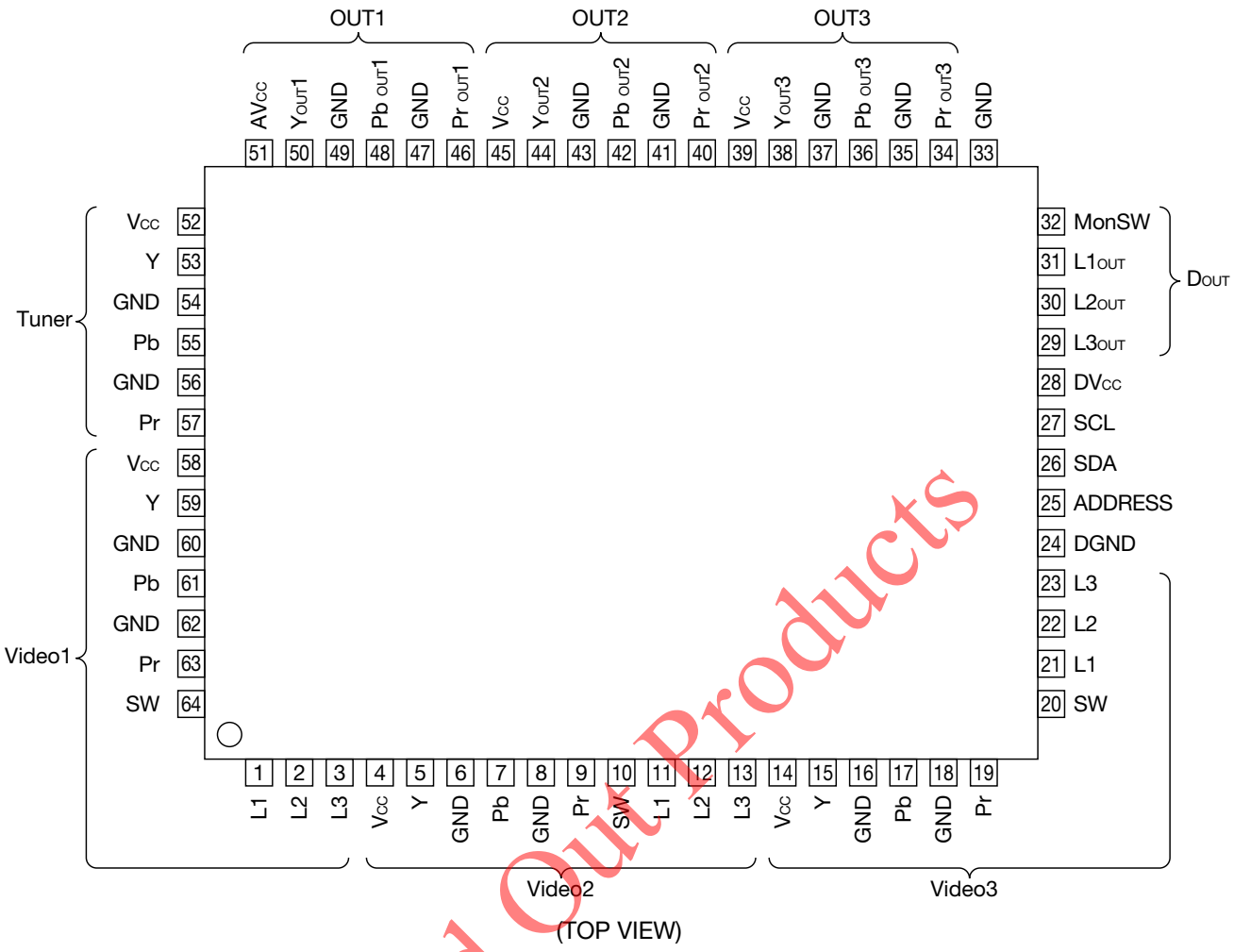
Applications

1. HDTVs
2. SDTVs
3. Other video equipment

Block Diagram

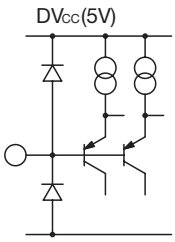
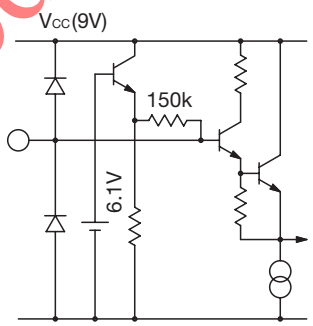


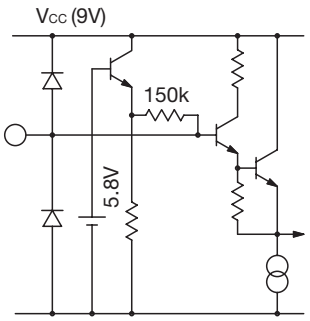
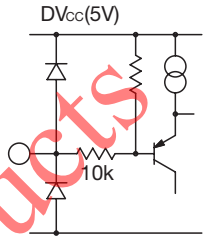
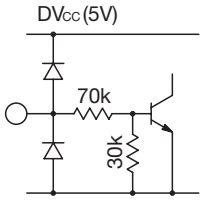
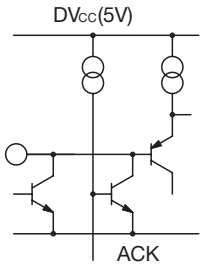
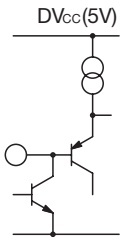
Pin Assignment

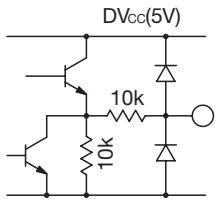
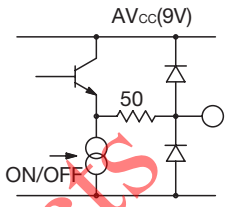


(TOP VIEW)

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 2 3 11 12 13 21 22 23	Video1-L1 Video1-L2 Video1-L3 Video2-L1 Video2-L2 Video2-L3 Video3-L1 Video3-L2 Video3-L3	Line input of D-terminal	
4 14 39 45 51 52 58	Vcc AVcc	Analog Vcc	
5 15 53 59	Video2-Y Video3-Y Tuner-Y Video1-Y	Y input	
6 8 16 18 24 33 35 37 41 43 47 49 54 56 60 62	GND DGND	GND	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7 9 17 19 55 57 61 63	Video2-Pb Video2-Pr Video3-Pb Video3-Pr Tuner-Pb Tuner-Pr Video1-Pb Video1-Pr	Pb,Pr input	
10 20 32 64	Video2-SW Video3-SW MonSW Video1-SW	SW-Line of D terminal	
25	ADDRESS	Slave Address select pin	
26	SDA	Data input of I²C BUS	
27	SCL	CLK input of I²C BUS	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
28	DVcc	Digital Vcc	
29 30 31	L3out L2out L1out	Line output for Monitor	
34 36 38 40 42 44 46 48 50	Pr out3 Pb out3 Y out3 Pr out2 Pb out2 Y out2 Pr out1 Pb out1 Y out1	Video output	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temparature	Tstg	–40~+125	°C
Operating temparature	Topr	–20~+75	°C
Supply voltage	Vcc max.	13	V
Power dissipation	Pd	1300	mW

Recommended Operating Conditions

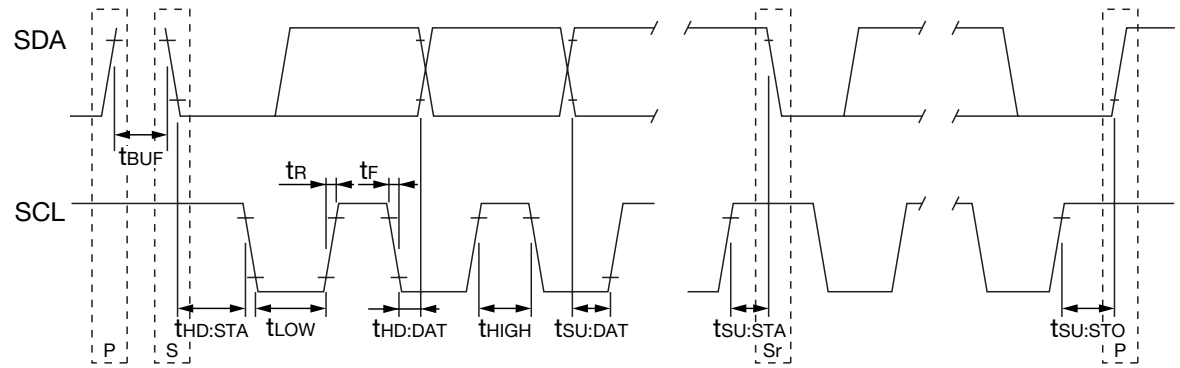
Item	Symbol	Ratings	Units
Operating temparature	Topr	–20~+75	°C
Operating voltage	Vop1	+8.0~+10.0	V
Operating voltage	Vop2	+4.5~+5.5	V

Electrical Characteristics (Except where noted therwise, Ta=25°C, Vcc=AVcc=9V, DVcc=5V)

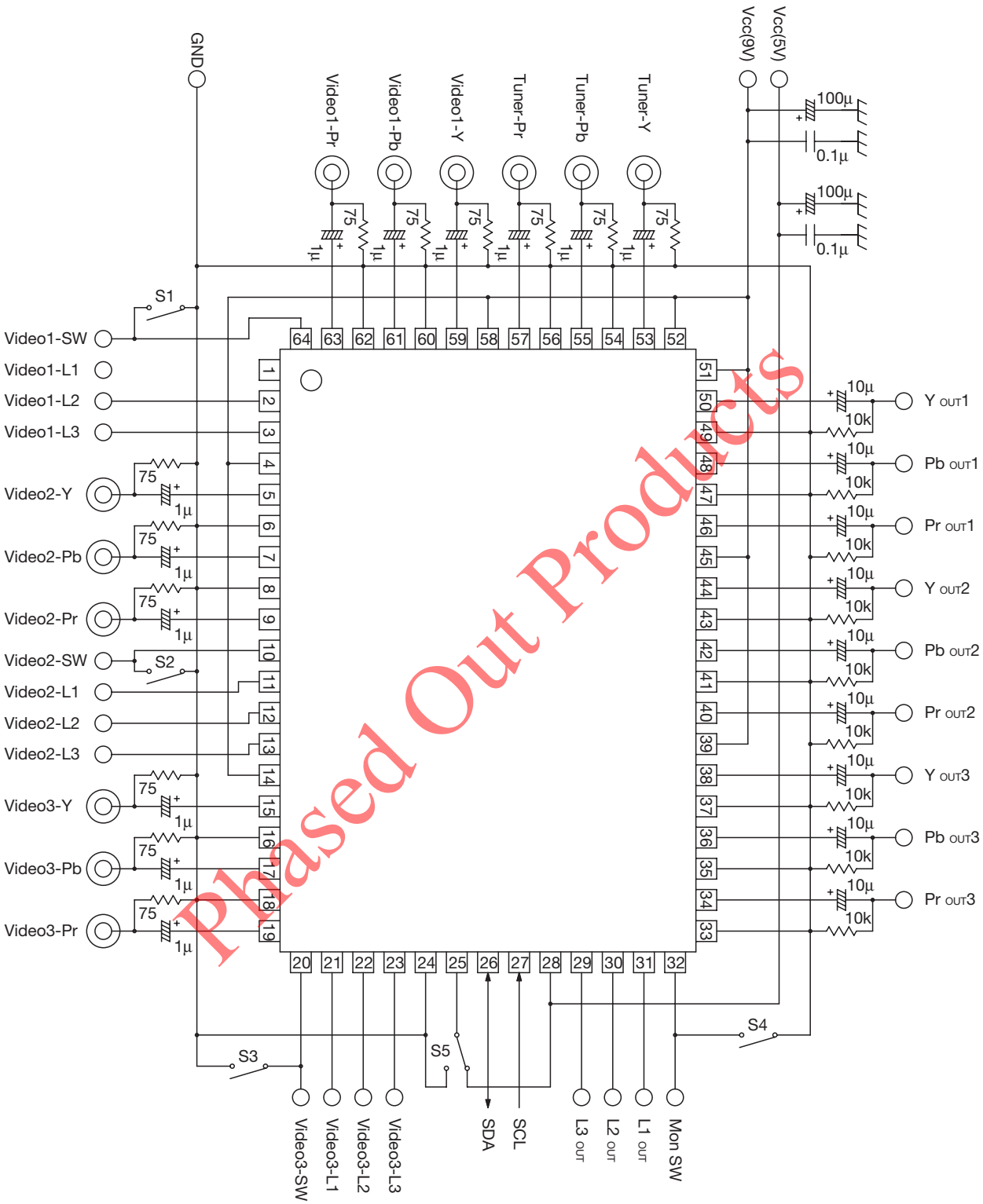
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[Vcc & AVcc] (Analog Vcc [9V])						
Current consumption	Icc0	No signal		67	87	mA
Current of power-save 1	Icc1	Out2 is turn–off, Out1&3 are active		55	72	mA
Current of power-save 2	Icc2	Out3 is turn–off, Out1&2 are active		55	72	mA
Current of power-save 3	Icc3	Out2&3 are turn–off, Out1 is active		43	60	mA
[DVcc] (Digital Vcc [5V])						
Current consumption	Icc4	No signal		8	10	mA
[Terminal voltage]						
Y input terminal	VYIN	53, 59, 5, 15 pin	4.8	5.2	5.6	V
Pb,Pr input terminal	VPIN	55, 57, 61, 63, 7, 9, 17, 19 pin	4.5	4.9	5.3	V
Y output terminal	VYOUT	50, 44, 38 pin	4.0	4.4	4.8	V
Pb, Pr output terminal	VPOUT	48, 46, 42, 40, 36, 34 pin	3.9	4.3	4.7	V
[D connecter conditions]						
Line1~3 detect level L	VdetL	1, 2, 3, 11, 12, 13, 21, 22, 23 pin	0.6	1.0	1.4	V
Line1~3 detect level H	VdetH	1, 2, 3, 11, 12, 13, 21, 22, 23 pin	2.4	2.9	3.4	V
Switch detect level L	VdetL	64, 10, 20, 32 pin			1.8	V
Switch detect level H	VdetH	64, 10, 20, 32 pin	3.5			V
Line output level L	VLL				0.4	V
Line output level M	VLM		1.4		2.4	V
Line output level H	VLH		3.4			V
[Address terminal]						
Address threshold level	VthADR		1.5	2.0	2.5	V
[Input terminal impedance]						
Y input	RYIN		100	150	200	kΩ
Pb input	RPBIN		100	150	200	kΩ
Pr input	RPBIN		100	150	200	kΩ
[YOUT1]						
Voltage gain	GY1	SIN wave: 1VP-P, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	fY1	SIN wave: 1VP-P 50MHz/100kHz	–3			dB
Input dynamic range	DY1	SIN wave: 100kHz THD=1.0%	2.5	3.0		VP-P
[YOUT2]						
Voltage gain	GY2	SIN wave: 1VP-P, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	fY1	SIN wave: 1VP-P 50MHz/100kHz	–3			dB
Input dynamic range	DY2	SIN wave: 100kHz THD=1.0%	2.5	3.0		VP-P
[YOUT3]						
Voltage gain	GY3	SIN wave: 1VP-P, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	fY1	SIN wave: 1VP-P 50MHz/100kHz	–3			dB
Input dynamic range	DY3	SIN wave: 100kHz THD=1.0%	2.5	3.0		VP-P
[Pb OUT1]						
Voltage gain	GPB1	SIN wave: 1VP-P, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	fY1	SIN wave: 1VP-P 25MHz/100kHz	–3			dB
Input dynamic range	DPB1	SIN wave: 100kHz THD=1.0%	2.5	3.0		VP-P
[Pb OUT2]						
Voltage gain	GPB2	SIN wave: 1VP-P, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	fY1	SIN wave: 1VP-P 25MHz/100kHz	–3			dB
Input dynamic range	DPB2	SIN wave: 100kHz THD=1.0%	2.5	3.0		VP-P

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[Pb OUT3]						
Voltage gain	G_{PB3}	SIN wave: 1V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f_{Y1}	SIN wave: 1V_{P-P} 25MHz/100kHz	–3			dB
Input dynamic range	D_{PB3}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V_{P-P}
[Pr OUT1]						
Voltage gain	G_{PR1}	SIN wave: 1V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f_{Y1}	SIN wave: 1V_{P-P} 25MHz/100kHz	–3			dB
Input dynamic range	D_{PR1}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V_{P-P}
[Pr OUT2]						
Voltage gain	G_{PR2}	SIN wave: 1V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f_{Y1}	SIN wave: 1V_{P-P} 25MHz/100kHz	–3			dB
Input dynamic range	D_{PR2}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V_{P-P}
[Pr OUT3]						
Voltage gain	G_{PR3}	SIN wave: 1V_{P-P}, 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f_{Y1}	SIN wave: 1V_{P-P} 25MHz/100kHz	–3			dB
Input dynamic range	D_{PR3}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V_{P-P}
[Crosstalk]						
YOUT1	CT_{Y1L}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
YOUT2	CT_{Y2L}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
YOUT3	CT_{Y3L}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pb OUT1	CT_{PB1}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pb OUT2	CT_{PB2}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pb OUT3	CT_{PB3}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pr OUT1	CT_{PR1}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pr OUT2	CT_{PR2}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
Pr OUT3	CT_{PR3}	SIN wave: 1V_{P-P}, 5MHz		–65	–55	dB
[I²C condition]						
Input voltage L	V_{IL}		0		1.5	V
Input voltage H	V_{IH}		3.0		5.0	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
Start condition setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		200			ns
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA, SCL rise time	t_R				1000	ns
SDA, SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			µs

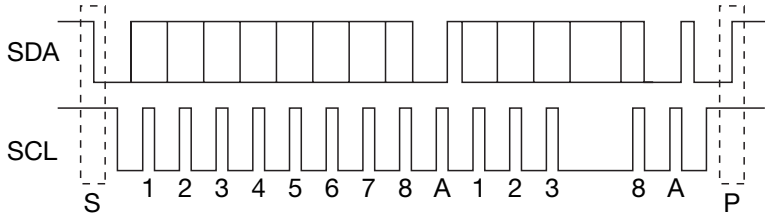
Note.1 I²C condition



Measuring Circuit



I²C BUS



I²C BUS is inter bus system controled by 2 lines (SDA,SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the Start conditions.

[Control registers]
Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.

S	Slave address							R/W	A	DATA1								A	DATA2								A	P
	1	0	0	1	0	1	0/1	0		b07	b06	b05	b04	b03	b02	b01	b00		b27	b26	b25	b24	b23	b22	b21	b20		

Address byte　　Data byte

Out of the Address byte, first 7bit are assigned to the slave address,while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1519 slave address, either 94H or 96H can be selected according to the ADR terminal conditions.
When ADR terminal is L,94H is selected.
The following figure indicates the control contents of control registers and switches.
Each bit of control registers is reset to 0,when power-on.

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	Power save 2	Power save 3	Out1 select		Out2 select		Out3 select	
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
	Line1 output			Line2 output		Line3 output		
	1080	720	480	60p	60i	16 : 9	Letter Box	4 : 3

MM1519 consists of one address byte and two control data bytes (3bytes in total).
All data over the limited length (4th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the another table.

Switch Control Table

Out1 select

b05	b04	YOUT1	Pb OUT1	Pr OUT1
0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
0	1	Video1-Y	Video1-Pb	Video1-Pr
1	0	Video2-Y	Video2-Pb	Video2-Pr
1	1	Video3-Y	Video3-Pb	Video3-Pr

Out2 select

b07	b03	b02	YOUT2	Pb OUT2	Pr OUT2
0	0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
	0	1	Video1-Y	Video1-Pb	Video1-Pr
	1	0	Video2-Y	Video2-Pb	Video2-Pr
	1	1	Video3-Y	Video3-Pb	Video3-Pr
1			OFF	OFF	OFF

Out3 select

b06	b01	b00	YOUT3	Pb OUT3	Pr OUT3
0	0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
	0	1	Video1-Y	Video1-Pb	Video1-Pr
	1	0	Video2-Y	Video2-Pb	Video2-Pr
	1	1	Video3-Y	Video3-Pb	Video3-Pr
1			OFF	OFF	OFF

Line1 output

b17	b16	b15	L1OUT
0	0	0	0V
0	0	1	0V
0	1	0	2.2V
0	1	1	0V
1	0	0	5V
1	0	1	0V
1	1	0	0V
1	1	1	0V

Line2 output

b14	b13	L2OUT
0	0	0V
0	1	0V
1	0	5V
1	1	0V

Line3 output

b12	b11	b10	L1OUT
0	0	0	0V
0	0	1	0V
0	1	0	2.2V
0	1	1	0V
1	0	0	5V
1	0	1	0V
1	1	0	0V
1	1	1	0V

[Status registers]

Status registers are data to inform the master of the device status.
The data format is set as shown in the following figure.

S	Slave address						R/W	A
	1	0	0	1	0	1	0/1	1

Address byte

DATA4								A	DATA5								A
b27	b26	b25	b24	b23	b22	b21	b20		b37	b36	b35	b34	b33	b32	b31	b30	

DATA5								A	DATA6								A	P
b47	b46	b45	b44	b43	b42	b41	b40		b57	b56	b55	b54	b53	b52	b51	b50		

Status byte

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers.
As MM1519 slave address, either 95H or 97H can be selected according to the ADR terminal conditions.
When ADR terminal is L,95H is selected.
Set the confirmation acknowledgement after the end of status register to non-ACK.
The following figure shows the correspondence of the output data of status registers.

No.	DATA condition							
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	Line1 (Out1)			Line2 (Out1)		Line3 (Out1)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA4	b37	b36	b35	b34	b33	b32	b31	b30
	Line1 (Out2)			Line2 (Out2)		Line3 (Out2)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA5	b47	b46	b45	b44	b43	b42	b41	b40
	Line1 (Out3)			Line2 (Out3)		Line3 (Out3)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA6	b57	b56	b55	b54	b53	b52	b51	b50
					Switch line detect			
					Video1	Video2	Video3	Mon SW

L1 voltage	Scanning line		
	1080	720	480
DC ≦ 0.8V	0	0	1
1.4V ≦ DC ≦ 2.4V	0	1	0
3.5V ≦ DC ≦ 5.0V	1	0	0

L2 voltage	I/P	
	60p	60i
DC ≦ 2.4V	0	1
3.5V ≦ DC ≦ 5.0V	1	0

L3 voltage	Aspect		
	16 : 9	Letter box	4 : 3
DC ≦ 0.8V	0	0	1
1.4V ≦ DC ≦ 2.4V	0	1	0
3.5V ≦ DC ≦ 5.0V	1	0	0

SW voltage	Switch line
DC ≦ 1.8V (connected)	0
3.2V ≦ DC (unconnected)	1

Application Circuit