

I²C Bus Control Broadband Video Switch

Monolithic IC MM1630

Outline

This is a video switch IC with I²C bus control developed for high-resolution TVs, PDP and projection TVs. It can switch 4 color difference signal lines (component signals), 5 S-video signal lines and 8 composite signal lines.

Design of the input switch block can be simplified by using this IC with MM1631 (audio switch IC).

Features

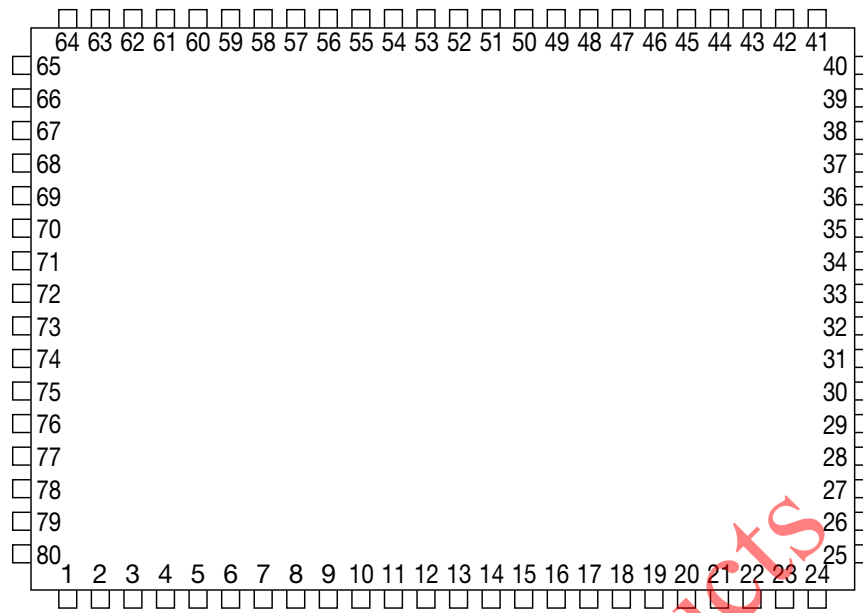
1. Supports component signals (enables 4-input switching and 5-input S-video signal switching) frequency response: 50MHz
2. Enables 8-input switching of component signals
3. Serial control by I²C bus
4. Includes a 0dB/6dB switching amp (OUT1/OUT2/OUT4)
5. Includes a filter (13.5MHz LPF) (slew selection possible)
6. Includes D-pin detection and S-pin detection functions
7. The V_{out3}, Y_{out3}, and C_{out3} pins support 75Ω drive.

Package

QFP-80D

Phased Out Products

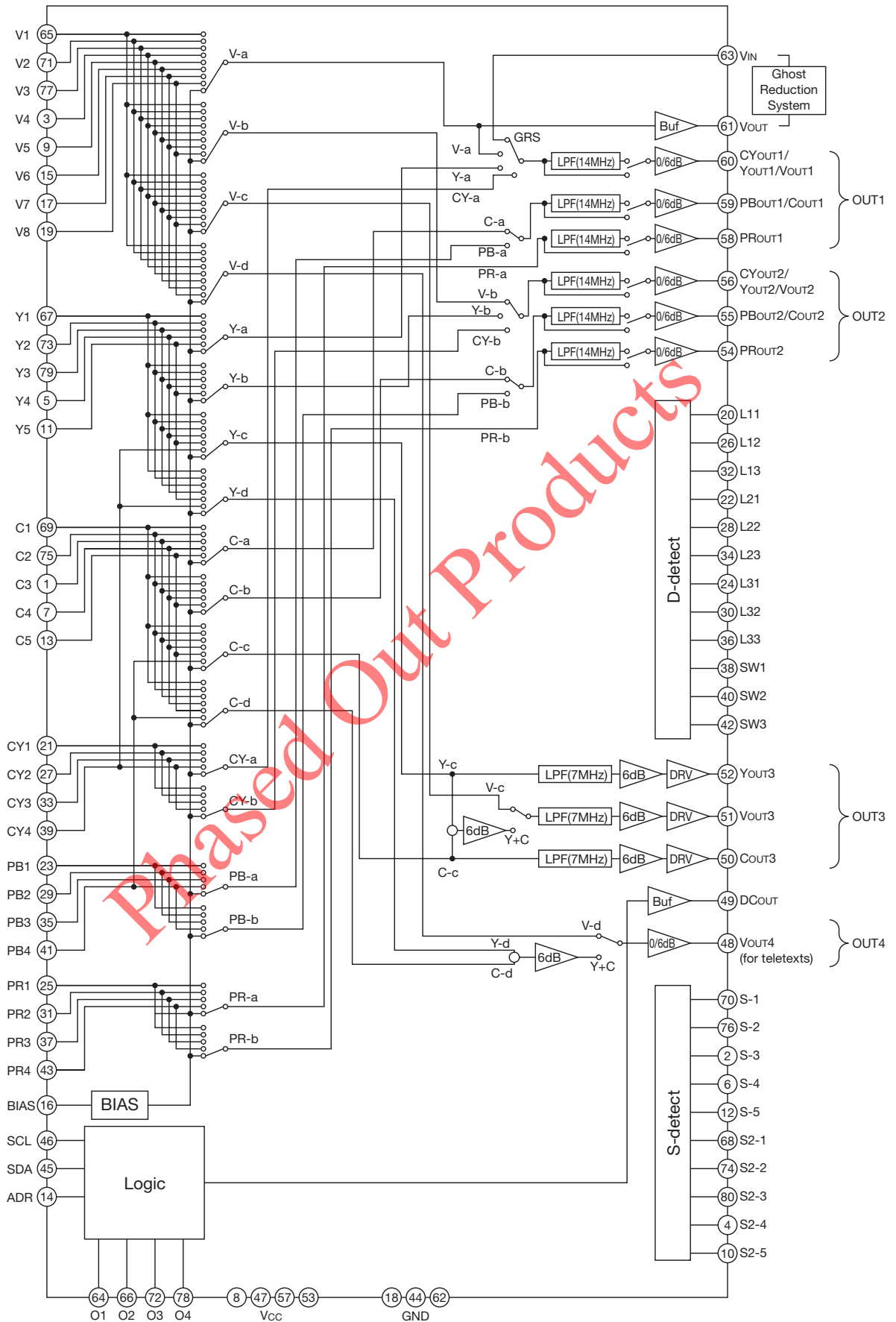
Pin Assignment



QFP-80D
(TOP VIEW)

1	C3	17	V7	33	CY3	49	DCOUT	65	V1
2	S3	18	GND	34	L23	50	COUT3	66	O2
3	V4	19	V8	35	PB3	51	VOU3	67	Y1
4	S2-4	20	L11	36	L33	52	YOU3	68	S2-1
5	Y4	21	CY1	37	PR3	53	VCC	69	C1
6	S4	22	L21	38	SW1	54	PROUT2	70	S-1
7	C4	23	PB1	39	CY4	55	PBOU2/COU2	71	V2
8	VCC	24	L31	40	SW2	56	CYOU2/YOU2/VOU2	72	O3
9	V5	25	PR1	41	PB4	57	VCC	73	Y2
10	S2-5	26	L12	42	SW3	58	PROUT1	74	S2-2
11	Y5	27	CY2	43	PR4	59	PBOU1/COU1	75	C2
12	S5	28	L22	44	GND	60	CYOU1/YOU1/VOU1	76	S-2
13	C5	29	PB2	45	SDA	61	VOU	77	V3
14	ADR	30	L32	46	SCL	62	GND	78	O4
15	V6	31	PR2	47	VCC	63	VIN	79	Y3
16	BIAS	32	L13	48	VOU4	64	O1	80	S2-3

Block Diagram



Note: Only OUT3 can correspond to 75Ω drive.

Pin Description

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
1 7 13 69 75	C3 C4 C5 C1 C2	Croma signal input	
2 6 12 70 76	S-3 S-4 S-5 S-1 S-2	SW of S connector	
3 9 15 17 19 63 65 71 77	V4 V5 V6 V7 V8 V _{IN} V1 V2 V3	Composite signal input	
4 10 68 74 80	S2-4 S2-5 S2-1 S2-2 S2-3	Detect of S connector	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
5 11 67 73 79	Y4 Y5 Y1 Y2 Y3	Luminance signal input	
8 47 53 57	Vcc	Vcc	
14	ADR	Slave address select PIN	
16	BIAS	Bias	
18 44 62	GND	GND	
20 26 32	L11 L12 L13	Detect of D connector scanning line	

Phased Out Products

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
21 27 33 39	CY1 CY2 CY3 CY4	Color difference signal input	
22 28 34	L21 L22 L23	Detect of D connector I/P	
23 29 35 41	PB1 PB2 PB3 PB4	Color difference signal input	
24 30 36	L31 L32 L33	Detect of D connector aspect	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
25 31 37 43	PR1 PR2 PR3 PR4	Color difference signal input	
38 40 42	SW1 SW2 SW3	SW of D connector	
45	SDA	Data input of I ² C BUS	
46	SCL	CLK input of I ² C BUS	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
48 61	V _{OUT4} V _{OUT}	Composite signal output for teletexts Composite signal output for GRS *GRS Ghost Reduction System	
49	DC _{OUT}	S - DC _{OUT}	
50 51 52	C _{OUT3} V _{OUT3} Y _{OUT3}	Monitor output	
54 58	PR _{OUT2} PR _{OUT1}	Color difference signal output	

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
55 59	PB _{OUT2} /C _{OUT2} PB _{OUT1} /C _{OUT1}	Color difference signal or Croma signal output	
56 60	CY _{OUT2} /Y _{OUT2} /V _{OUT2} CY _{OUT1} /Y _{OUT1} /V _{OUT1}	Color difference signal, Luminance signal or Composite signal output	
64 66 72 78	O1 O2 O3 O4	Output port 1~4	

Phased Out Products

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-65~+150	°C
Operating temperature	T _{OPR}	-40~+85	°C
Supply voltage	V _{CC} max.	-0.2~+13	V
Input voltage	V _{IN} max.	-0.2~V _{CC} +0.2	V
Output voltage	V _{OUT} max.	-0.2~V _{CC} +0.2	V
Output current	I _{OUT} max.	25	mA
Junction temperature	T _j max.	150	°C
Thermal resistance	θ _{j-c}	6.0	°C/W
Allowable loss *1	P _d	3.6	W

Note: *1 Board mounting power dissipation. Board size 193×189×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T _{OPR}	-40~+85	°C
Operating voltage	V _{CCOP}	+8.0~+10.0	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=9V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption						
Current consumption	I _{CC0}	No signal OUT1 & OUT2 Power Save bit "0"	110	155	200	mA
Current of power save 1	I _{CC1}	No signal OUT1 Power Save bit "0" OUT2 Power Save bit "1" or OUT1 Power Save bit "1" OUT2 Power Save bit "0"	90	130	170	mA
Current of power save 2	I _{CC2}	No signal OUT1 & OUT2 Power Save bit "1"	70	100	130	mA
Input pin voltage						
Composite video signal input	V _{VIN}	3, 9, 15, 17, 19, 63, 65, 71, 77 PIN	5.1	5.5	5.9	V
Luminance signal input	V _{YIN}	5, 11, 67, 73, 79 PIN	5.1	5.5	5.9	V
Croma signal input	V _{CIN}	1, 7, 13, 69, 75 PIN	5.1	5.5	5.9	V
Color difference signal input 1	V _{CYIN}	21, 27, 33, 39 PIN	5.1	5.5	5.9	V
Color difference signal input 2	V _{PBIN}	23, 29, 35, 41 PIN	5.1	5.5	5.9	V
Color difference signal input 3	V _{PrIN}	25, 31, 37, 43 PIN	5.1	5.5	5.9	V
Output pin voltage						
Composite video signal output	V _{VOUT}	48, 51, 61 PIN	3.4	3.8	4.2	V
Luminance signal output	V _{YOUT}	52 PIN	3.4	3.8	4.2	V
Croma signal output	V _{COUT}	50 PIN	3.4	3.8	4.2	V
Color difference signal output 1	V _{CYOUT}	56, 60 PIN	3.4	3.8	4.2	V
Color difference signal output 2	V _{PBOUT}	55, 59 PIN	3.4	3.8	4.2	V
Color difference signal output 3	V _{PrOUT}	54, 58 PIN	3.4	3.8	4.2	V

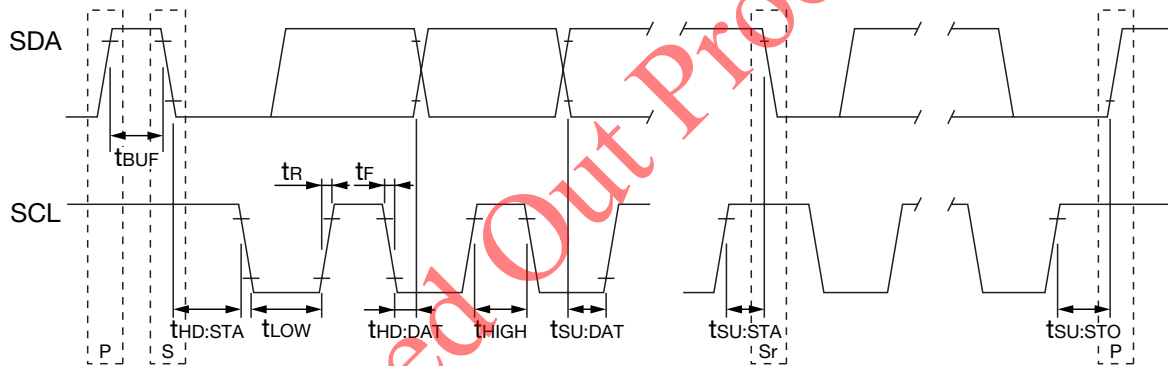
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
S-DC_{OUT} pin output voltage							
S-DC_{OUT} PIN output voltage	L	V _{DCOUT L}	49 PIN R _L =10kΩ+100kΩ		0.1	0.5	V
	M	V _{DCOUT M}	49 PIN R _L =10kΩ+100kΩ	1.6	2.1	2.4	V
	H	V _{DCOUT H}	49 PIN R _L =10kΩ+100kΩ	4.3	4.6		V
Input impedance							
V _{IN} input impedance	Z _{VIN}	3, 9, 15, 17, 19, 63, 65, 71, 77 PIN	135	190	250	kΩ	
Y _{IN} input impedance	Z _{YIN}	5, 11, 67, 73, 79 PIN	135	190	250	kΩ	
C _{IN} input impedance	Z _{CIN}	1, 7, 13, 69, 75 PIN	135	190	250	kΩ	
CY _{IN} input impedance	Z _{CYIN}	21, 27, 33, 39 PIN	135	190	250	kΩ	
Pb _{IN} input impedance	Z _{PbIN}	23, 29, 35, 41 PIN	135	190	250	kΩ	
Pr _{IN} input impedance	Z _{PrIN}	25, 31, 37, 43 PIN	135	190	250	kΩ	
V_{OUT} (61PIN) electrical characteristics							
V _{OUT} voltage gain	G _{VVOUT}	SIN wave: 1V, f=100kHz	-0.3	0.0	0.3	dB	
V _{OUT} frequency characteristic	f _{VOUT}	SIN wave: 1V, 10MHz/100kHz	-1.0	0.0	1.5	dB	
V _{OUT} input dynamic range	DR _{VOUT}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V	
V _{OUT} crosstalk	CT _{VOUT}	SIN wave: 1V, f=4.43MHz		-65	-55	dB	
V_{OUT3} (51PIN) electrical characteristics							
V _{OUT3} voltage gain	G _{VVOUT3}	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB	
V _{OUT3} frequency characteristic	with filter	f _{1VOUT3}	SIN wave: 1V, 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f _{2VOUT3}	SIN wave: 1V, 27MHz/100kHz		-33.0	-24.0	dB
V _{OUT3} input dynamic range	DR _{VOUT3}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V	
V _{OUT3} group delay	with filter	t _{GDVOUT3}	at 100kHz		50	ns	
V _{OUT3} group delay deviation 1	with filter	Δt _{1GDVOUT3}	to 3.58MHz		4	20	ns
V _{OUT3} group delay deviation 2	with filter	Δt _{2GDVOUT3}	to 4.43MHz		7	20	ns
V _{OUT3} group delay deviation 3	with filter	Δt _{3GDVOUT3}	to 6MHz		12	20	ns
V _{OUT3} crosstalk	CT _{VOUT3}	SIN wave: 1V, f=4.43MHz		-65	-55	dB	
V_{OUT4} (48PIN) electrical characteristics							
V _{OUT4} voltage gain	0dB	G _{V1VOUT4}	SIN wave: 1V, f=100kHz	-0.3	0.0	0.3	dB
	6dB	G _{V2VOUT4}	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB
V _{OUT4} frequency characteristic	f _{VOUT4}	SIN wave: 1V, 10MHz/100kHz	-1.0	0.0	1.0	dB	
V _{OUT4} input dynamic range	DR _{VOUT4}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V	
V _{OUT4} crosstalk	CT _{VOUT4}	SIN wave: 1V, f=4.43MHz		-65	-55	dB	
Y_{OUT3} (52PIN) electrical characteristics							
Y _{OUT3} voltage gain	G _{VYOUT3}	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB	
Y _{OUT3} frequency characteristic	with filter	f _{1YOUT3}	SIN wave: 1V, 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f _{2YOUT3}	SIN wave: 1V, 27MHz/100kHz		-33.0	-24.0	dB
Y _{OUT3} input dynamic range	DR _{YOUT3}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V	
Y _{OUT3} group delay	with filter	t _{GDYOUT3}	at 100kHz		50	ns	
Y _{OUT3} group delay deviation 1	with filter	Δt _{1GDYOUT3}	to 3.58MHz		4	20	ns
Y _{OUT3} Group delay deviation 2	with filter	Δt _{2GDYOUT3}	to 4.43MHz		7	20	ns
Y _{OUT3} group delay deviation 3	with filter	Δt _{3GDYOUT3}	to 6MHz		12	20	ns
Y _{OUT3} crosstalk	CT _{YOUT3}	SIN wave: 1V, f=4.43MHz		-45	-43	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
(50PIN) electrical characteristics								
C _{OUT3} voltage gain	G _V C _{OUT3}	SIN wave: 1V, f=100kHz	5.7	6.0	6.3	dB		
C _{OUT3} frequency characteristic	with filter	f ₁ C _{OUT3}	SIN wave: 1V, 6.75MHz/100kHz		-1.0	0.0	1.0	dB
		f ₂ C _{OUT3}	SIN wave: 1V, 27MHz/100kHz			-33.0	-24.0	dB
C _{OUT3} input dynamic range	DR _C OUT3	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V		
C _{OUT3} group delay	with filter	t _G D _C OUT3	at 100kHz			50	ns	
C _{OUT3} group delay deviation 1	with filter	Δt ₁ G _D C _{OUT3}	to 3.58MHz			4	20	ns
C _{OUT3} group delay deviation 2	with filter	Δt ₂ G _D C _{OUT3}	to 4.43MHz			7	20	ns
C _{OUT3} group delay deviation 3	with filter	Δt ₃ G _D C _{OUT3}	to 6MHz			12	20	ns
C _{OUT3} crosstalk	CT _C OUT3	SIN wave: 1V, f=4.43MHz		-45	-43	dB		
CY_{OUT} (56,60PIN) electrical characteristics								
CY _{OUT} voltage gain	0dB	G _V 1 _C Y _{OUT}	SIN wave: 1V, f=100kHz		-0.3	0.0	0.3	dB
	6dB	G _V 2 _C Y _{OUT}	SIN wave: 1V, f=100kHz		5.7	6.0	6.3	dB
CY _{OUT} frequency characteristic	without filter	f ₁ C _Y OUT	SIN wave: 1V, 50MHz/100kHz		-3.0	2.0	3.0	dB
	with filter	f ₂ C _Y OUT	SIN wave: 1V, 13.5MHz/100kHz		-1.0	0.0	1.0	dB
		f ₃ C _Y OUT	SIN wave: 1V, 54MHz/100kHz			-33.0	-24.0	dB
CY _{OUT} input dynamic range	DR _C Y _{OUT}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V		
CY _{OUT} group delay	with filter	t _G D _C Y _{OUT}	at 100kHz			25	ns	
CY _{OUT} group delay deviation 1	with filter	Δt ₁ G _D C _Y OUT	to 3.58MHz			1	20	ns
CY _{OUT} group delay deviation 2	with filter	Δt ₂ G _D C _Y OUT	to 4.43MHz			1	20	ns
CY _{OUT} group delay deviation 3	with filter	Δt ₃ G _D C _Y OUT	to 12MHz			9	20	ns
CY _{OUT} crosstalk	CT _C Y _{OUT}	SIN wave: 1V, f=4.43MHz		-65	-55	dB		
Pb_{OUT} (55,59PIN) electrical characteristics								
Pb _{OUT} Voltage gain	0dB	G _V 1 _P b _{OUT}	SIN wave: 1V, f=100kHz		-0.3	0.0	0.3	dB
	6dB	G _V 2 _P b _{OUT}	SIN wave: 1V, f=100kHz		5.7	6.0	6.3	dB
Pb _{OUT} frequency characteristic	without filter	f ₁ P _b OUT	SIN wave: 1V, 25MHz/100kHz		-3.0	4.0	5.0	dB
	with filter	f ₂ P _b OUT	SIN wave: 1V, 13.5MHz/100kHz		-1.0	2.0	3.0	dB
		f ₃ P _b OUT	SIN wave: 1V, 54MHz/100kHz			-33.0	-24.0	dB
Pb _{OUT} input dynamic range	DR _P b _{OUT}	SIN wave: 100kHz, THD=1.0%	2.5	3.0		V		
Pb _{OUT} group delay	with filter	t _G D _P b _{OUT}	at 100kHz			25	ns	
Pb _{OUT} group delay deviation 1	with filter	Δt ₁ G _D P _b OUT	to 3.58MHz			1	20	ns
Pb _{OUT} group delay deviation 2	with filter	Δt ₂ G _D P _b OUT	to 4.43MHz			1	20	ns
Pb _{OUT} group delay deviation 3	with filter	Δt ₃ G _D P _b OUT	to 12MHz			9	20	ns
Pb _{OUT} crosstalk	CT _P b _{OUT}	SIN wave: 1V, f=4.43MHz		-65	-55	dB		

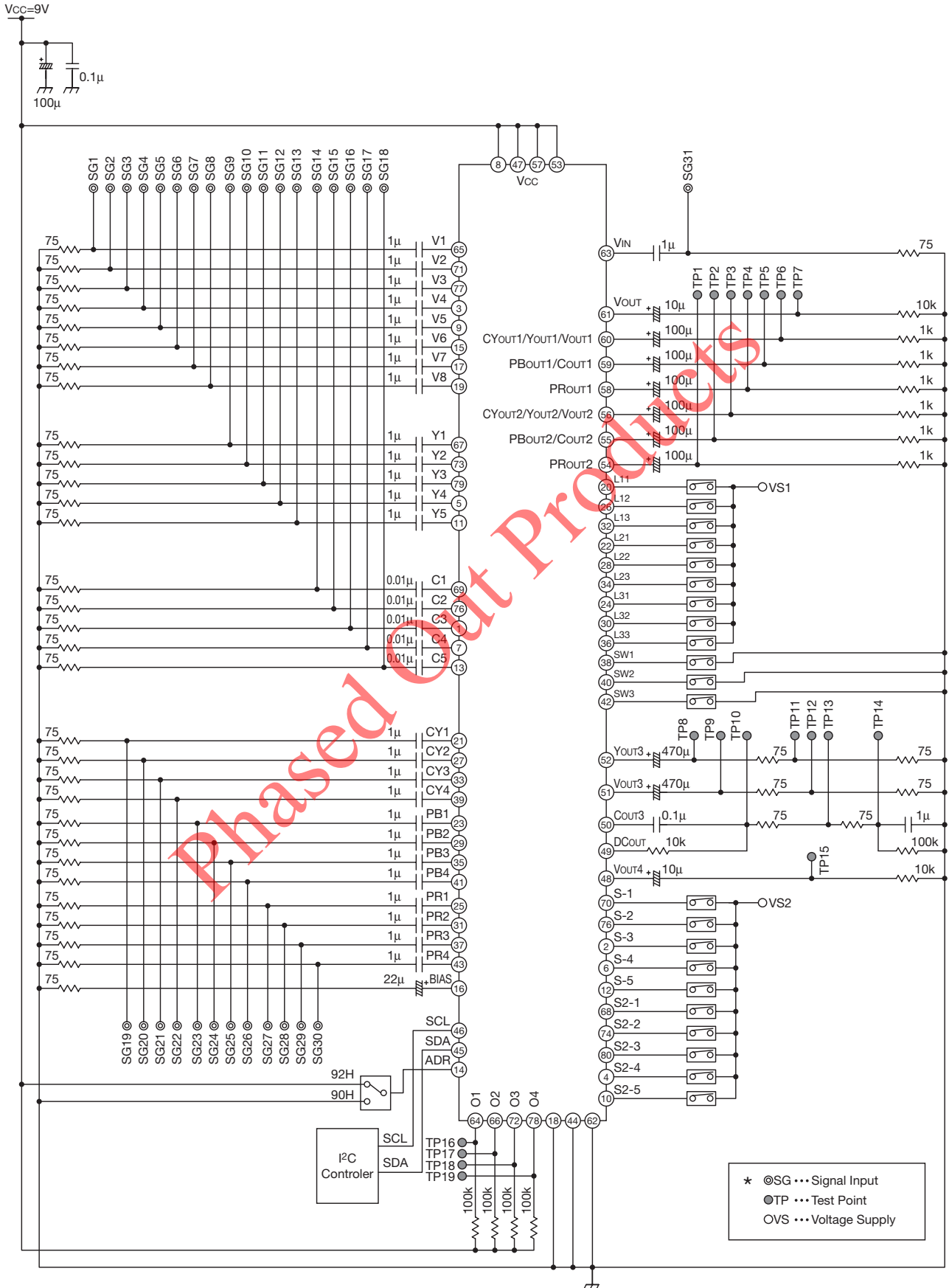
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
PrOUT (54,58PIN) electrical characteristics								
PrOUT voltage gain	0dB	Gv1PrOUT	SIN wave: 1V, f=100kHz		-0.3	0.0	0.3	dB
	6dB	Gv2PrOUT	SIN wave: 1V, f=100kHz		5.7	6.0	6.3	dB
PrOUT frequency characteristic	without filter	f1PrOUT	SIN wave: 1V, 25MHz/100kHz		-3.0	4.0	5.0	dB
	with filter	f2PrOUT	SIN wave: 1V, 13.5MHz/100kHz		-1.0	2.0	3.0	dB
		f3PrOUT	SIN wave: 1V, 54MHz/100kHz			-33.0	-24.0	dB
PrOUT input dynamic range	DRPrOUT	SIN wave: 100kHz, THD=1.0%		2.5	3.0		V	
PrOUT group delay	with filter	tGDPPrOUT	at 100kHz			25		ns
PrOUT group delay deviation 1	with filter	$\Delta t1GDPPrOUT$	to 3.58MHz			1	20	ns
PrOUT group delay deviation 2	with filter	$\Delta t2GDPPrOUT$	to 4.43MHz			1	20	ns
PrOUT group delay deviation 3	with filter	$\Delta t3GDPPrOUT$	to 12MHz			9	20	ns
PrOUT crosstalk	CTPrOUT	SIN wave: 1V, f=4.43MHz		-65	-55		dB	
Group delay deviation-between each channels								
Group delay deviation between C and Y	$\Delta t1chGD$	between C and Y at 3.58MHz			0	10	ns	
Group delay deviation between CY and Pb (Pr)	$\Delta t2chGD$	between CY and Pb (Pr) at 2MHz			0	10	ns	
O1 (64PIN) electrical characteristics								
O1 pin low level output voltage	V01	O1 PIN sink 1mA		0.0		0.4	V	
O1 pin Leak current (at the time of OFF)	I01			-1.0		1.0	μ A	
O2 (66PIN) electrical characteristics								
O2 pin low level output voltage	V02	O2 PIN sink 1mA		0.0		0.4	V	
O2 pin Leak current (at the time of OFF)	I02			-1.0		1.0	μ A	
O3 (72PIN) electrical characteristics								
O3 pin low level output voltage	V03	O3 PIN sink 1mA		0.0		0.4	V	
O3 pin Leak current (at the time of OFF)	I03			-1.0		1.0	μ A	
O4 (78PIN) electrical characteristics								
O4 pin low level output voltage	V04	O4 PIN sink 1mA		0.0		0.4	V	
O4 pin leak current (at the time of OFF)	I04			-1.0		1.0	μ A	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C condition						
Input voltage L	V _{IL}		0.0		0.8	V
Input voltage H	V _{IH}		2.2		5.0	V
SDA low level output voltage	V _{OL}	SDA sink 3mA	0.0		0.4	V
High level input current	I _{IH}	SDA, SCL=4.5V	-10		10	μA
Low level input current	I _{IL}	SDA, SCL=0.4V	-10		10	μA
Clock Frequency	f _{SCL}				100	kHz
Data transfer wait time	t _{BUF}		4.7			μs
SCL start hold time	t _{HD; STA}		4.0			μs
SCL low level hold time	t _{LOW}		4.7			μs
SCL high level hold time	t _{HIGH}		4.0			μs
Start condition setup time	t _{SU; STA}		4.7			μs
SDA data hold time	t _{HD; DAT}		200			ns
SDA data setup time	t _{SU; DAT}		250			ns
SDA,SCL rise time	t _R				1000	ns
SDA,SCL fall time	t _F				300	ns
Stop condition setup time	t _{SU; STO}		4.0			μs

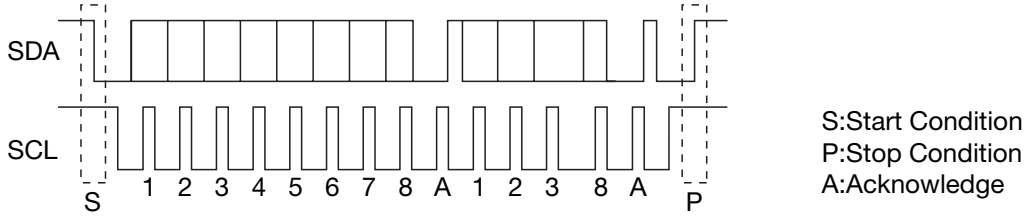
Note I²C condition



Measuring Circuit



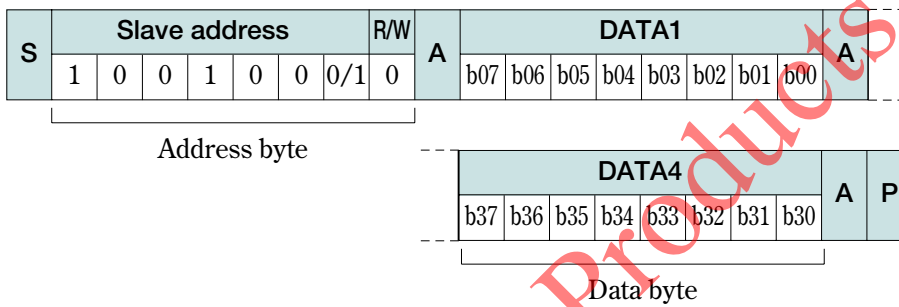
I²C BUS



I²C BUS is inter bus system controlled by 2 lines (SDA.SCL).
 Data are transmitted and received in the units of byte and Acknowledge.
 It is transmitted by MSB first from the start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.
 The data format is set as shown in the following figure.)



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit.
 Set the R/W bit to 0 when data are used control registers.

As MM1630 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches.
 Each bit of control registers is reset to 0, when power-on.

MM1630 consists of one address byte and 4 control data bytes (5bytes in total).
 All data over the limited length (XXXth and subsequent bytes) are fully neglected.
 For details of the control contents of switches, refer to the another table.

No.	DATA condition							
DATA1 (00H)	b07	b06	b05	b04	b03	b02	b01	b00
	OUT1 LPF SW	OUT1 Power Save	OUT1 GAIN SW	OUT1 LINE SELECT				
DATA2 (00H)	b17	b16	b15	b14	b13	b12	b11	b10
	OUT2 LPF SW	OUT1 Power Save	OUT1 GAIN SW	OUT2 LINE SELECT				
DATA3 (00H)	b27	b26	b25	b24	b23	b22	b21	b20
	OUT4 LINE SELECT				OUT3 LINE SELECT			
DATA4 (00H)	b37	b36	b35	b34	b33	b32	b31	b30
	O4 OUTPUT	O3 OUTPUT	O2 OUTPUT	O1 OUTPUT	DCout OUTPUT VOLTAGE		OUT4 GAIN SW	

* [00H] is in the initial state of control registers.

Switch Control Table

OUT1 LINE SELECT

b04	b03	b02	b01	b00	V _{OUT1}	PB _{OUT1}	PR _{OUT1}	V _{OUT}
0	0	0	0	0	Mute	Mute	Mute	Mute
0	0	0	0	1	V1	Mute	Mute	V1
0	0	0	1	0	V2	Mute	Mute	V2
0	0	0	1	1	V3	Mute	Mute	V3
0	0	1	0	0	V4	Mute	Mute	V4
0	0	1	0	1	V5	Mute	Mute	V5
0	0	1	1	0	V6	Mute	Mute	V6
0	0	1	1	1	V7	Mute	Mute	V7
0	1	0	0	0	V8	Mute	Mute	V8
0	1	0	0	1	V1 (GRS)	Mute	Mute	V1
0	1	0	1	0	V2 (GRS)	Mute	Mute	V2
0	1	0	1	1	V3 (GRS)	Mute	Mute	V3
0	1	1	0	0	V4 (GRS)	Mute	Mute	V4
0	1	1	0	1	V5 (GRS)	Mute	Mute	V5
0	1	1	1	0	V6 (GRS)	Mute	Mute	V6
0	1	1	1	1	V7 (GRS)	Mute	Mute	V7
1	0	0	0	0	V8 (GRS)	Mute	Mute	V8
1	0	0	0	1	Y1	C1	Mute	Mute
1	0	0	1	0	Y2	C2	Mute	Mute
1	0	0	1	1	Y3	C3	Mute	Mute
1	0	1	0	0	Y4	C4	Mute	Mute
1	0	1	0	1	Y5	C5	Mute	Mute
1	0	1	1	0	CY1	PB1	PR1	Mute
1	0	1	1	1	CY2	PB2	PR2	Mute
1	1	0	0	0	CY3	PB3	PR3	Mute
1	1	0	0	1	CY4	PB4	PR4	Mute
1	1	0	1	0	Mute	Mute	Mute	Mute
					Mute	Mute	Mute	Mute
1	1	1	1	1	Mute	Mute	Mute	Mute

■ OUT2 LINE SELECT

b14	b13	b12	b11	b10	V _{out2}	PB _{out2}	PR _{out2}
0	0	0	0	0	Mute	Mute	Mute
0	0	0	0	1	V1	Mute	Mute
0	0	0	1	0	V2	Mute	Mute
0	0	0	1	1	V3	Mute	Mute
0	0	1	0	0	V4	Mute	Mute
0	0	1	0	1	V5	Mute	Mute
0	0	1	1	0	V6	Mute	Mute
0	0	1	1	1	V7	Mute	Mute
0	1	0	0	0	V8	Mute	Mute
0	1	0	0	1	Mute	Mute	Mute
⋮					Mute	Mute	Mute
1	0	0	0	0	Mute	Mute	Mute
1	0	0	0	1	Y1	C1	Mute
1	0	0	1	0	Y2	C2	Mute
1	0	0	1	1	Y3	C3	Mute
1	0	1	0	0	Y4	C4	Mute
1	0	1	0	1	Y5	C5	Mute
1	0	1	1	0	CY1	PB1	PR1
1	0	1	1	1	CY2	PB2	PR2
1	1	0	0	0	CY3	PB3	PR3
1	1	0	0	1	CY4	PB4	PR4
1	1	0	1	0	Mute	Mute	Mute
⋮					Mute	Mute	Mute
1	1	1	1	1	Mute	Mute	Mute

■ OUT3 LINE SELECT

b23	b22	b21	b20	V _{out3}	Y _{out3}	C _{out3}
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Y1+C1	Y1	C1
0	0	1	0	Y2+C2	Y2	C2
0	0	1	1	Y3+C3	Y3	C3
0	1	0	0	Y4+C4	Y4	C4
0	1	0	1	Y5+C5	Y5	C5
0	1	1	0	V1	Mute	Mute
0	1	1	1	V2	Mute	Mute
1	0	0	0	V3	Mute	Mute
1	0	0	1	V4	Mute	Mute
1	0	1	0	V5	Mute	Mute
1	0	1	1	V6	Mute	Mute
1	1	0	0	V7	Mute	Mute
1	1	0	1	V8	Mute	Mute
1	1	1	0	CY4+PB4	CY4	PB4
1	1	1	1	Mute	Mute	Mute

■ OUT4 LINE SELECT

b27	b26	b25	b24	V _{out4}
0	0	0	0	Mute
0	0	0	1	Y1+C1
0	0	1	0	Y2+C2
0	0	1	1	Y3+C3
0	1	0	0	Y4+C4
0	1	0	1	Y5+C5
0	1	1	0	V1
0	1	1	1	V2
1	0	0	0	V3
1	0	0	1	V4
1	0	1	0	V5
1	0	1	1	V6
1	1	0	0	V7
1	1	0	1	V8
1	1	1	0	CY4+PB4
1	1	1	1	Mute

■ DC_{OUT} OUTPUT VOLTAGE

b33	b32	DC _{OUT}
0	0	0V
0	1	2.2V
1	*	5V

■ GAIN SW

bit	GAIN
0	0dB
1	6dB

■ Power save SW

bit	Conditions
0	Active
1	Power Save

■ LPF SW

bit	LPF
0	without filter
1	with filter

■ O1~O4 OUTPUT

bit	O1~O4
0	Low
1	Open

■ L11, L12, L13 DETECT (Scanning Line)

L11~L13 Voltage	Scanning Line	2bit	1bit
DC ≤ 1.0V	480	0	0
1.3V ≤ DC ≤ 2.7V	720	0	1
3.5V ≤ DC ≤ 5.0V	1080	1	0

■ S2-1~S2-5 DETECT (Aspect)

S2-1~S2-5 Voltage	Aspect	2bit	1bit
DC ≤ 1.0V	4 : 3	0	0
1.3V ≤ DC ≤ 2.7V	Letter box	0	1
3.5V ≤ DC ≤ 5.0V	16 : 9	1	0

■ L21, L22, L23 DETECT (IP)

L21~L23 Voltage	I/P	1bit
DC ≤ 2.7V	Interlace	0
3.5V ≤ DC ≤ 5.0V	Progressive	1

■ S1~S5 DETECT

S1~S5 Voltage	Conditions	bit
DC ≤ 4.2V	CONNECTED	1
5.3V ≤ DC	UNCONNECTED	0

■ L31, L32, L33 DETECT (Aspect)

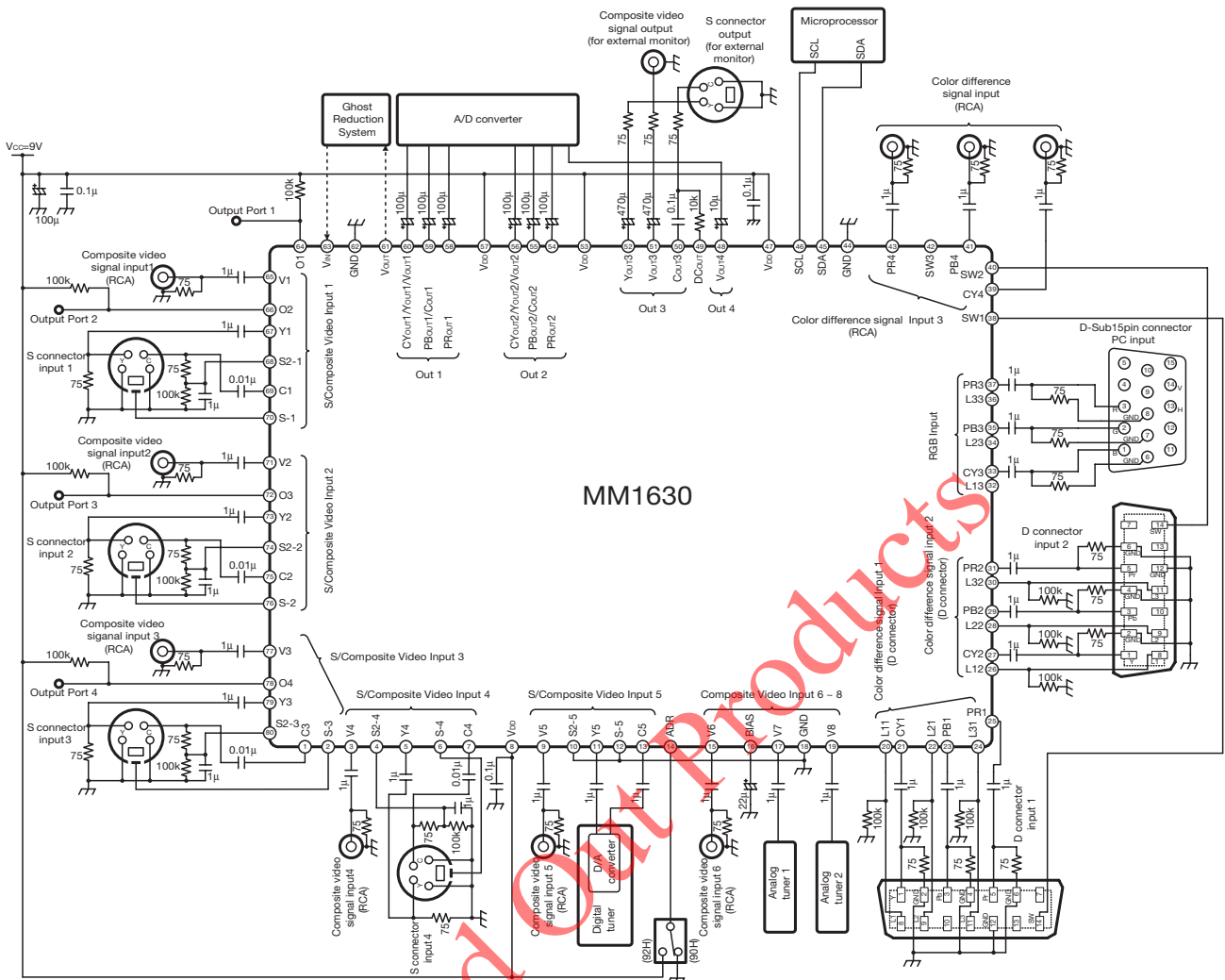
L31~L33 Voltage	Aspect	2bit	1bit
DC ≤ 1.0V	4 : 3	0	0
1.3V ≤ DC ≤ 2.7V	Letter box	0	1
3.5V ≤ DC ≤ 5.0V	16 : 9	1	0

■ SW1~SW3 DETECT

SW1~SW3 Voltage	Conditions	bit
DC ≤ 4.2V	CONNECTED	1
5.3V ≤ DC	UNCONNECTED	0

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Application Circuit



MM1630

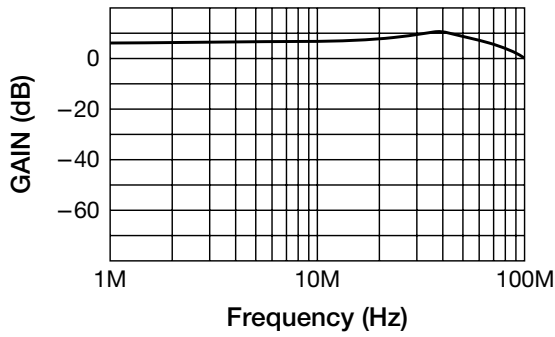
Note:

- We shall not be liable for any trouble or damage caused by using this circuit.
- In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

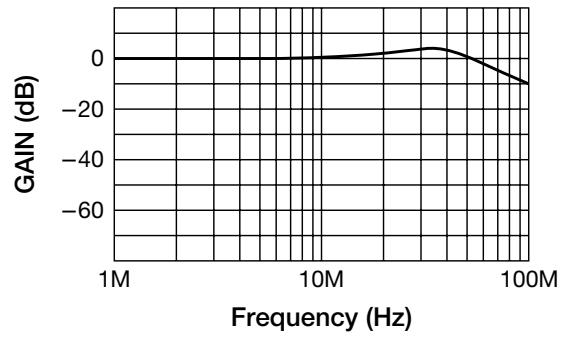
Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=9V)

A. Frequency Characteristics

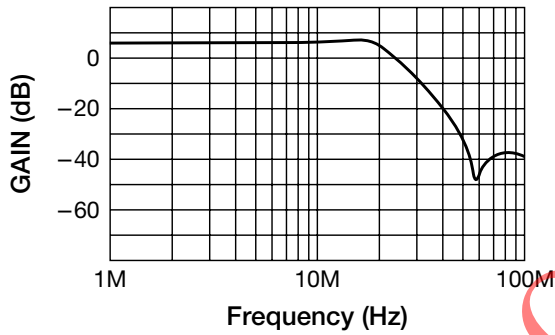
■ CYout1, 2 THRU 6dB



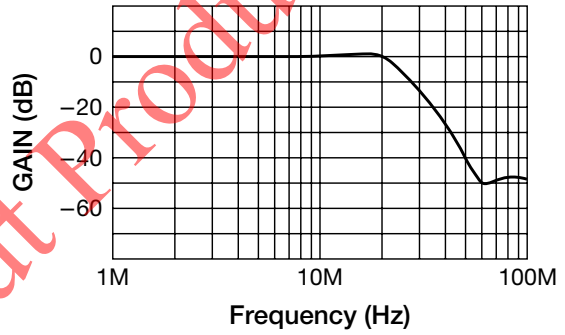
■ CYout1, 2 THRU 0dB



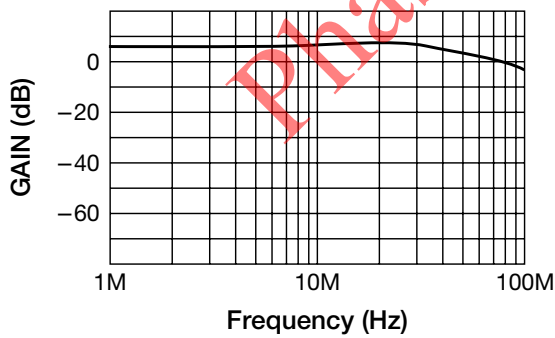
■ CYout1, 2 LPF 6dB



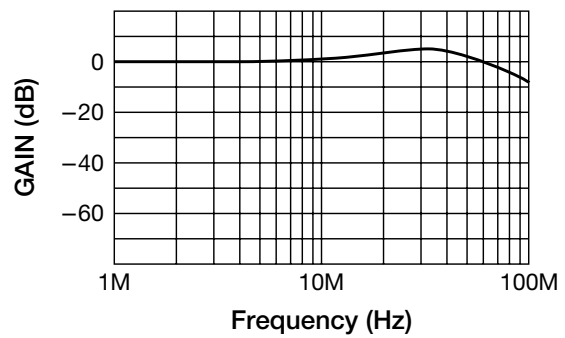
■ CYout1, 2 LPF 0dB



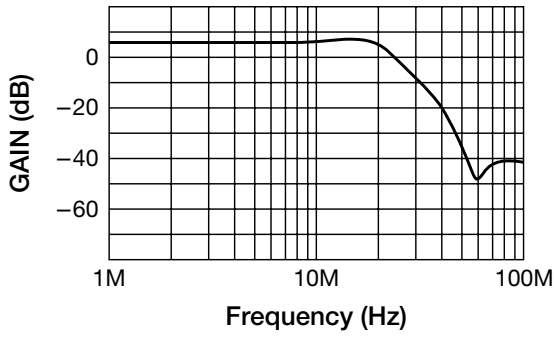
■ Pb, Prout1, 2 THRU 6dB



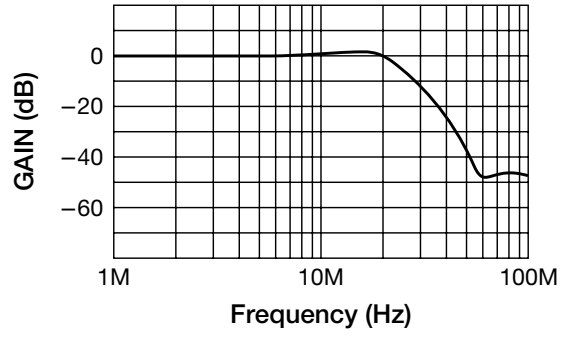
■ Pb, Prout1, 2 THRU 0dB



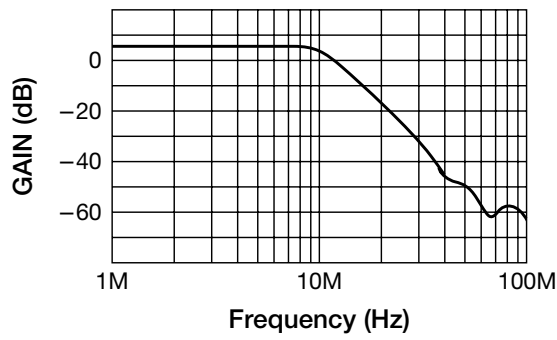
■ Pb, Prout1, 2 LPF 6dB



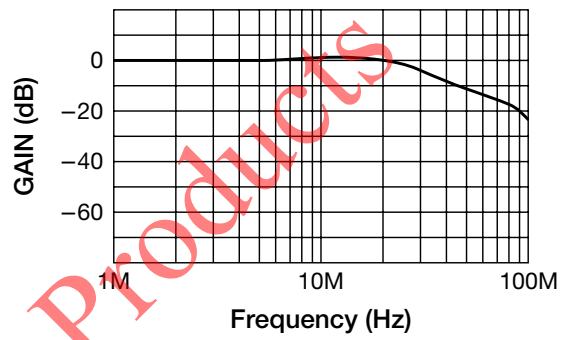
■ Pb, Prout1, 2 LPF 0dB



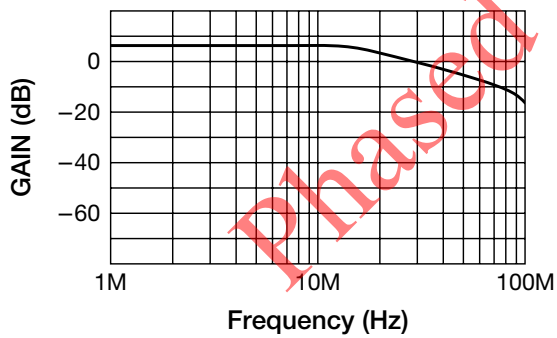
■ V, Y, Cout3



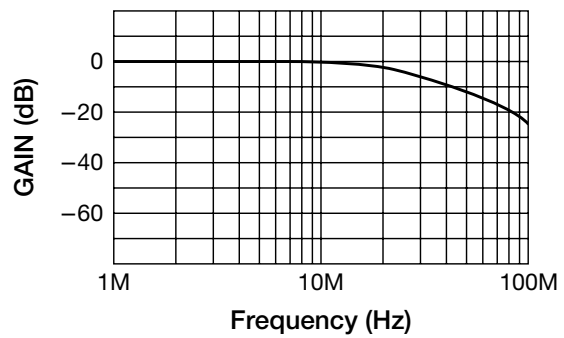
■ Vout



■ Vout4 6dB

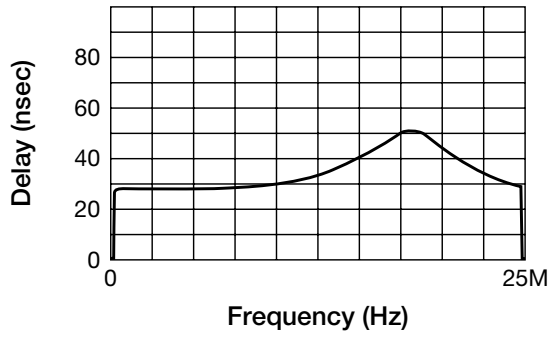


■ Vout4 0dB

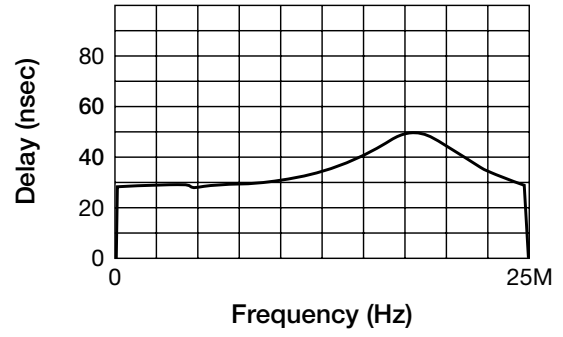


B. Group delay

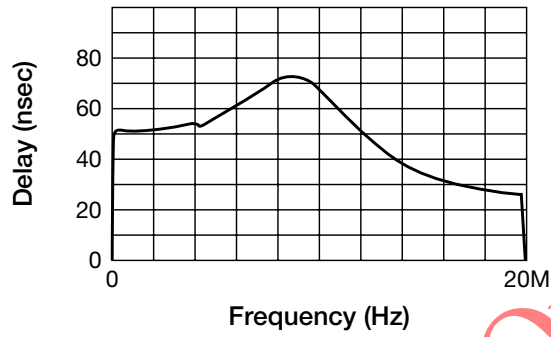
■ CYOUT LPF



■ Pb, PrOUT LPF



■ V, Y, Cout3



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