I²C Bus - Controlled 11-Input 3-Output Audio Switch
Monolithic IC MM1631

Outline

This is an I²C bus controlled audio switch IC developed for TVs, PDP and projection TVs. It provides 11 inputs and 3 outputs of audio singals (R/L).
Design of the input switch block can be simplified by using this IC with MM1630 (video switch IC).

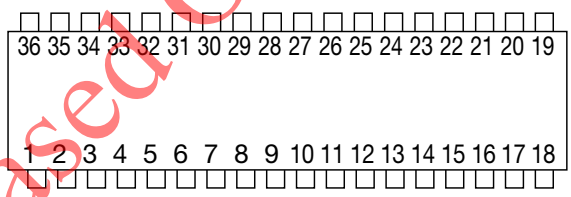
Features

1. The desired input can be selected for each of the 3 independent output lines.
2. Wide dynamic range (3Vrms)
3. Serial by I²C bus
4. Forced mute enabled by an external pin
5. Includes a power-save function
6. I²C bus lines maintain high impedance during power-off.
7. No output waveform folding with 7.1Vrms input

Package

SSOP-36A

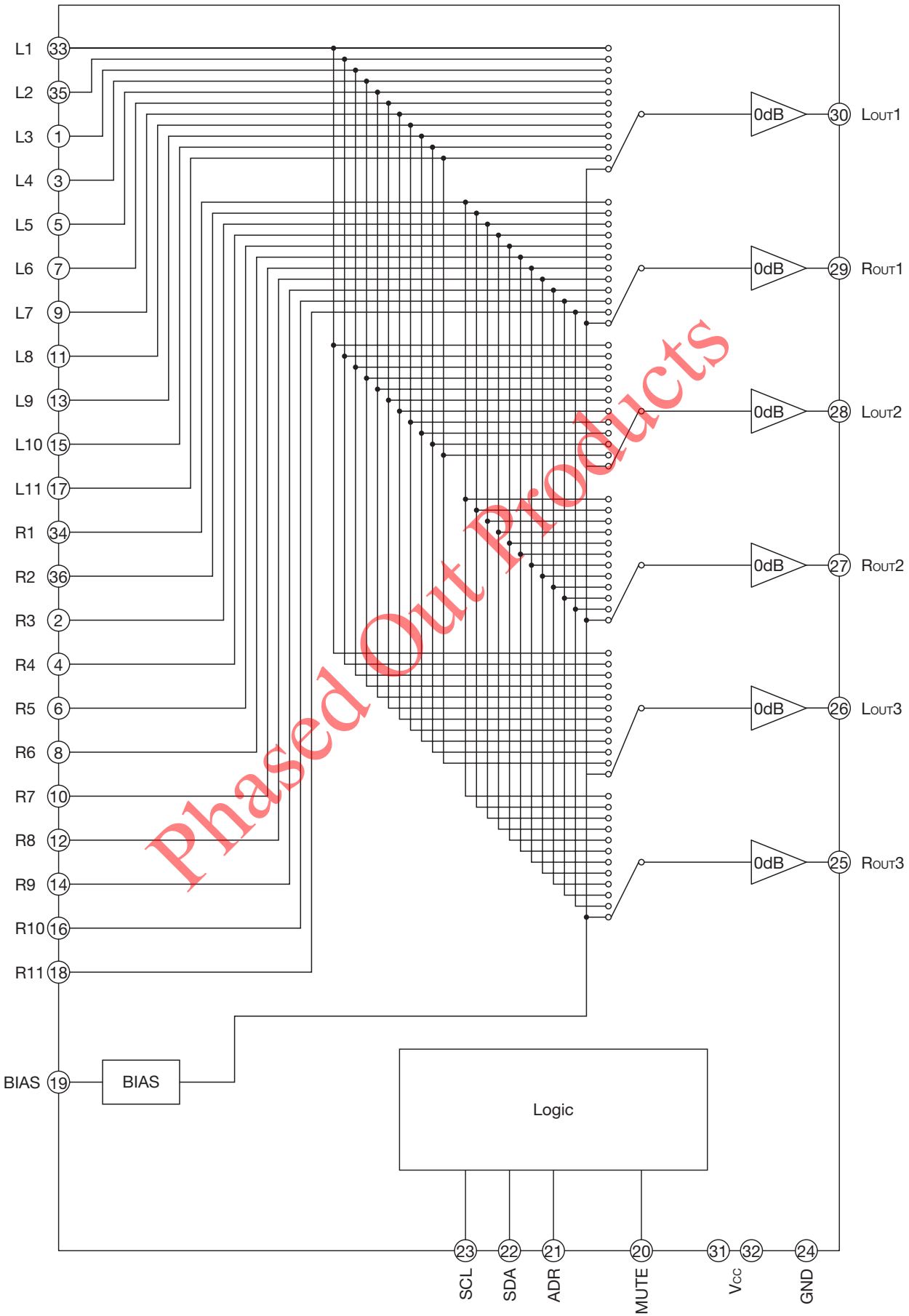
Pin Assignment



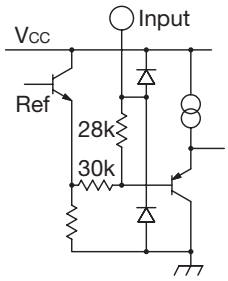
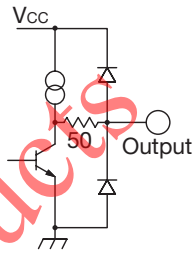
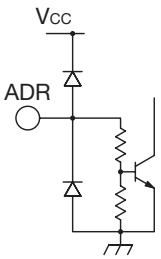
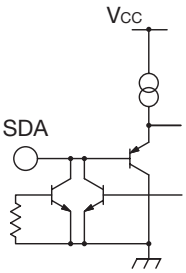
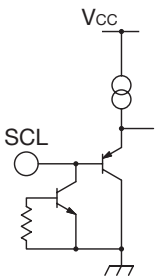
SSOP-36A
(TOP VIEW)

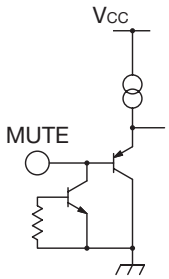
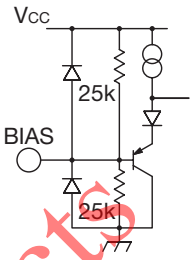
1	L3	10	R7	19	BIAS	28	LOUT2
2	R3	11	L8	20	MUTE	29	ROUT1
3	L4	12	R8	21	ADR	30	LOUT1
4	R4	13	L9	22	SDA	31	VCC
5	L5	14	R9	23	SCL	32	VCC
6	R5	15	L10	24	GND	33	L1
7	L6	16	R10	25	ROUT3	34	R1
8	R6	17	L11	26	LOUT3	35	L2
9	L7	18	R11	27	ROUT2	36	R2

Block Diagram



Pin Description

Pin no.	Pin name	Functions	Internal equivalent circuit diagram
1~18 33~36	L1~L11 R1~R11	Line input of Audio	
25~30	LOUT1~3 ROUT1~3	Line output of Audio	
21	ADR	Slave address select pin	
22	SDA	Data input of I²C BUS	
23	SCL	CLK input of I²C BUS	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
20	MUTE	Mute select pin	
19	BIAS	Connect 22µF between this pin and CND for stabilize internal reference voltage	
31 32	Vcc	Vcc	
24	GND	GND	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	TSTG	–65~+150	°C
Operating temperature	TOPR	–40~+85	°C
Supply voltage	Vcc max.	–0.2~+13	V
I/0 terminal voltage	VIN max. VOUT max.	–0.2~Vcc+0.2	V
Output current	IOUT max.	25	mA
Junction temperature	Tj max.	150	°C
Allowable loss *1	Pd	1.0	W

Note: *1 Board mounting power dissipation. Board size 100×100×1.6mm

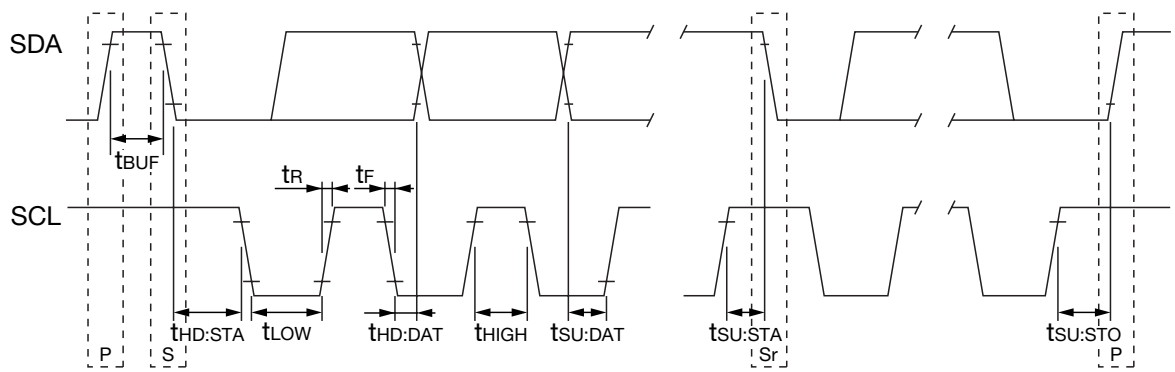
Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	TOPR	–40~+85	°C
Operating voltage	VCCOP	+8.0~+10.0	V
Operating I/0 voltage	VINOP VOUTOP	0~Vcc	V

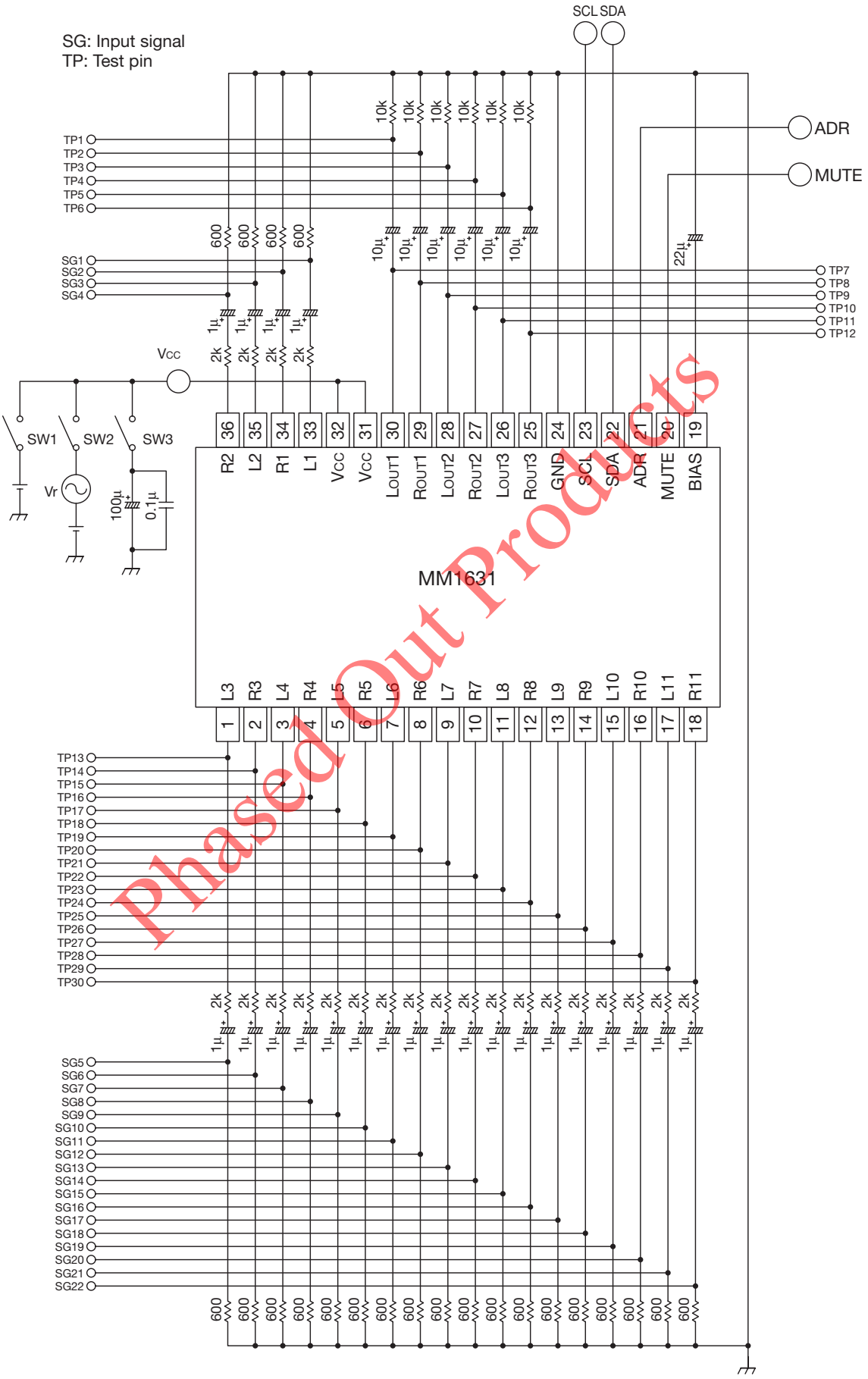
Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=9V, SW1 ON, SW2 OFF, SW3 ON)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption	Icc0	No signal , No Load		35	46	mA
Current of power-save 1	Icc1	OUT1 (or OUT2): Power-Save OUT2 (or OUT1)&3: Active		28	37	mA
Current of power-save 2	Icc2	OUT1 & 2: Power-Save OUT3: Active		21	28	mA
Voltage gain	GV	SG: 1Vrms, 1kHz	–0.5	0	0.5	dB
Frequency characteristic	FBW	SG: 1Vrms, 50kHz	–3			dB
Total harmonic distortion	THD	SG: 1Vrms, 1kHz		0.03	0.05	%
Input dynamic range	DR	f=1kHz, THD=0.5%	2.8	3.0		Vrms
Crosstalk	CT	SG: 1Vrms, f=1kHz, Without power-save mode		–90	–80	dB
Rippler rejection	PSRR	Vr: 100mVrms, 100kHz SW1 OFF, SW2 ON, SW3 OFF		–50	–40	dB
Output offset voltage	VOFF	VOUT (Active)–VOUT (Mute)	–15	0	15	mV
S/N ratio	S/N	SG: 1Vrms, 1kHz, A curve		–100	–90	dB
Input impedance of input terminal	ZIN		47	60	73	kΩ
Input terminal voltage	VIN	No signal , No Load	4.25	4.50	4.75	V
Output terminal voltage	VOUT	No signal , No Load	4.25	4.50	4.75	V
Audio signal input voltage	VSG	No output signal turnup			7.1	Vrms
I²C condition						
Input voltage L	VIL		0.0		0.8	V
Input voltage H	VIH		2.2		5.0	V
SDA low level output voltage	VOL	SDA sink 3mA	0.0		0.4	V
High level input current	IIH	SDA, SCL=4.5V	–10		10	µA
Low level input current	IIL	SDA, SCL=0.4V	–10		10	µA
Clock frequency	fSCL				100	kHz
Data transfer wait time	tBUF		4.7			µs
SCL start hold time	tHD;STA		4.0			µs
SCL low level hold time	tLOW		4.7			µs
SCL high level hold time	tHIGH		4.0			µs
Start condition setup time	tSU;STA		4.7			µs
SDA data hold time	tHD;DAT		200			ns
SDA data setup time	tSU;DAT		250			ns
SDA, SCL rise time	tR				1000	ns
SDA, SCL fall time	tF				300	ns
Stop condition setup time	tSU;STO		4.0			µs

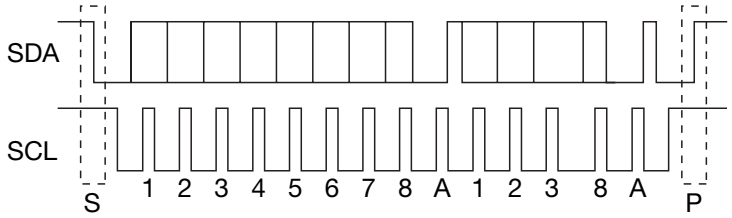
Note I²C condition



Measuring Circuit



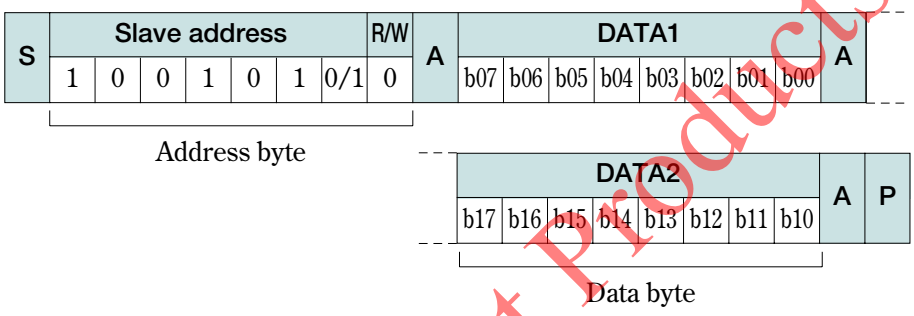
I²C BUS



S:Start Condition
P:Stop Condition
A:Acknowledge

I²C BUS is inter bus system controlled by 2 lines (SDA, SCL).
Data are transmitted and received in the units of byte and acknowledge.
It is transmitted by MSB first from the start conditions.

[Control registers]
Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address,while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1631 slave address, either 94H or 96H can be selected according to the ADR terminal conditions. When ADR terminal is L94H is selected.
The relationship between each bit of the control register and the switch controls are as shown in the figure.
Each bit of control registers is reset to 0, when power-on.)

No.	DATA condition							
DATA1 (00H)	b07	b06	b05	b04	b03	b02	b01	b00
	L1, R2 line select				L1, R2 line select			
DATA2 (00H)	b17	b16	b15	b14	b13	b12	b11	b10
			Power Save (OUT2)	Power Save (OUT2)	L3, R3 line select			

MM1631 consists of one address byte and two control data bytes (3 bytes in total).
All data over the limited length (4th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the another table.

Switch Control Table

L1, R1 OUT select

b03	b02	b01	b00	L1, R1 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

L2, R2 OUT select

b07	b06	b05	b04	L2, R2 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

L3, R3 OUT select

b13	b12	b11	b10	L3, R3 OUT
0	0	0	0	Mute
0	0	0	1	L1, R1
0	0	1	0	L2, R2
0	0	1	1	L3, R3
0	1	0	0	L4, R4
0	1	0	1	L5, R5
0	1	1	0	L6, R6
0	1	1	1	L7, R7
0	0	0	0	L8, R8
1	0	0	1	L9, R9
1	0	1	0	L10, R10
1	0	1	1	L11, R11
1	1	0	0	Mute
1	1	0	1	Mute
1	1	1	0	Mute
1	1	1	1	Mute

Power Save select

b15	b14	L2, R2 OUT	L1, R1 OUT
0	0	Active	Active
0	1	Active	Power Save
1	0	Power Save	Active
1	1	Power Save	Power Save

[Status registers]

There is no preparation of th status register in MM1631. A status register returns all the 1 when 1 is set in the R/W bit. At this time, the control of each SW is not done at all.

S	Slave address							R/W	A	DATA								A	P
	1	0	0	1	0	1	0/1	1		1	1	1	1	1	1	1	1		
	Address byte									Status byte									

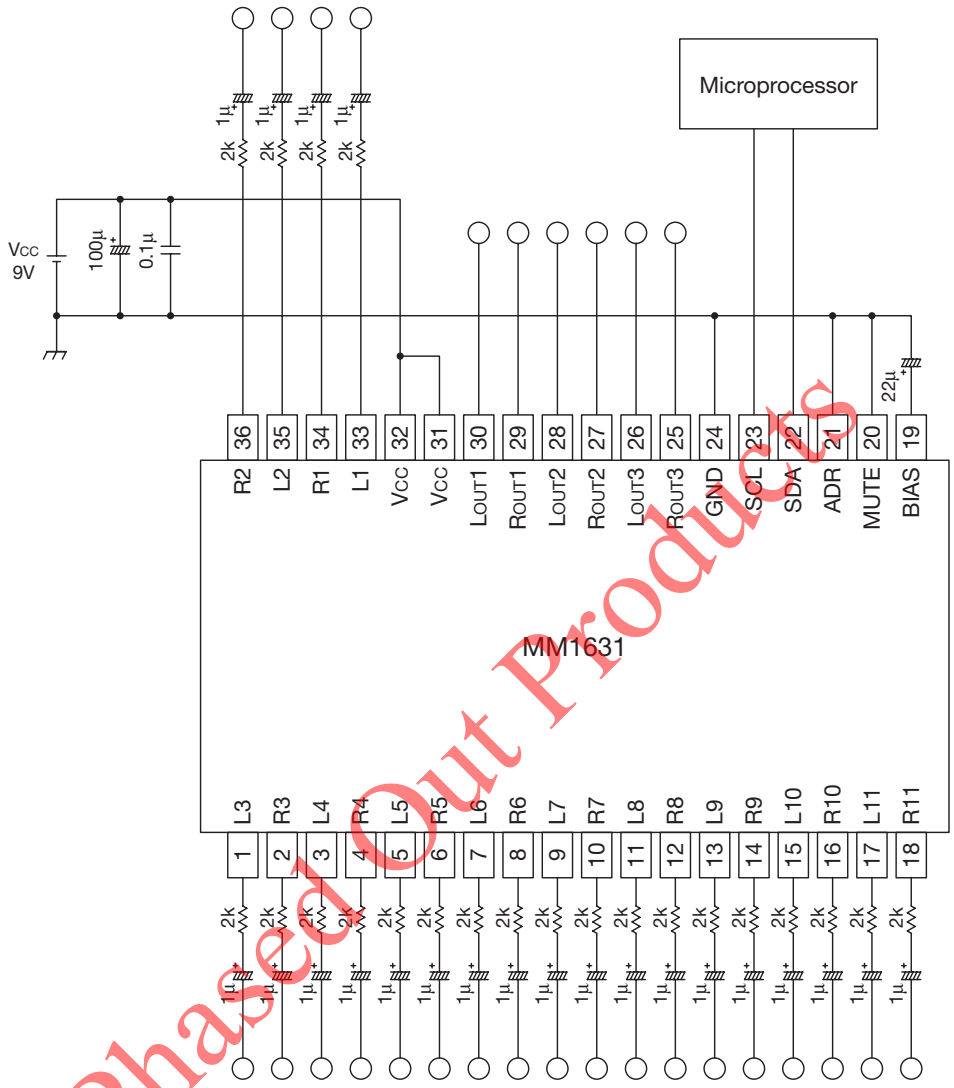
·Mute terminal operation

All of audio output is connected with internal bias-voltage when Mute terminal is "H". And when Mute level return from "H" to "L" , audio output selections return to previous conditions.

Mute select

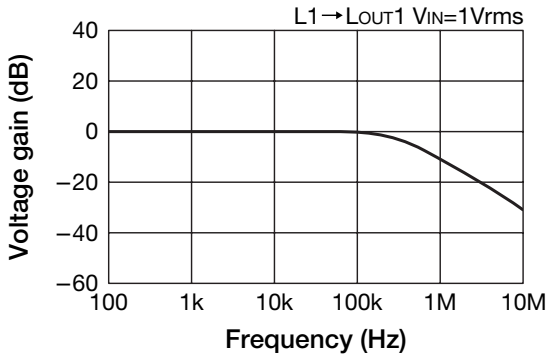
Mute	Output
H	Mute
L	Active

Application Circuit



Characteristics

Frequency characteristic



THD VS Input voltage