Video Switch for DVD Recorders
Monolithic IC MM1697BJ

Outline

This IC is a video switch IC that includes an LPF (anti-aliasing filter) required before A/D conversion for DVD recorders, etc. It provides three input channels for composite video (CV), three input channels for S-Video (Y, C), one output channel for Y/CV$_{OUT}$ (used for both Y and CV), one output channel for C$_{OUT}$, and one output channel for CV$_{OUT}$ (select V$_{IN}$ or Y$_{IN}$+C$_{IN}$). It also includes S-terminal connection detection function, which is ideal as a video input switch for DVD recorders that perform A/D conversion.

Features

1. Input channel: Composite video input ··· 3 channels
   S-Video (Y, C) ··· 3 channels
2. Includes a high performance LPF (anti-aliasing filter)
   −3dB pass bandwidth: 7MHz (typ.)
   Attenuation at 10.7MHz: −36dB (typ.)
   Attenuation at 13.5MHz: −40dB (typ.)
   Attenuation at 27.0MHz: −37dB (typ.)
3. Includes a Y+C amplifier (Y/C MIX)
4. Includes 2 channels for detecting S-terminal connection

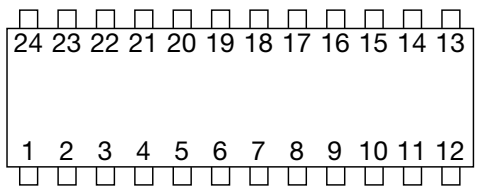
Package

SSOP-24B

Applications

DVD recorder

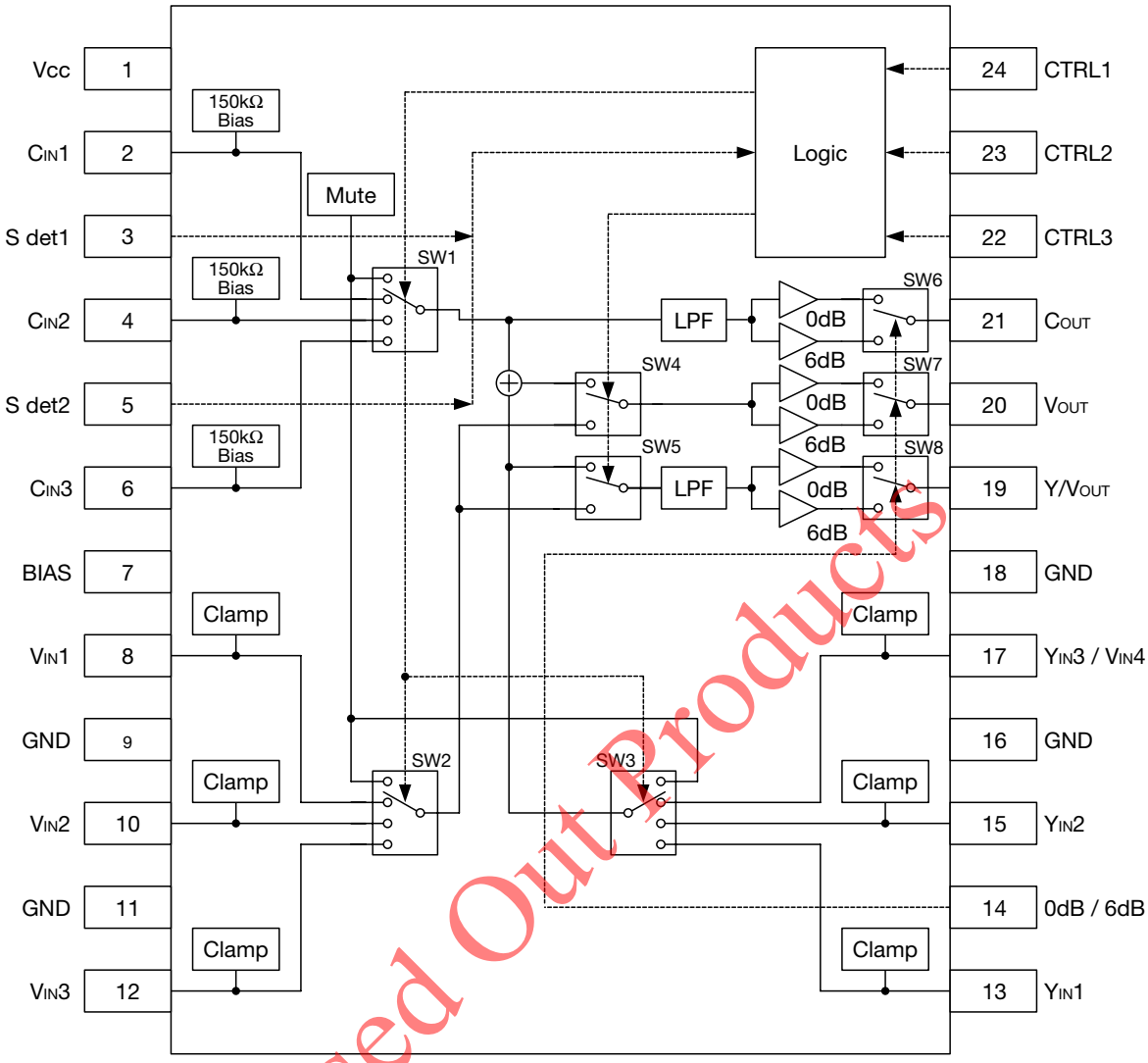
Pin Assignment



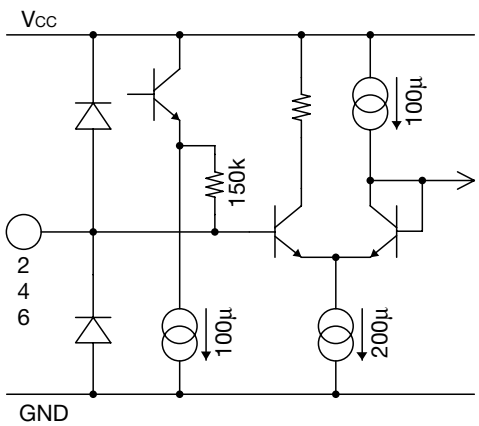
SSOP-24B
(TOP VIEW)

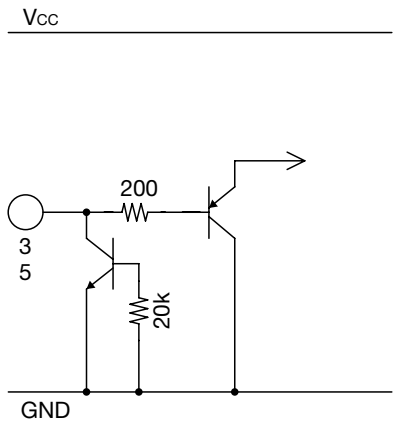
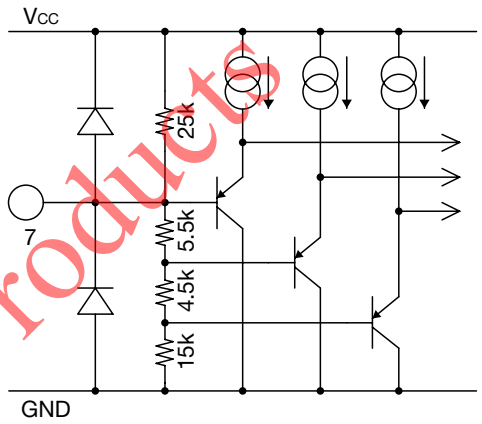
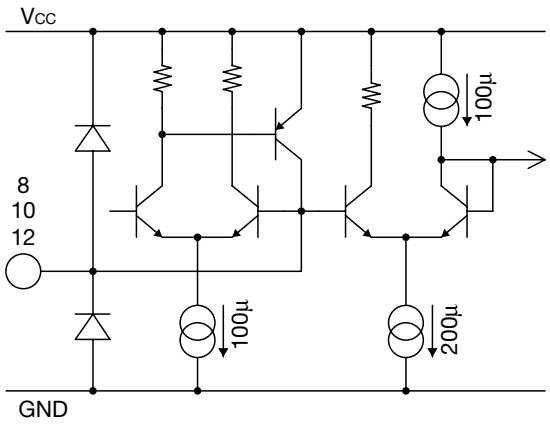
1	V$_{CC}$	9	GND	17	Y$_{IN}$3/V$_{IN}$4
2	C$_{IN}$1	10	V$_{IN}$2	18	GND
3	S det1	11	GND	19	Y/V$_{OUT}$
4	C$_{IN}$2	12	V$_{IN}$3	20	V$_{OUT}$
5	S det2	13	Y$_{IN}$1	21	C$_{OUT}$
6	C$_{IN}$3	14	0dB/6dB	22	CTRL3
7	BIAS	15	Y$_{IN}$2	23	CTRL2
8	V$_{IN}$1	16	GND	24	CTRL1

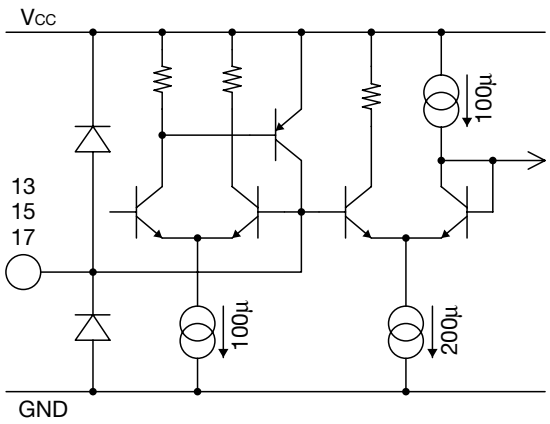
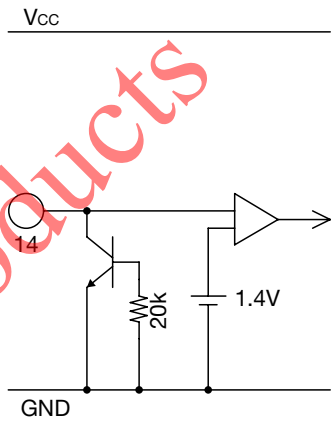
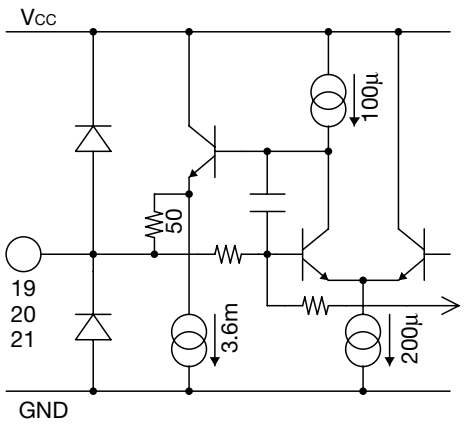
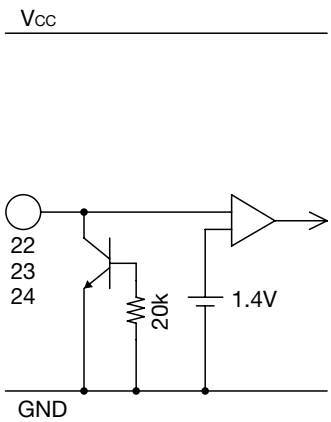
Block Diagram



Pin Description

Pin no.	Pin name	Function	Internal equivalent circuit diagram
1	VCC	VCC	
2 4 6	CIN1 CIN2 CIN3	Chroma signal input 150kΩ bias input (Average clamp input)	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
3 5	Sdet 1 Sdet 2	S-terminal detect	
7	BIAS	Bias	
8 10 12	VIN1 VIN2 VIN3	Video signal input (Composite video) Sync tip clamp input	
9 11 16 18	GND	Ground	

Pin no.	Pin name	Function	Internal equivalent circuit diagram
13 15 17	$Y_{IN}1$ $Y_{IN}2$ $Y_{IN}3/V_{IN}4$	Video signal input (Y) Sync tip clamp input	
14	0dB/6dB	0dB/6dB control select	
19 20 21	Y/V_{OUT} V_{OUT} C_{OUT}	Signal output	
22 23 24	CTRL1 CTRL2 CTRL3	Control select	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	–65~+150	°C
Operating temperature	T_{OPR}	–40~+85	°C
Supply voltage	$V_{CC\ max.}$	7	V
Allowable loss	Pd	650	mW

Recommended Operating Conditions

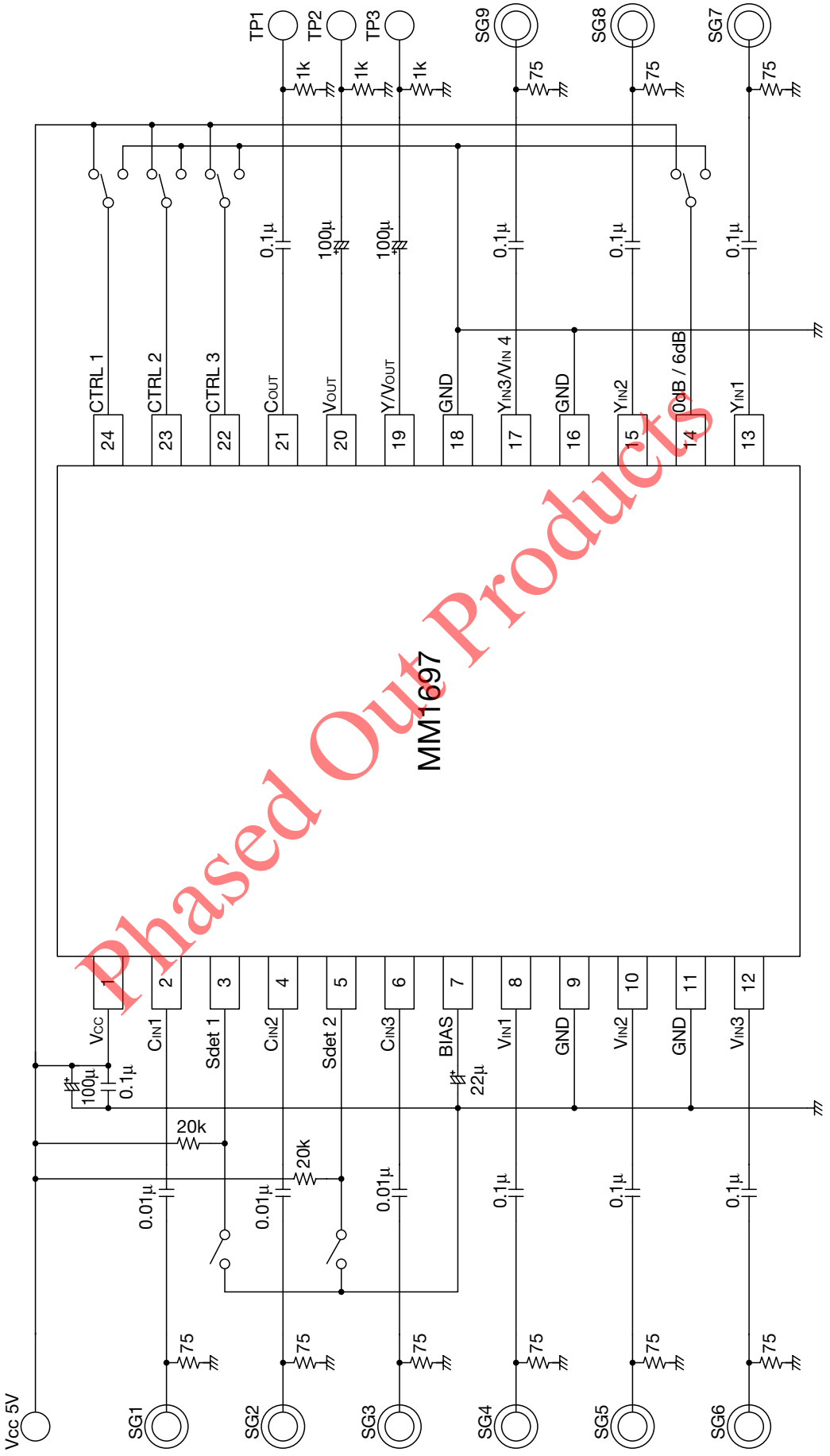
Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	–40~+85	°C
Operating supply voltage	V_{CCOP}	4.5~5.5	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, Vcc=5V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Supply current 1		I_{CC1}	No signal	33	48	63	mA
Supply current 2		I_{CC2}	No signal (at Power saving)	3	5	7	mA
Terminal voltage	Chroma input	$V_{CIN1\sim3}$	2, 4, 6 pin	1.6	2.1	2.6	V
	Composite video input	$V_{VIN1\sim3}$	8, 10, 12pin	1.0	1.5	2.0	V
	Luminance input	$V_{YIN\ 1,\ 2,\ YIN3/VIN4}$	13, 15, 17 pin	1.0	1.5	2.0	V
	Chroma output	V_{COUT}	21 pin	1.6	2.1	2.6	V
	Composite video output	V_{VOUT}	20 pin (14pin=H)	1.0	1.5	2.0	V
			20 pin (14pin=L)	0.4	0.7	1.0	V
	Luminance output	$V_{Y/VOUT}$	19 pin (14pin=H)	1.0	1.5	2.0	V
			19 pin (14pin=L)	0.4	0.7	1.0	V
CTRL terminal threshold voltage		V_{th1}	22, 23, 24 pin	0.7	1.4	2.1	V
0dB/6dB terminal threshold voltage		V_{th2}	14 pin	0.7	1.4	2.1	V
S detect of S det		V_{ths}	3, 5 pin	0.7	1.4	2.1	V
Input impedance		$Z_{CIN\ 1\sim3}$	2, 4, 6 pin	100	150	200	kΩ
Output force current		I_{OUT1}	19, 20, 21 pin	4	5		mA
Output sink current		I_{OUT2}	19, 20, 21 pin	2.5	3		mA
Voltage gain		$G1_{COUT,\ VOUT,\ Y/VOUT}$	SIN wave: 1V f=100kHz	–0.5	0	0.5	dB
		$G2_{COUT,\ VOUT,\ Y/VOUT}$		5.7	6.0	6.3	dB
Frequency characteristic		$f1_{COUT,\ VOUT,\ Y/VOUT}$	SIN wave: 1V –3dB Bandwidth	6.0	6.6		MHz
		$f2_{COUT,\ Y/VOUT}$	SIN wave: 1V 10.74MHz/100kHz		–33	–30	dB
		$f3_{COUT,\ Y/VOUT}$	SIN wave: 1V 13.5MHz/100kHz		–40	–37	dB
		$f4_{COUT,\ Y/VOUT}$	SIN wave: 1V 27MHz/100kHz		–40	–35	dB
Group delay		$tGD_{(COUT,\ Y/VOUT)}$	at 100kHz		85	120	ns

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Group delay deviation		⊿tGD (COUT, Y/VOUT)	to 3.58MHz		15	30	ns
			to 4.43MHz		25	40	ns
Between channel group delay deviation		⊿tchGD	Between C and Y at 4.43MHz		2	20	ns
Differential gain		DGVOUT, Y/VOUT	Staircase signal 1V		0.8	1.5	%
Differential phase		DPVOUT, Y/VOUT	Staircase signal 1V		0.8	1.5	°
Input dynamic range		DRCIN	Measure input terminal when sin wave: 100kHz THD=1.0% of output terminal (14pin=H)	1.4	2.5		V
		DRVIN		1.4	2.5		V
		DRY/VIN		1.4	2.5		V
		DRCIN	Measure input terminal when sin wave: 100kHz THD=1.0% of output terminal (14pin=L)	1.4	1.5		V
		DRVIN		1.4	1.5		V
		DRY/VIN		1.4	1.5		V
Crosstalk	COUT	CTCOUT	Crosstalk to the non-input root. VIN=1V, f=4.43MHz		–60	–50	dB
	VOUT	CTVOUT					
	Y/VOUT	CTY/VOUT					
S/N		SNCOUT, Y/VOUT	BW: 100k~6MHz		70		dB

Measuring Circuit



Switch Control Table

Input select

When not using a Sdet terminal

CTRL1	CTRL2	CTRL3	S det1	S det2	VOUT	Y/VOUT	COUT
L	L	*	H	H	Mute	Mute	Mute
L	H	H			VIN1	VIN1	Mute
		L			CIN1+YIN1	YIN1	CIN1
H	L	H			VIN2	VIN2	Mute
		L			CIN2+YIN2	YIN2	CIN2
H	H	H			VIN3	VIN3	Mute
		L			CIN3+YIN3	YIN3	CIN3

When using a Sdet terminal

CTRL1	CTRL2	CTRL3	S det1	S det2	VOUT	Y/VOUT	COUT
L	L	*	*	*	Mute	Mute	Mute
L	H	H	H	*	VIN1	VIN1	Mute
		*	L	*	CIN1+YIN1	YIN1	CIN1
		L	*	*			
H	L	H	*	H	VIN2	VIN2	Mute
		*	*	L	CIN2+YIN2	YIN2	CIN2
		L	*	*			
H	H	H	*	*	VIN3	VIN3	Mute
		L	*	*	CIN3+YIN3	YIN3	CIN3

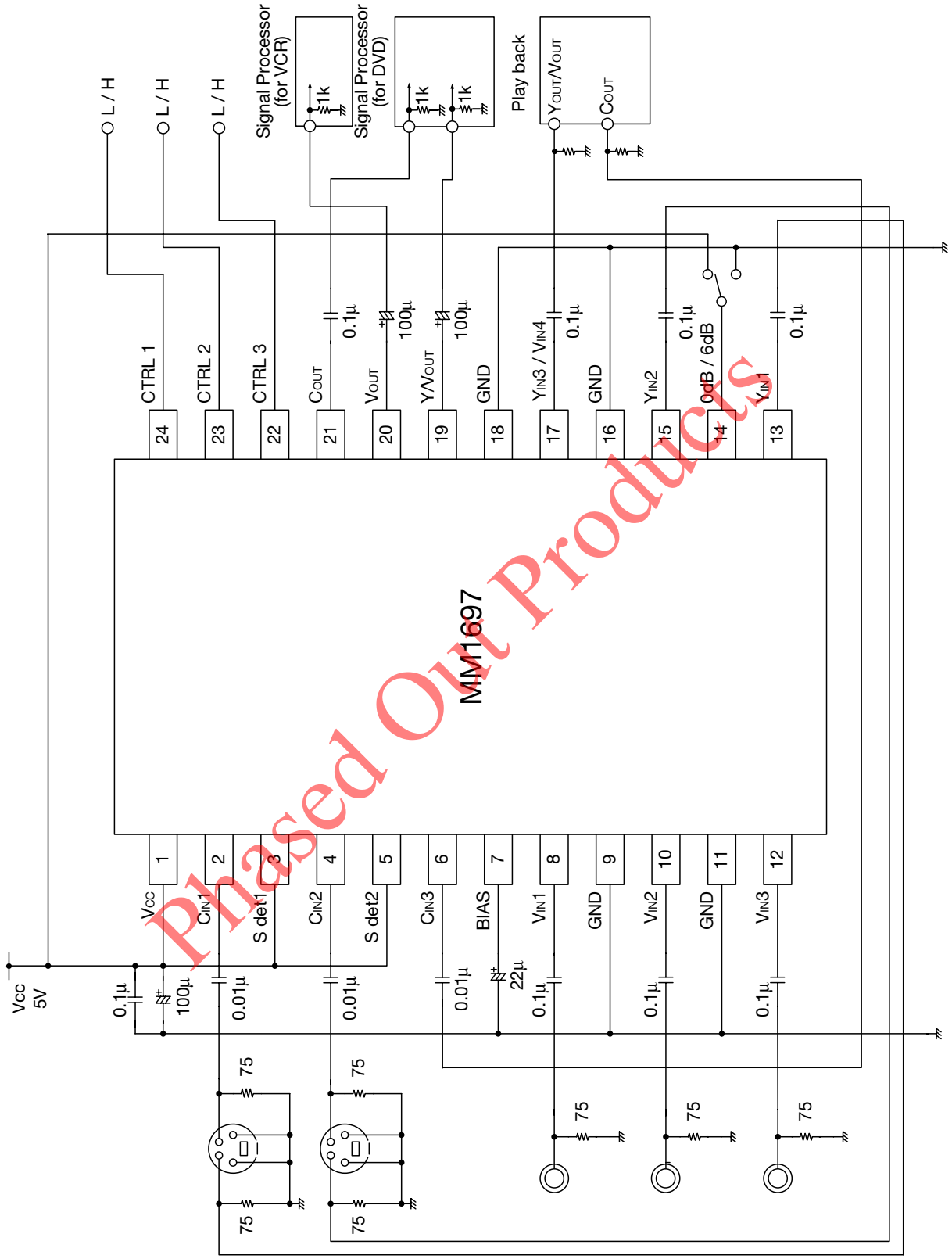
Note: When a Sdet terminal is not used, all mode can be controlled with only a CTRL terminal by making it Sdet1 and 2= H (VCC).
When a Sdet terminal is used, please attach the pull-up resistor of 20kΩ to Sdet1, Sdet2 terminal (3pin, 5pin).
*: Don't care

Gain select

0dB/6dB	GCOUT, VOUT, Y/VOUT
H	0dB
L	6dB

Application Circuit

S det terminal At the time of intact

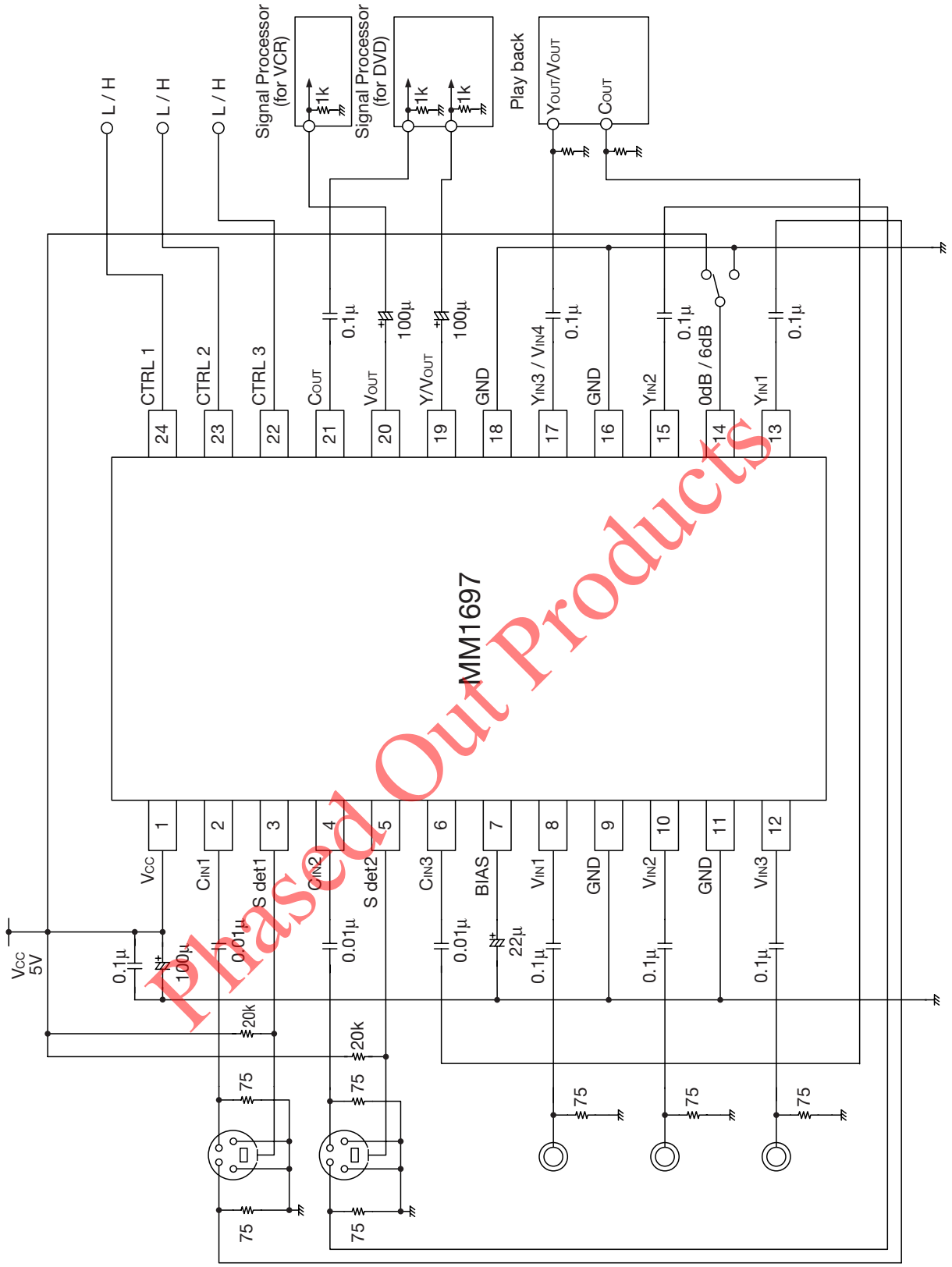


Note Please connect Sdet terminal to Vcc for the measure against a cross talk, when you do not use Sdet terminal. (3, 5pin)

· We shall not be liable for any trouble or damage caused by using this circuit.

· In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.

S det terminal At the time of use



Note Please arrange power supply bypass capacitor near the V_{CC} terminal (1pin).
Please attach the pull up resistor of 20kΩ to Sdet1, Sdet2 terminal (3pin, 5pin)

· We shall not be liable for any trouble or damage caused by using this circuit.
· In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.