HD-Compatible Video Driver IC
Monolithic IC MM1757 Series

April 28, 2009

Outline

This IC is a two-channel 75Ω video driver IC supporting HD (720p/D4, 1080i/D3). It provides the input and output for composite video (V), S-Video (Y, C), and Y color difference (CY, Cb, Cr) (only Y color difference input/output is HD-compatible). It supports both single and dual power supplies. If a single power supply is used, a sag correction circuit can reduce output capacitance, while no output capacitance is required if a dual power supply is used. It also includes an LPF (VCVS Butterworth) required after D/A conversion, D-terminal identification signal (line 1 - line 3) and S-terminal identification signal (S1, S2) output functions, which is ideal as an output driver for Hi-Vision (HD) signal output equipment such as set-top boxes (STBs) and DVD, Blu-ray recorders.

Features

1. Supports the Hi-Vision signal
2. Supports single power supplies and dual power supplies
3. Includes a VCVS Butterworth LPF
4. Includes D-terminal identification signal (line 1 - line 3) and S-terminal identification signal (S1, S2) output functions (F rank)
5. Two types of IC control methods are available; I^2C bus control and DC control with a control pin (F rank)

Item \ Model	MM1757DH	MM1757EH	MM1757FH
Input/Output terminal	CY/Cb/Cr, CVBS, Y/C		
Power supply	Dual/Single	Single	Dual/Single
Output coupling capacitor	○/×	×	○/×
D Terminal	×	×	○
HD/SD switch	○	○	○
I^2C Bus control	×	×	○
Clamp/Bias switch	×	○	○
CVBS/Y/C (Bus bandwidth/Stop Bus bandwidth)	6.75MHz/27MHz		
CY/Cb/Cr-SD (Bus bandwidth/Stop Bus bandwidth)	13.5MHz/54MHz		
CY/Cb/Cr-HD (Bus bandwidth/Stop Bus bandwidth)	37MHz/148MHz	30MHz/74MHz	30MHz/74MHz
Packages	HSOP-28	HSOP-28	HSOP-36

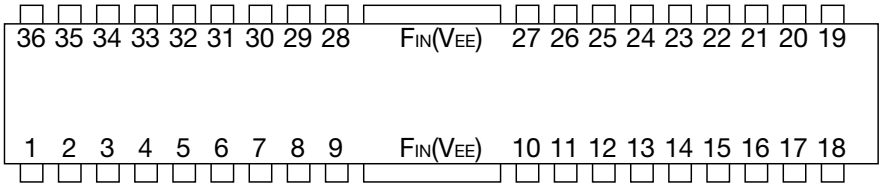
Packages

1. HSOP-28 (D, E rank)
2. HSOP-36 (F rank)

Applications

1. STB
2. DVD, Blu-ray Recorder

Pin Assignment

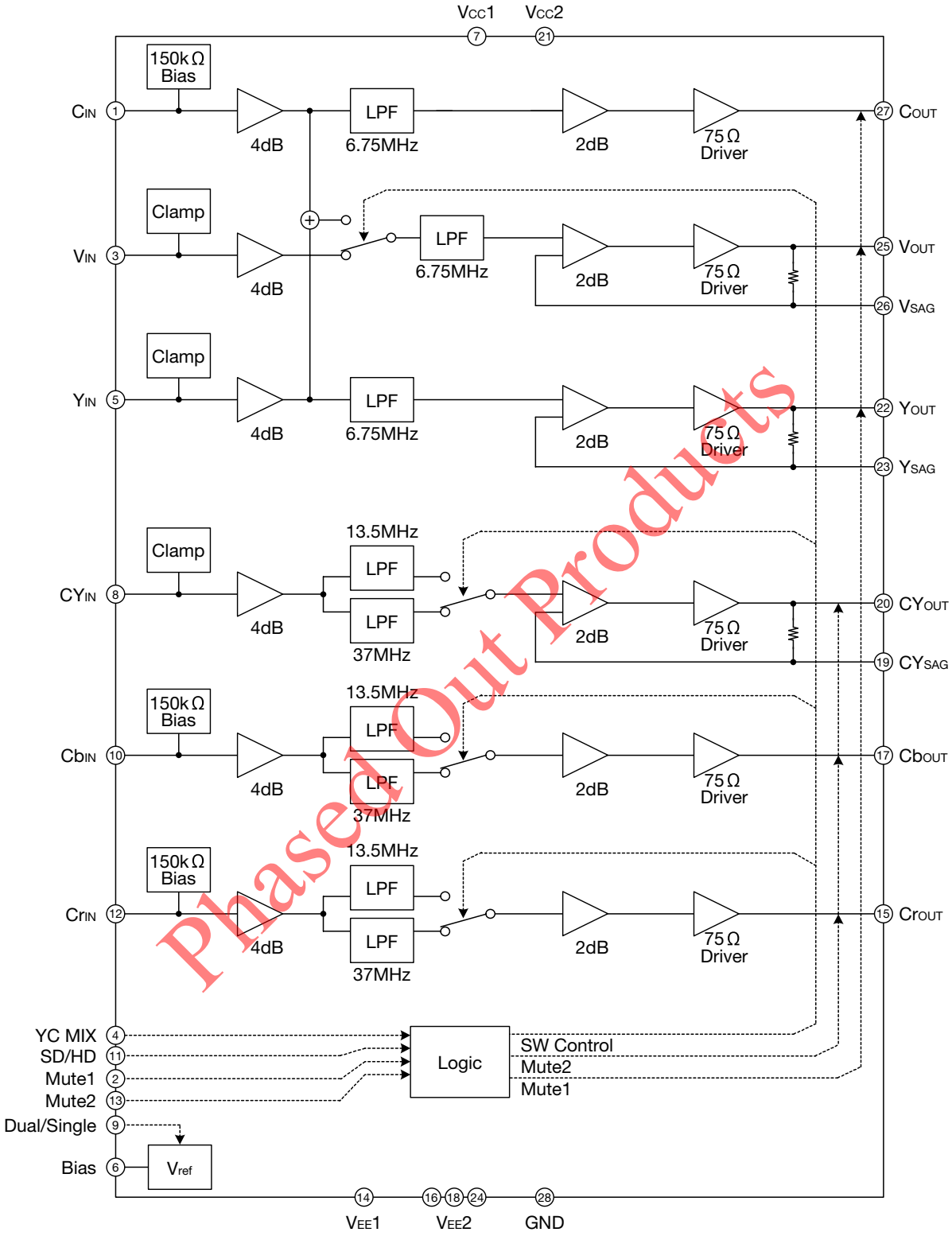


HSOP-36A
(TOP VIEW)

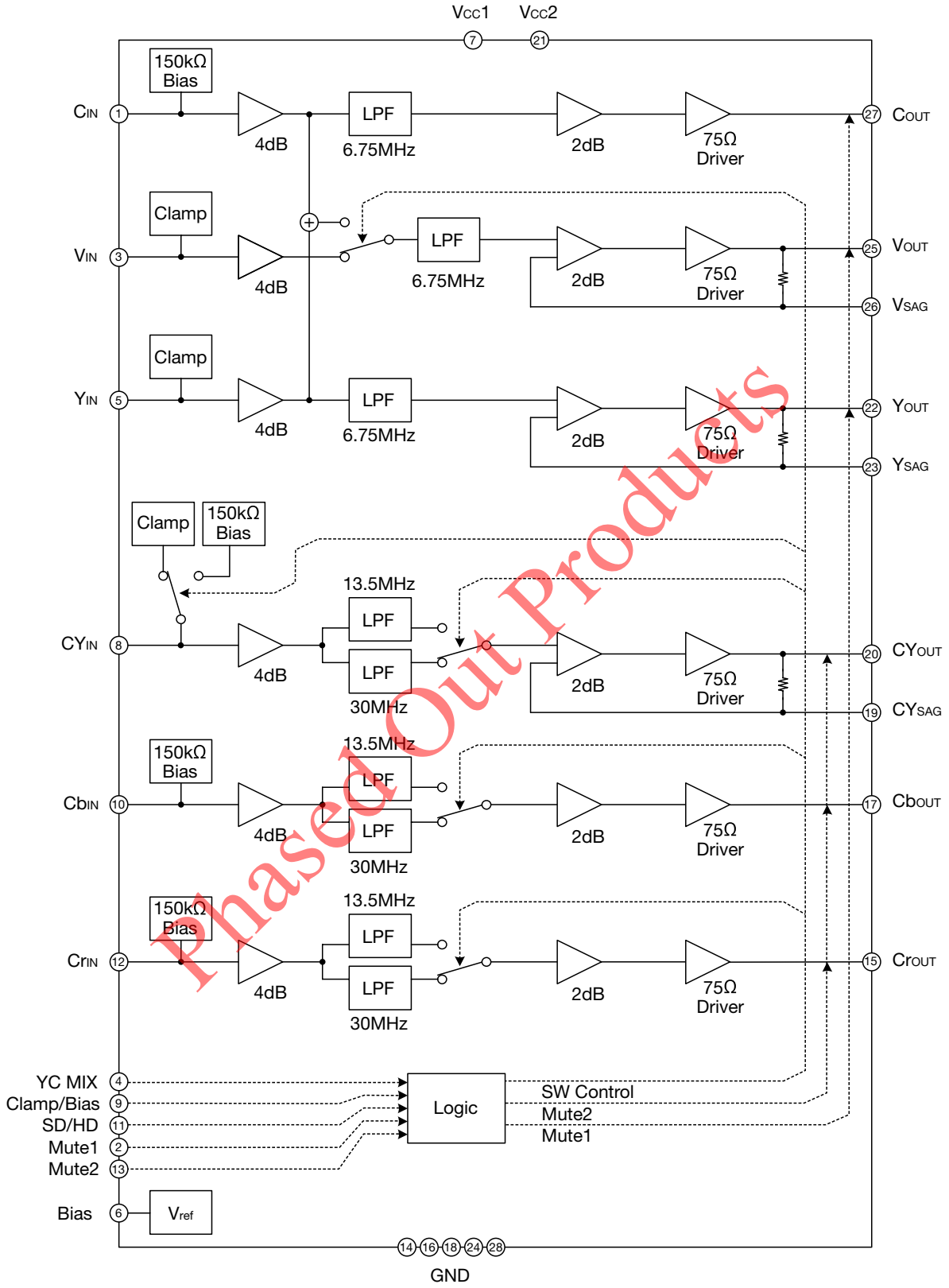
1	CIN	11	VCC1	21	VEE2	31	VEE2
2	Mute1	12	CYIN	22	CbOUT	32	VOUT
3	VIN	13	Clamp/Bias	23	Line2 out	33	VSAG
4	YC MIX	14	CbIN	24	VEE2	34	COUT
5	YIN	15	SD/HD	25	CYSAG	35	S1/S2 out
6	Dual/Single	16	CrIN	26	CYOUT	36	GND
7	Bias	17	Mute2	27	Line1 out		
8	SCL	18	VEE1	28	VCC2		
9	SDA	19	CrOUT	29	YOUT		
10	Address	20	Line3 out	30	YSAG		

Block Diagram

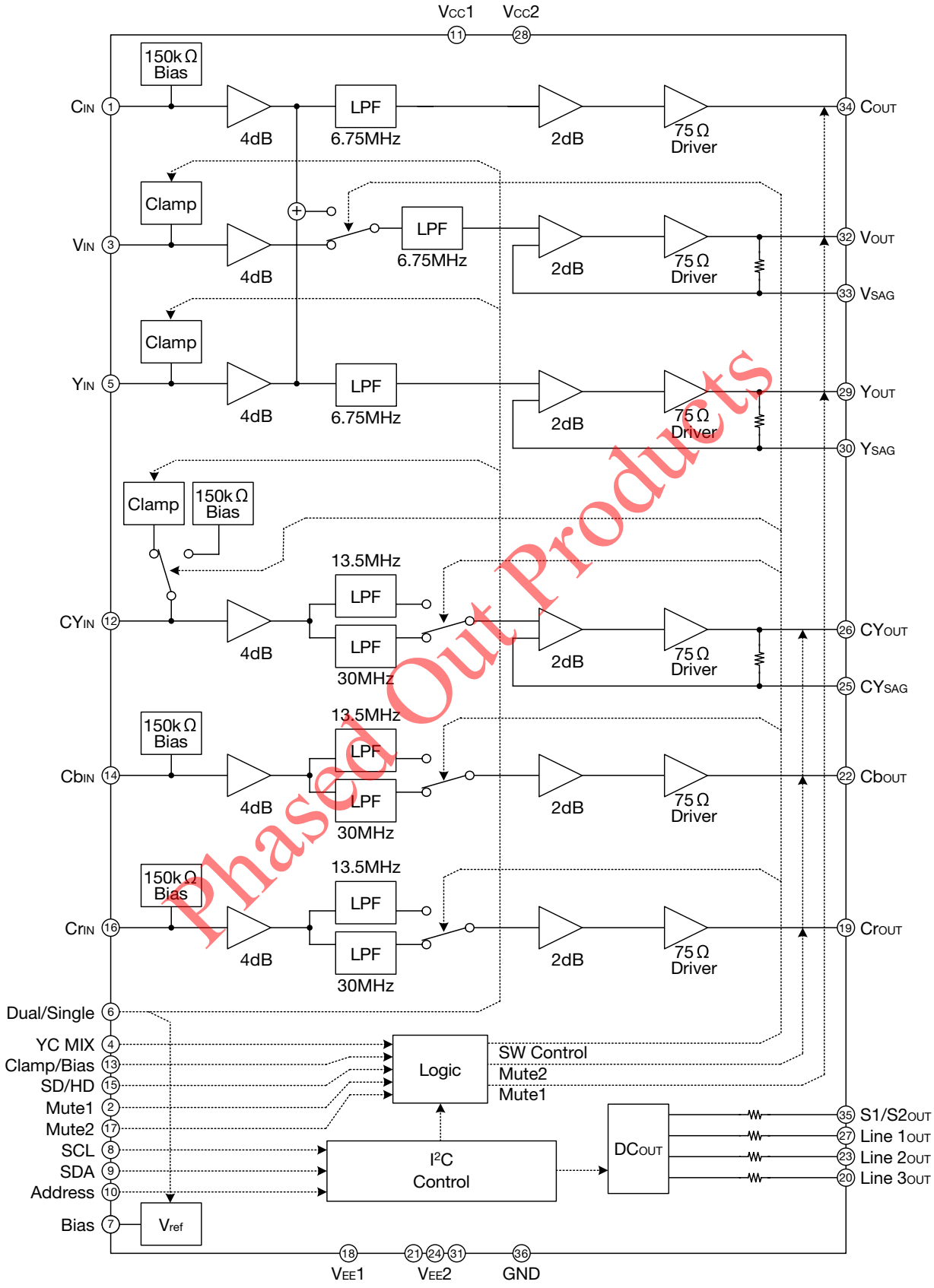
D rank



E rank

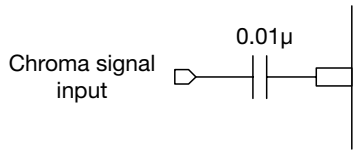


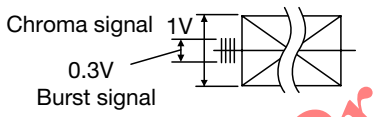
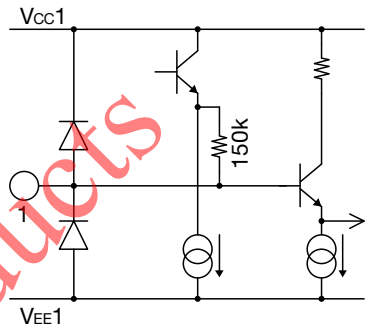
F rank



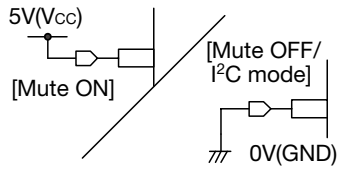
Pin Description (F rank)

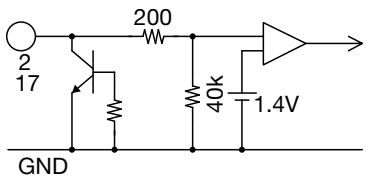
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">1</td><td rowspan="4">CIN</td><td>Function
Chroma Signal Input
Pin to input chrominance signals of S-video. Bias input pin.

Pin voltage: 2.5V typ. [at Single mode]
Input impedance: 150kΩ typ.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

when not using it : Open
Input signal
 
</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td rowspan="4">2
17</td><td rowspan="4">Mute1
Mute2</td><td>Function
Mute select
Select mute ON/OFF with a voltage applied to this pin.
Mute1 controls C/V/Y.
Mute2 controls CY/Cb/Cr.

To select mute ON/OFF, I²C BUS can be also used.
* See section Switch Control Table.

Threshold : 1.4V typ.
Input impedance : 40kΩ typ.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

when not using it : Open
Input signal
DC Voltage : 0V(GND) to 5V(VCC)</td><td>Equivalent circuit diagram
 
</td></tr>
</table>

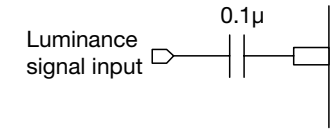
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">3</td><td rowspan="4">V_{IN}</td><td>Function</td></tr>
<tr><td>Composite Video Signal Input
Pin to input composite video signals.
Clamp input pin.

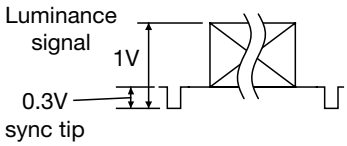
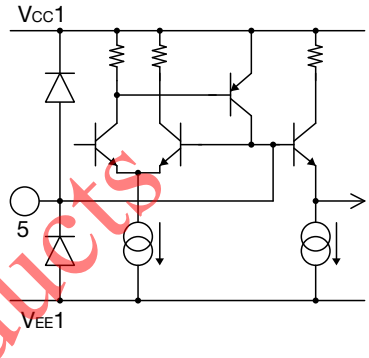
Pin voltage : 1.4V typ. [at Single mode]</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>SDTV Composite video signal input
0.1µ
when not using it : Open
Input signal
SDTV Composite video signal
1V
0.3V
sync tip
Vcc1
3
VEE1</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">YC MIX</td><td>Function</td></tr>
<tr><td>YC MIX select
Select MIX mode/V through mode with a voltage applied to this pin.

To select YC MIX, I²C BUS can be also used.
* See section Switch Control Table.

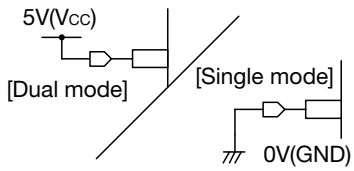
Threshold : 1.4V typ.
Input impedance : 40kΩ typ.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>5V(Vcc)
[YC MIX]
[V Through/ I²C mode]
0V(GND)
when not using it : Open
Input signal
DC Voltage : 0V(GND) to 5V(Vcc)
4
200
40k
1.4V
GND</td></tr>
</table>

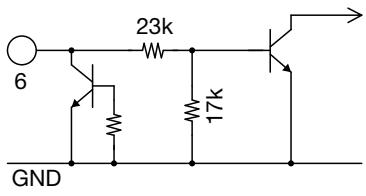
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">5</td><td rowspan="4">Y_{IN}</td><td>Function
Luminance Signal Input
Pin to input luminance signals of S-video.
Clamp input pin.

Pin voltage : 1.4V typ. [at Single mode]</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

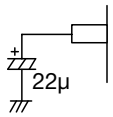
when not using it : Open
Input signal
 
</td></tr>
<tr><td>Equivalent circuit diagram</td></tr>
<tr><td> 
</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">Dual/Single</td><td>Function
Dual/Single Power Supply select
Select (a) type of (a) power supply (single supply/dual power supplies) with a voltage applied to this pin.
Single mode : V_{CC} = 5V typ. , V_{EE} = GND
Dual mode : V_{CC} = 5V typ. , V_{EE} = –3V typ.

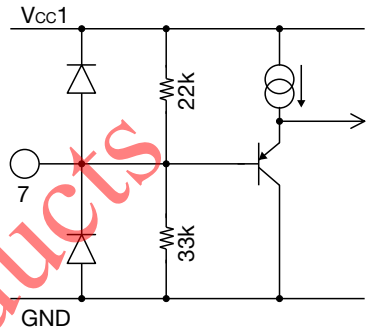
* See section Switch Control Table.

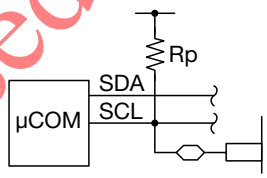
Threshold : 1.7V typ.
Input impedance : 40kΩ typ.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

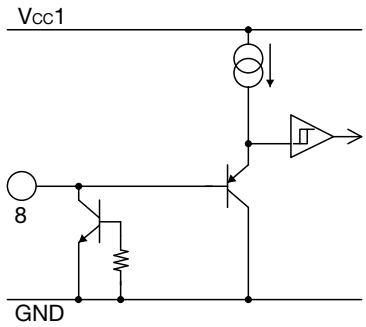
Input signal
DC Voltage : 0V(GND) to 5V(Vcc)</td></tr>
<tr><td>Equivalent circuit diagram</td></tr>
<tr><td> 
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">7</td><td rowspan="4">Bias</td><td>Function</td></tr>
<tr><td>Bias
All the reference voltages used inside the IC are produced according to the resistance divider of this pin.
Pin to stabilize reference voltages, and reduce both power supply ripple and cross talk by decreasing impedance with an external 22µF.

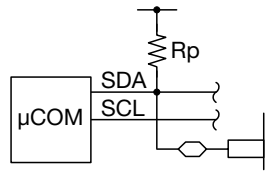
Input Impedance : 13kΩ typ.</td></tr>
<tr><td>External circuit
 

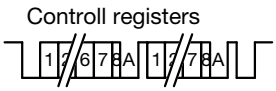
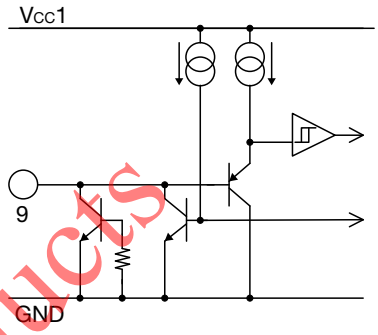
when not using it : Open
Input signal
—</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td rowspan="4">8</td><td rowspan="4">SCL</td><td>Function</td></tr>
<tr><td>Clock Input of I²C BUS
Pin to control the IC with I²C BUS along with SDA (9pin)
Address (10pin) is used to select an address.

* See section I²C BUS.</td></tr>
<tr><td>External circuit
 

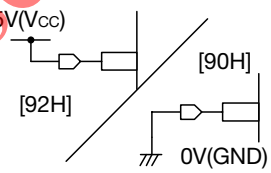
when not using it : Open
Input signal
Clock signal
 
</td><td>Equivalent circuit diagram
 
</td></tr>
</table>

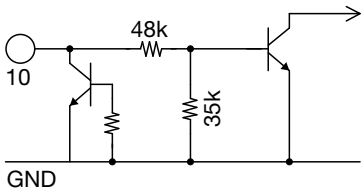
<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="4">9</td><td rowspan="4">SDA</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">DATA Input of I²C BUS
Pin to control the IC with I²C BUS along with SCL (8pin).
The Address pin (10pin) is used to select an address.

* See section I²C BUS.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

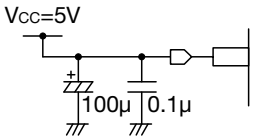
when not using it : Open
Input signal
 
</td><td> 
</td></tr>
<tr><td rowspan="4">10</td><td rowspan="4">Address</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Slave Address select
Select an I²C slave address 90H/92H with a voltage applied to this pin.

* See section I²C BUS.

Threshold : 1.7V typ.
Input impedance : 83kΩ typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

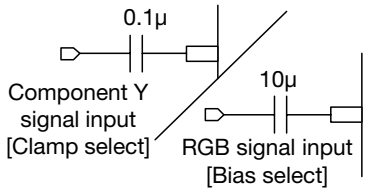
when not using it : Open
Input signal
DC Voltage : 0V(GND) to 5V(Vcc)</td><td> 
</td></tr>
</table>

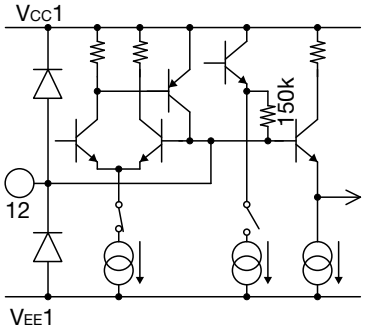
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>11
28</td><td>Vcc1
Vcc2</td><td>
Function
Positive Voltage Supply
Pin to apply a positive supply voltage. Apply 5V.
11pin and 28pin are not shorted inside the IC.
Vcc2 is connected to an output stage circuit, and Vcc1 is connected to a circuit other than an output stage circuit.

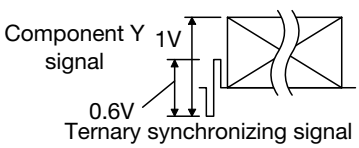
Note : Please be sure to short-circuit Vcc1 and Vcc2 externally.
Note : When using dual power supplies,
after VEE1 and VEE2 or simultaneously, turn on Vcc1 and Vcc2.
Note : Please arrange power supply bypass capacitor near the terminal.
External circuit


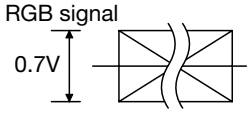
Equivalent circuit diagram
—
Input signal
DC Voltage :
4.5V~5.5V [at Single mode]
4.7V~5.3V [at Dual mode]
</td></tr>
<tr><td>12</td><td>CYIN</td><td>
Function
Component Y Signal Input or RGB Signal Input
Pin to input component Y signals or RGB signals
Select an input type (clamp/bias) with the Clamp/Bias pin (13pin) or I²C BUS.

Note : As shown below, select an external input capacitance corresponding to an input type (clamp/bias).

Pin voltage : 1.4V typ. [Clamp] [at Single mode]
or 2.5V typ. [Bias] [at Single mode]
Input impedance : 150kΩ [Bias]
External circuit


when not using it : Open
Equivalent circuit diagram


Input signal


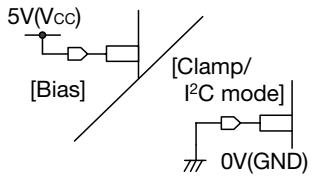


</td></tr>
</table>

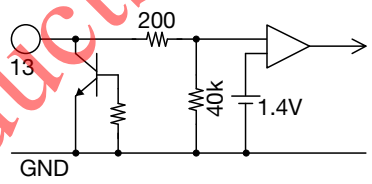
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">13</td><td rowspan="2">Clamp/Bias</td><td>
Function
Clamp/Bias select
Select an input type (clamp/bias) of CY_{IN} (12pin) with a voltage applied to this pin.

To select clamp or bias, I²C BUS can be also used.
∗See section Switch Control Table.

Threshold : 1.4V typ.
Input impedance : 40kΩ typ.

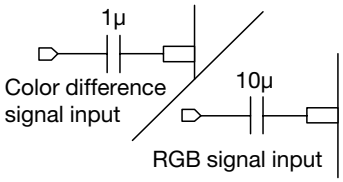
External circuit


when not using it : Open

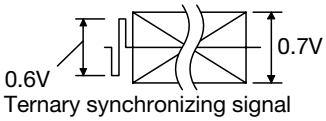
Input signal
DC Voltage : 0V(GND) to 5V(Vcc)
</td><td>
Equivalent circuit diagram


</td></tr>
<tr><td colspan="2">
Function
Color Difference Signal Cb Input or RGB Signal Input
Pin to input color difference signals Cb or RGB signals.
Bias input pin.

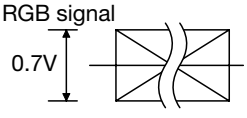
Pin voltage : 2.5V typ. [at Single mode]
Input impedance : 150kΩ typ.

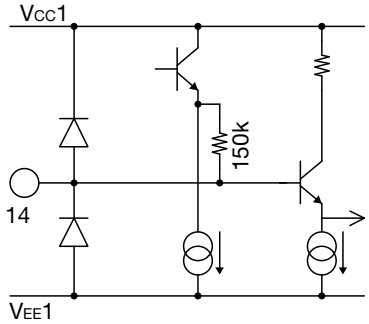
External circuit


when not using it : Open

Input signal
Color difference signal


Ternary synchronizing signal

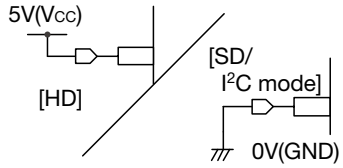
RGB signal


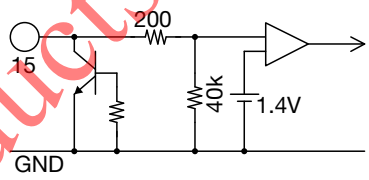
</td><td>
Equivalent circuit diagram


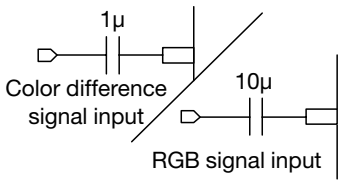
</td></tr>
<tr><td>14</td><td>CbIN</td><td></td><td></td></tr>
</table>

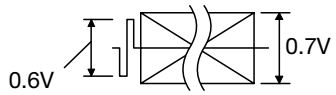
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">15</td><td rowspan="4">SD/HD</td><td>Function</td></tr>
<tr><td>LPF select
Select a cutoff frequency of LPF (CY/Cb/Cr) with a voltage applied to this pin.
(SD : pass bandwidth 13.5MHz / HD : pass bandwidth 30MHz)

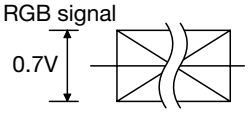
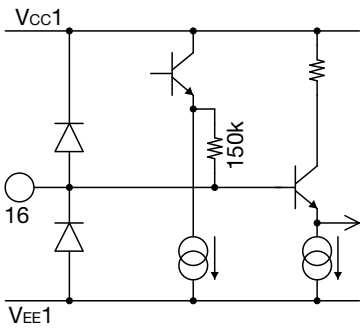
To select LPF, I²C BUS can be also used.
* See section Switch Control Table.

Threshold : 1.4V typ.
Input impedance : 40kΩ typ.</td></tr>
<tr><td>External circuit
 

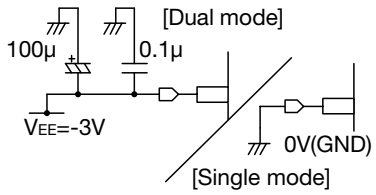
when not using it : Open</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td>Input signal
DC Voltage : 0V(GND) to 5V(Vcc)</td><td></td></tr>
<tr><td rowspan="4">16</td><td rowspan="4">CrIN</td><td>Function</td></tr>
<tr><td>Color Difference Signal Cr Input or RGB Signal Input
Pin to input color difference signals Cr or RGB signals.
Bias input pin.

Pin voltage : 2.5V typ. [at Single mode]
Input impedance : 150kΩ typ.</td></tr>
<tr><td>External circuit
 

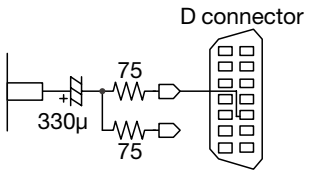
when not using it : Open
Input signal
Color difference signal
 

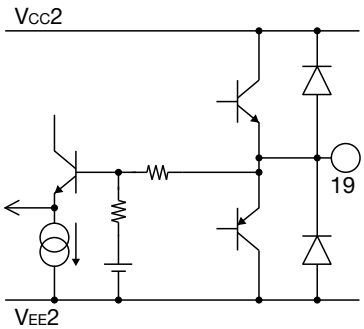
Ternary synchronizing signal
RGB signal
 
</td><td>Equivalent circuit diagram
 
</td></tr>
</table>

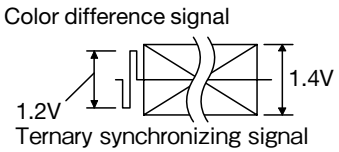
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>18
21
24
31</td><td>VEE1
VEE2
VEE2
VEE2</td><td>
Function
Negative Voltage Supply
Pin to apply a negative supply voltage.
Connect to GND when using a single power supply.
Apply –3V when using dual power supplies.
18pin is not shorted to 21pin, 24pin, or 31pin inside the IC.
21pin, 24pin and 31pin are shorted inside the IC.
VEE2 is connected to an output stage circuit, and VEE1 is connected to a circuit other than an output stage circuit.

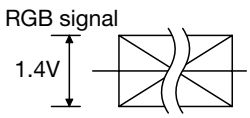
Note : Please arrange power supply bypass capacitor near the terminal when using dual power supplies.
External circuit


Equivalent circuit diagram
—
Input signal
DC Voltage :
GND [at Single mode]
–3.3V~ –2.7V [at Dual mode]
</td></tr>
<tr><td>19</td><td>CROUT</td><td>
Function
Color Difference Signal Cr Output or RGB Signal Output
Pin to output color difference signals Cr or RGB signals.
Bias output pin.

Pin voltage: 2.4V typ. [at Single mode] or 0V typ. [at Dual mode]
Output dynamic range: 3.0VP-P typ.
* See section Pin Description Supplemental. 2, 3
External circuit


when not using it : Open
Equivalent circuit diagram


Input signal




</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">20</td><td rowspan="4">Line3 out</td><td>Function</td></tr>
<tr><td>Line3 Output
Pin to output Line3 of D connector detect signal
The output DC voltage is controlled with I²C BUS.

* See section Switch Control Table.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>D connector
10k
10k
when not using it : Open
Input signal
DC Voltage : 0V typ.
or 2.1V typ.
or 4.6V typ.

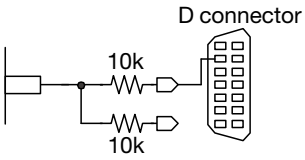
Vcc1
20
GND</td></tr>
<tr><td rowspan="5">22</td><td rowspan="5">Cbout</td><td>Function</td></tr>
<tr><td>Color Difference Signal Cb Output or RGB Signal Output
Pin to output color difference signals Cb or RGB signals.
Bias output pin.

Pin voltage : 2.4V typ. [at Single mode] or 0V typ. [at Dual mode]
Output dynamic range : 3.0V_{P-P} typ.

* See section Pin Description Supplemental. 2, 3</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>D connector
75
330µ
75
when not using it : Open
Input signal
Color difference signal
1.4V
1.2V
Ternary synchronizing signal

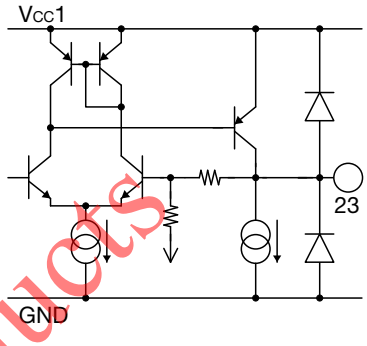
RGB signal
1.4V</td><td>Vcc2
22
VEE2</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">23</td><td rowspan="4">Line2 out</td><td>Function</td></tr>
<tr><td>Line2 Output
Pin to output Line2 of D connector detect signal.
The output DC voltage is controlled with I²C BUS.

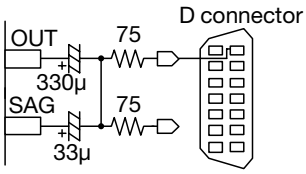
* See section Switch Control Table.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

when not using it : Open

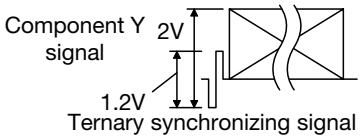
Input signal
DC Voltage : 0V typ.
or 4.6V typ.

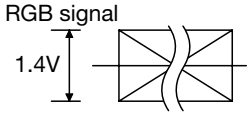
Equivalent circuit diagram:
 
</td></tr>
<tr><td rowspan="4">25
26</td><td rowspan="4">CYSAG
CYOUT</td><td>Function</td></tr>
<tr><td>Component Y Signal Output or RGB Signal Output
Pin to output component Y signals or RGB signals
Select an output type (clamp/bias) with the Clamp/Bias pin (13pin) or I²C BUS.

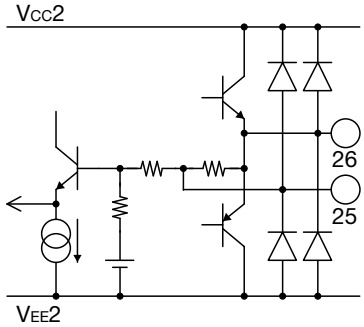
Pin voltage : 1.1V typ. [Clamp] [at Single mode]
or 2.4V typ. [Bias] [at Single mode]
or 0V typ. [at Dual mode]
Output dynamic range : 2.8Vp-p typ. [Clamp]
or 3.0Vp-p typ. [Bias]

* See section Pin Description Supplemental. 2, 3</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

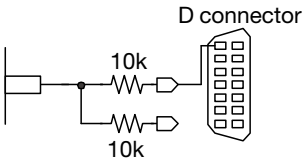
when not using it : Open

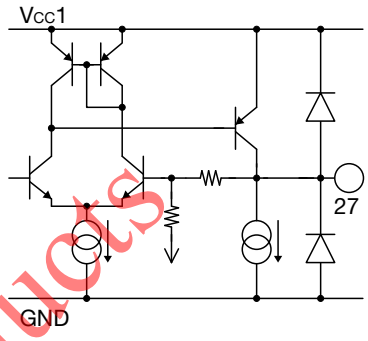
Input signal
 

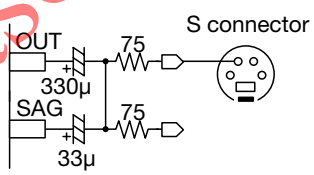
Equivalent circuit diagram:
 
</td></tr>
</table>

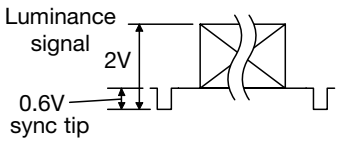
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">27</td><td rowspan="4">Line1 out</td><td>Function</td></tr>
<tr><td>Line1 Output
Pin to output Line1 of D connector detect signal.
The output DC voltage is controlled with I²C BUS.

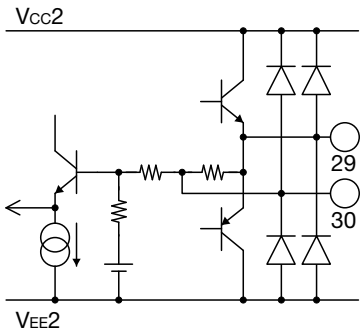
* See section Switch Control Table.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

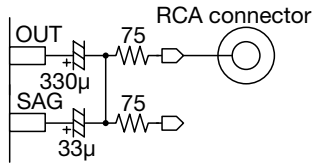
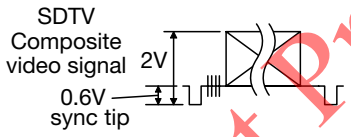
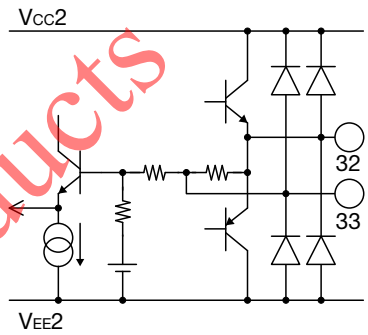
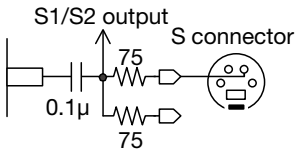
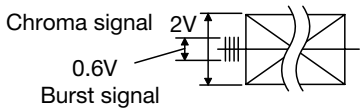
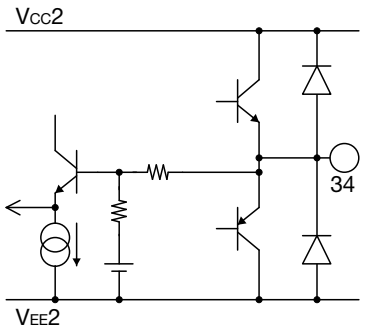
when not using it : Open
Input signal
DC Voltage : 0V typ.
or 2.1V typ.
or 4.6V typ.
Equivalent circuit diagram:
 
</td></tr>
<tr><td rowspan="4">29
30</td><td rowspan="4">YOUT
YSAG</td><td>Function</td></tr>
<tr><td>Luminance Signal Output
Pin to output luminance signals of S-video.
Clamp output pin.

Pin voltage : 1.1V typ. [at Single mode] or 0V typ. [at Dual mode]
Output dynamic range : 2.8VP-P typ.

* See section Pin Description Supplemental. 2, 3</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

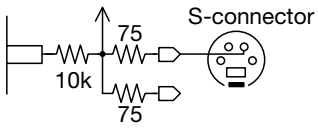
when not using it : Open
Input signal
 

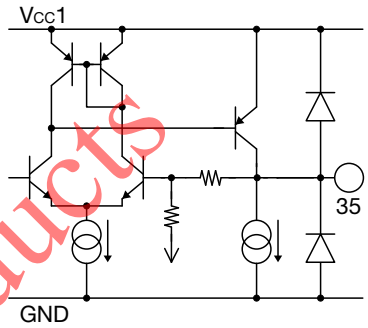
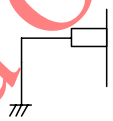
Equivalent circuit diagram:
 
</td></tr>
</table>

Pin No.	Pin name	Pin description
32 33	V_{OUT} V_{SAG}	**Function** Composite Video Signal Output Pin to output composite video signals. Clamp output pin. Pin voltage : 1.1V typ. [at Single mode] or 0V typ. [at Dual mode] Output dynamic range : 2.8V_{P-P} typ. * See section Pin Description Supplemental. 2, 3 **External circuit**  when not using it : Open **Input signal**  **Equivalent circuit diagram** 
34	C_{OUT}	**Function** Chroma Signal Output Pin to output Chrominance signals of S-video. Bias output pin. Pin voltage : 2.4V typ. [at Single mode] or 0V typ. [at Dual mode] Output dynamic range : 3.0V_{P-P} typ. * See section Pin Description Supplemental. 2, 3 **External circuit**  when not using it : Open **Input signal**  **Equivalent circuit diagram** 

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">35</td><td rowspan="4">S1/S2 out</td><td>Function</td></tr>
<tr><td>S1/S2 Output
Pin to output S1/S2 of S-connector detect signal.
The output DC voltage is controlled with I²C BUS.

* See section Switch Control Table.

Output Impedance : 200Ω typ.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>Chroma signal output
 

when not using it : Open
 
</td></tr>
<tr><td>Input signal</td></tr>
<tr><td rowspan="4">36</td><td rowspan="4">GND</td><td>Function</td></tr>
<tr><td>Ground
Ground pin.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td> 
Input signal
—
—</td></tr>
</table>

Supplemental 1 : SAG pin

If the SAG pin is not used, the OUT pin and the SAG pin should be shorted.
Then, a coupling capacitance of approx. 1000µF should be used.

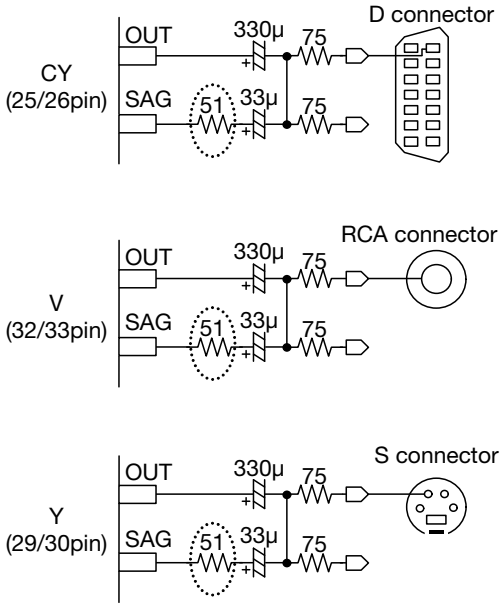
Supplemental 2 : Using dual power supplies

When using dual power supplies, the device level shifts so that the pedestal level outputs with 0±0.1V (no signal : 0±0.1V) if sending a signal of the pedestal level of 0.3V (no signal : 0.3V) to a terminal where the luminance elements of V_{IN}, Y_{IN},and CY_{IN} are received, and sending a signal of the center of 0.6V (no signal : 0.6V) to a terminal where the color elements of C_{IN}, Cb_{IN}, Cr_{IN} are received. Thus, the output coupling capacitance can be eliminated.

Supplemental3 : Wire routing for video output pins

Keep the wire as short as possible between each video output pin and 75Ω.

If using a SAG correction circuit, when wire routing is long, add a resistor as shown below.



Supplemental 4 : D connector discernment signal output pin

Object : S1/S2 out (35pin) , Line1 out (27pin) , Line2 out (23pin) , Line3 out (20pin)

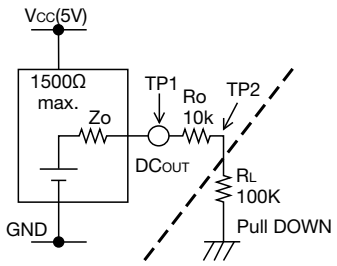
The output impedance of these terminals of MM1757FH is 1500Ω max. (Refer to electrical characteristics) .

There is a case where D connector specification (CP-4120) is not fulfilled depending on the state of connection apparatus.

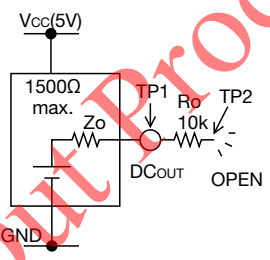
In this case, please adjust the value of the external series resistance R_O.

D connector discernment signal line specifications			The example of Output Voltage (R_O=10kΩ , R_L=Open or 100kΩ)						
Discernment voltage		Tolerance	Pull DOWN (Normal)		OPEN		Pull UP		UNIT
			TP1	TP2	TP1	TP2	TP1	TP2	
H	5.0	0 −1.5	4.82	4.38	4.84	4.83	4.84	4.85	V
M	2.2	+0.2 −0.8	2.19	1.99	2.19	2.19	2.19	**2.45**	V
L	0		0	0	0	0	0.03	0.48	V

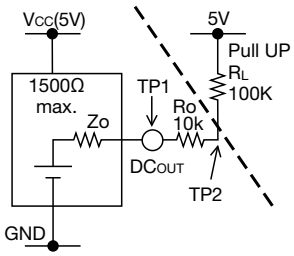
Measurement circuit diagram ＊TP=Test Point



Pull DOWN (Normal)

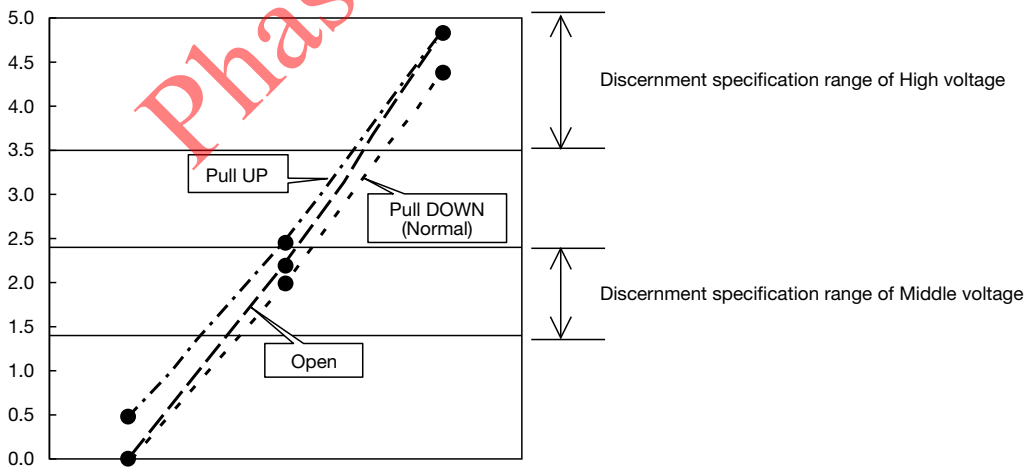


Open



Pull UP

Graph Output voltage TP2



Absolute Maximum Ratings (at the single power supply , except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}_s	−55~+150	°C
Operating temperature	T_{OPR}_s	−40~+85	°C
Supply voltage	$V_{CC\ max.}$_s	6	V
Allowable loss (Note1)	Pd_s	2.6	W

Note1 : Board mounting allowable loss. Board size 100 × 100 × 1.6mm

Absolute Maximum Ratings (at the dual power supply, except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}_d	−55~+150	°C
Operating temperature	T_{OPR}_d	−40~+85	°C
Positive supply voltage	$V_{CC\ max.}$_d	6	V
Negative supply voltage	$V_{EE\ max.}$_d	−4	V
Allowable loss (Note2)	Pd_d	2.6	W

Note2 : Board mounting allowable loss. Board size 100 × 100 × 1.6mm

Recommended Operating Conditions (at the single power supply)

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}_s	−40~+85	°C
Operating voltage	V_{CCOP}_s	4.5~5.5	V

Recommended Operating Conditions (at the dual power supply)

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}_d	−40~+75	°C
Positive operating voltage	V_{CCOP}_d	4.7~5.3	V
Negative operating voltage	V_{EEOP}_d	−2.7~−3.3	V

Electrical Characteristics (at the single power supply, except where noted otherwise, Ta=25°C, V_{CC}=5V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Supply current 1		I_{CC1_s}	No signal	87	125	162	mA
Supply current 2		I_{CC2_s}	No signal, Mute1 : ON	66	95	123	mA
Supply current 3		I_{CC3_s}	No signal, Mute2 : ON	35	50	65	mA
Supply current 4		I_{CC4_s}	No signal, Mute1 and Mute2 : ON	6	9	12	mA
Terminal voltage	Chroma input	V_{CIN_s}	1pin	2.0	2.5	3.0	V
	Composite video input	V_{VIN_s}	3pin	1.2	1.4	1.6	V
	Luminance input	V_{YIN}, C_{YIN_s}	5, 12pin	1.2	1.4	1.6	V
	Component input	V_{CbIN}, C_{RIN_s}	14, 16pin	2.0	2.5	3.0	V
	Chroma output	V_{COUT_s}	34pin		2.4		V
	Composite video output	V_{VOUT_s}	32pin		1.1		V
	Luminance output	V_{YOUT}, C_{YOUT_s}	26, 29pin		1.1		V
	Component output	V_{CbOUT}, C_{ROUT_s}	19, 22pin		2.4		V
Output dynamic range		DR3, 5, 7, 8_s (✶ 6)	SIN wave : 100kHz, THD=1.0%	2.6	3.0		V
		DR1, 2, 4, 6_s (✶ 6)	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V

Electrical Characteristics (at the dual power supply, except where noted otherwise, Ta=25°C, V_{CC}=5V, V_{EE}=-3V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Positive supply current 1		I_{CC1_d}	No signal	87	125	162	mA
Positive supply current 2		I_{CC2_d}	No signal, Mute1 : ON	66	95	123	mA
Positive supply current 3		I_{CC3_d}	No signal, Mute2 : ON	35	50	65	mA
Positive supply current 4		I_{CC4_d}	No signal, Mute1 and Mute2 : ON	6	9	12	mA
Negative supply current 1		I_{EE1_d}	No signal	80	115	150	mA
Negative supply current 2		I_{EE2_d}	No signal, Mute1 : ON	60	85	110	mA
Negative supply current 3		I_{EE3_d}	No signal, Mute2 : ON	28	40	52	mA
Negative supply current 4		I_{EE4_d}	No signal, Mute1 and Mute2 : ON		1	4	mA
Terminal voltage	Chroma output	V_{COUT_d}	34pin (✶ 1)	−0.18	0.0	0.18	V
	Composite video output	V_{VOUT_d}	32pin (✶ 2)	−0.18	0.0	0.18	V
	Luminance output	V_{YOUT}, C_{YOUT_d}	26, 29pin (✶ 3)	−0.18	0.0	0.18	V
	Component output	V_{CbOUT}, C_{ROUT_d}	19, 22pin (✶ 4)	−0.18	0.0	0.18	V
Output dynamic range		DR3, 5, 7, 8_d (✶ 6)	SIN wave : 100kHz, THD=1.0%	3.0			V
		DR1, 2, 4, 6_d (✶ 6)	SIN wave : 100kHz, THD=1.0%	3.0			V

Electrical Characteristics

(Except where noted otherwiseTa=25°C, V_{CC}=5V, V_{EE}=-3V [dual power supply] or V_{CC}=5V [single power supply])

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Control terminal input voltage	High	V_{thHm} (★ 5)	2, 4, 6, 13, 15, 17pin	2.1			V
	Low	V_{thLm} (★ 5)				0.7	V
Control terminal input current	High	I_{IHm} (★ 5)	2, 4, 6, 13, 15, 17pin, V_H=4.5V			160	µA
	Low	I_{ILm} (★ 5)	2, 4, 6, 13, 15, 17pin, V_L=0.4V			15	µA
Address threshold voltage	90H	V_{th90}	10pin			0.8	V
	92H	V_{th92}		2.2			V
S1/S2 out Terminal output voltage	High	V_{SoutH}	R_L=10kΩ+100kΩ	4.3	4.6		V
	Middle	V_{SoutM}	R_L=10kΩ+100kΩ	1.6	2.1	2.4	V
	Low	V_{SoutL}	R_L=10kΩ+100kΩ		0.1	0.5	V
Line1 out Terminal output voltage	High	V_{L1outH}	R_L=10kΩ+100kΩ	4.3	4.6		V
	Middle	V_{L1outM}	R_L=10kΩ+100kΩ	1.6	2.1	2.4	V
	Low	V_{L1outL}	R_L=10kΩ+100kΩ		0.1	0.5	V
Line2 out Terminal output voltage	High	V_{L2outH}	R_L=10kΩ+100kΩ	4.3	4.6		V
	Low	V_{L2outL}	R_L=10kΩ+100kΩ		0.1	0.5	V
Line3 out Terminal output voltage	High	V_{L3outH}	R_L=10kΩ+100kΩ	4.3	4.6		V
	Middle	V_{L3outM}	R_L=10kΩ+100kΩ	1.6	2.1	2.4	V
	Low	V_{L3outL}	R_L=10kΩ+100kΩ		0.1	0.5	V
Input impedance		Z_{CIN}, C_{BIN}, C_{RIN}	1, 14, 16pin	100	150	200	kΩ
Output impedance		Z_{SOUT}, $L1_{OUT}$, $L2_{OUT}$, $L3_{OUT}$	20, 23, 27, 35pin		200		Ω
Voltage gain		G1n (★ 6)	SIN wave : 1V, f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic 1 (C, V, Y)		$f1_{1\sim5}$ (★ 6)	SIN wave : 1V, 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		$f2_{1\sim5}$ (★ 6)	SIN wave : 1V, 27MHz/100kHz		−33	−27	dB
Frequency characteristic 2 (CY, Cb, Cr) at Standard Definition select		$f3_{6\sim8}$ (★ 6)	SIN wave : 1V, 13.5MHz/100kHz	−1.0	0.0	1.0	dB
		$f4_{6\sim8}$ (★ 6)	SIN wave : 1V, 54MHz/100kHz		−33	−27	dB
Frequency characteristic 3 (CY, Cb, Cr) at High Definition select		$f5_{6\sim8}$ (★ 6)	SIN wave : 1V, 30MHz/100kHz	−1.0	0.0	1.0	dB
		$f6_{6\sim8}$ (★ 6)	SIN wave : 1V, 74MHz/100kHz		−33	−27	dB
Group delay 1		$t1_{GD1\sim5}$ (★ 6)	at 100kHz		45	80	ns
Group delay 2		$t2_{GD6\sim8}$ (★ 6)	Standard Definition select at 100kHz		25	50	ns
Group delay 3		$t2_{GD6\sim8}$ (★ 6)	High Definition select at 100kHz		22	45	ns
Group delay deviation 1 (C, V, Y)		$\Delta t1_{GD1\sim5}$ (★ 6)	to 3.58MHz		4	10	ns
			to 4.43MHz		6	10	ns
			to 6MHz		12	20	ns
Group delay deviation 2 (CY, Cb, Cr) at Standard Definition select		$\Delta t2_{GD6\sim8}$ (★ 6)	to 2MHz		1	10	ns
			to 12MHz		6	15	ns
Group delay deviation 3 (CY, Cb, Cr) at High Definition select		$\Delta t3_{GD6\sim8}$ (★ 6)	to 4MHz		1	10	ns
			to 24MHz		6	15	ns
Between channel Group delay deviation 1		$\Delta t1_{chGD}$	Between C and Y at 3.58MHz		1	10	ns
Between channel Group delay deviation 2		$\Delta t2_{chGD}$	Between CY and Cb (Cr) at 2MHz (Standard Definition)		1	10	ns
Between channel Group delay deviation 3		$\Delta t3_{chGD}$	Between CY and Cb (Cr) at 4MHz (High Definition)		1	10	ns
Differential gain		$DG_{1\sim3}$ (★ 6)	Staircase signal 1V		1.0	1.5	%
Differential phase		$DP_{1\sim3}$ (★ 6)	Staircase signal 1V		1.0	1.5	°
Crosstalk 1		$CT1_n$ (★ 6)	f=4.43MHz, 1V		−60	−55	dB
Crosstalk 2		$CT2_n$ (★ 6)	f=20MHz, 1V		−45	−40	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
S/N 1	$SN1_{1,4\sim5}$ (*6)	BW : 100k ~ 6MHz		–80		dB
S/N 2	$SN2_{2\sim3}$ (*6)	BW : 100k ~ 6MHz at MIX OUT		–74		dB
S/N 3	$SN3_{6\sim8}$ (*6)	BW : 100k ~ 6MHz at SD select		–80		dB
S/N 4	$SN4_{6\sim8}$ (*6)	BW : 100k ~ 30MHz at HD select		–66		dB

Note1 : *1 It is a output terminal voltage when input terminal (1pin) is 0.6V.
Note2 : *2 It is a output terminal voltage when input terminal (3pin) is 0.3V.
Note3 : *3 It is a output terminal voltage when input terminal (5, 12pin) is 0.3V.
Note4 : *4 It is a output terminal voltage when input terminal (14, 16pin) is 0.6V.
Note5 : *5 The subscript number "m" is the terminal of under table.

m	terminal
1	Mute1
2	Mute2
3	SD/HD
4	YC MIX
5	Clamp/Bias
6	Dual/Single

Note6 : *6 The subscript number "n" is the combination of under table.

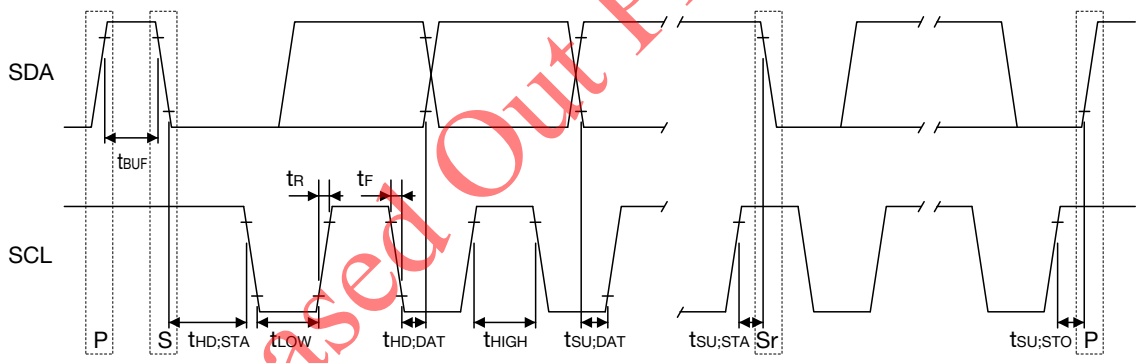
n	input	output
1	V_{IN}	V_{OUT}
2	Y_{IN}	
3	C_{IN}	
4	Y_{IN}	Y_{OUT}
5	C_{IN}	C_{OUT}
6	CY_{IN}	CY_{OUT}
7	Cb_{IN}	Cb_{OUT}
8	Cr_{IN}	Cr_{OUT}

Electrical Characteristics

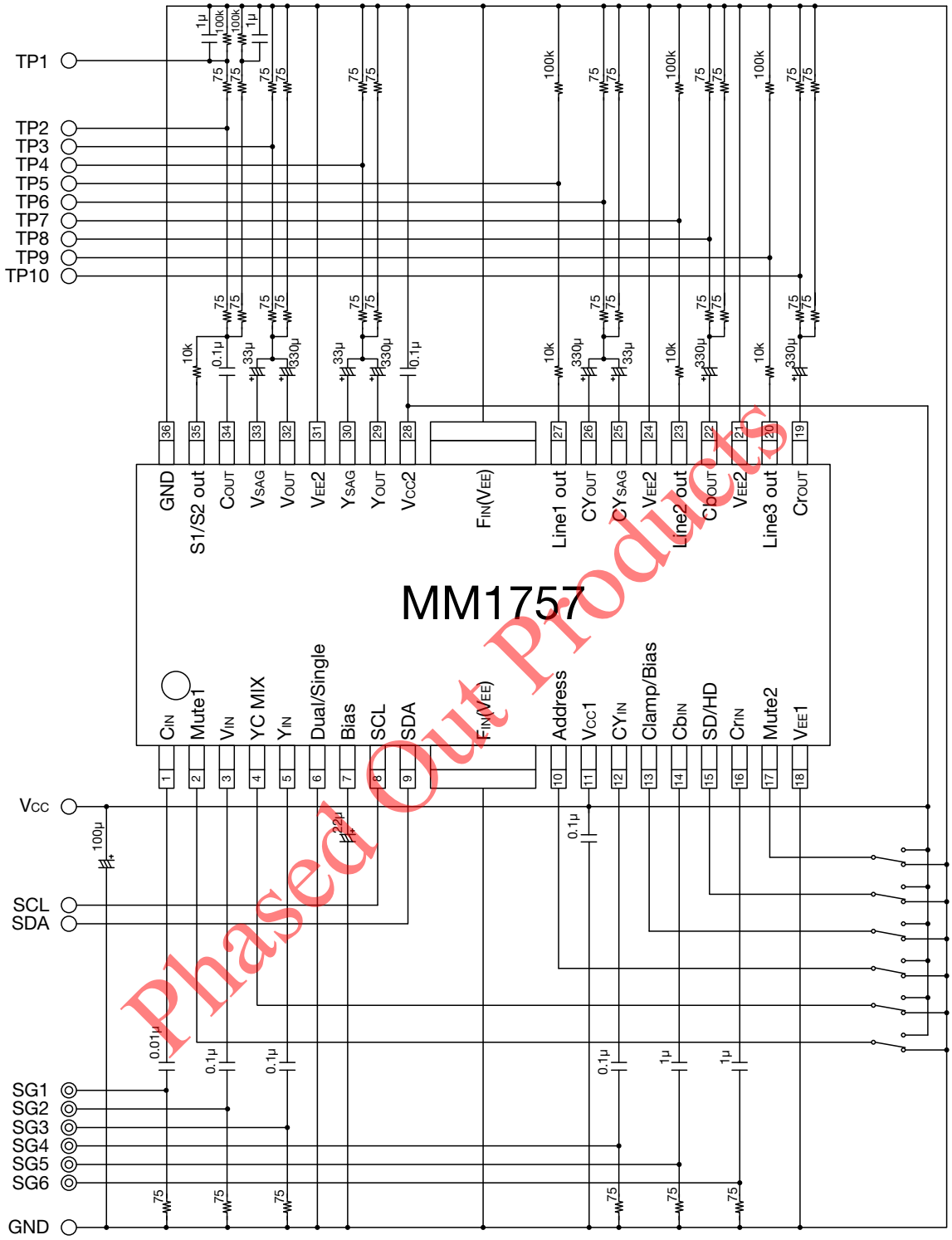
(Except where noted otherwiseTa=25°C, V_{CC}=5V, V_{EE}=-3V [dual power supply] or V_{CC}=5V [single power supply])

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[I²C condition]						
Input voltage Low	V_{IL}		0		0.7	V
Input voltage High	V_{IH}		2.1		5.0	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	0		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	−10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	−10		10	µA
Clock frequency	f_{SCL}				100	kHz
Data transfer wait time	t_{BUF}		4.7			µs
SCL start hold time	$t_{HD;STA}$		4.0			µs
SCL low level hold time	t_{LOW}		4.7			µs
SCL high level hold time	t_{HIGH}		4.0			µs
Start condition setup time	$t_{SU;STA}$		4.7			µs
SDA data hold time	$t_{HD;DAT}$		0			µs
SDA data setup time	$t_{SU;DAT}$		250			ns
SDA, SCL rise time	t_R				1000	ns
SDA, SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		4.0			µs

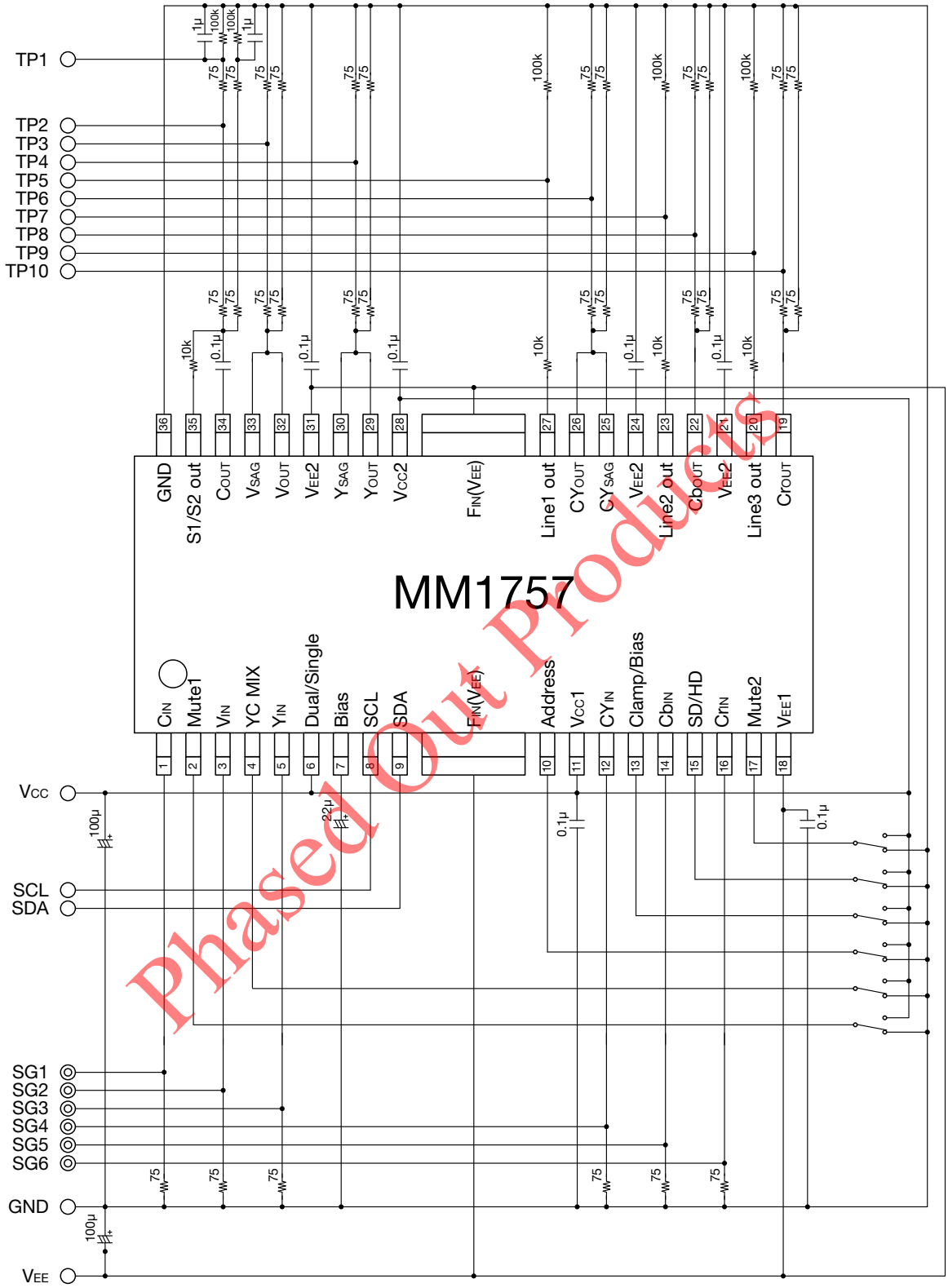
I²C condition



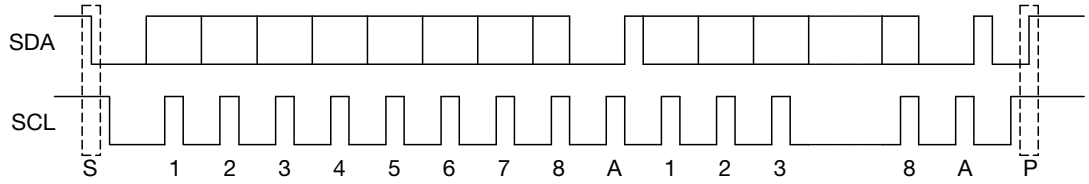
Measuring Circuit (at the single power supply)



Measuring Circuit (at the dual power supply)



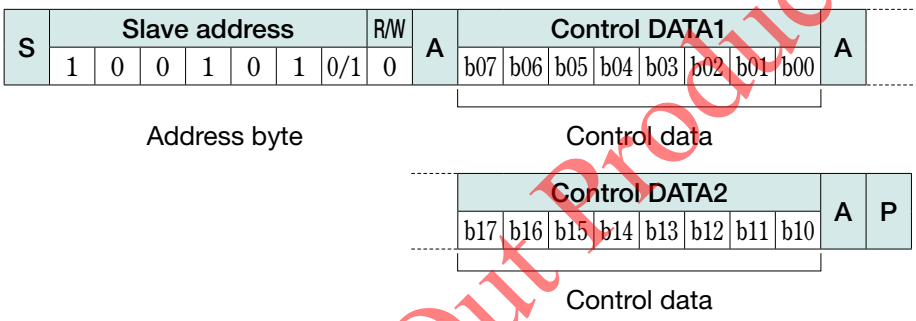
I²C BUS



I²C BUS is inter IC bus system controlled by 2 lines (SDA,SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used control register. As MM1757 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

No.	Control DATA condition							
Control DATA1	b07	b06	b05	b04	b03	b02	b01	b00
				SD/HD	YC MIX	Clamp/Bias	Mute1	Mute2
Control DATA2	b17	b16	b15	b14	b13	b12	b11	b10
		Line1		Line2	Line3		S1/S2	

MM1757 consists of one address byte and two control data bytes (3bytes in total). All data over the limited length (4th and subsequent bytes) is fully neglected.

For details of the control contents of switches, refer to the separate table.

Switch Control Table (* : Don't care (High Low))

(1) Mute select

I²C control		Control terminal		Output terminal					
b01	b00	Mute1 (2pin)	Mute2 (17pin)	VOUT	YOUT	COUT	CYOUT	CbOUT	CrOUT
0	*	Low	*	Mute OFF			*	*	*
1		Low		Mute ON					
*		High							
*	0	*	Low	*	*	*	Mute OFF		
	1		Low				Mute ON		
	*		High						

(2) Clamp/Bias select

I²C control	Control terminal	Input terminal	
b02	Clamp/Bias (13pin)	CYIN (Single)	CYIN (Dual)
0	Low	Clamp ON	Clamp OFF
1	Low	Bias	
*	High		

·Single : Single power supply, Dual: Dual power supply

(3) YC MIX select

I²C control	Control terminal	Input terminal
b03	YC MIX (4pin)	VOUT
0	Low	VIN
1	Low	YIN + CIN
*	High	

(1) + (2) + (3) Input select

Input	Output	I²C BUS Control				Control terminal			
		b03	b02	b01	b00	YC MIX (4pin)	Clamp/Bias (13pin)	Mute1 (2pin)	Mute2 (17pin)
Mute	VOUT	*	*	1	*	*	*	Low	*
				*				High	
VIN		0		0		Low		Low	
VIN + CIN		1							
		*				High			
Mute	YOUT	*	*	1	*	*	*	Low	*
				*				High	
YIN				0				Low	
Mute	COUT	*	*	1	*	*	*	Low	*
				*				High	
CIN				0				Low	
Mute	CYOUT	*	*	*	1	*	*	*	Low
					*				High
YIN (Clamp ON or OFF)			0		0		Low		Low
YIN (Bias)			1				Low		
			*				High		
Mute	CbOUT	*	*	*	1	*	*	*	Low
					*				High
CbIN					0				Low
Mute	CrOUT	*	*	*	1	*	*	*	Low
					*				High
CrIN					0				Low

LPF select

I²C control b04	Control terminal SD/HD (15pin)	CY, CB, CR LPF bandwidth
0	Low	13.5MHz (Standard Definition)
1	Low	30MHz (High Definition)
*	High	

S1/S2 Output terminal voltage [Aspect]

I²C control b11	I²C control b10	S1/S2 out Output voltage	Signal mode
0	0	0V	4:3 Normal
0	1	2.1V	4:3 Letter box
1	1		
1	0	4.6V	16:9 Squeeze

Line1 Output terminal voltage [Scanning Line]

I²C control b16	I²C control b15	Line1 out Output voltage	Signal mode
0	0	0V	480
0	1	2.1V	720
1	1		
1	0	4.6V	1080

Line2 Output terminal voltage [Interlace/Progressive]

I²C control b14	Line2 out Output voltage	Signal mode
0	0V	Interlace
1	4.6V	Progressive

Line3 Output terminal voltage [Aspect]

I²C control b13	I²C control b12	Line3 out Output voltage	Signal mode
0	0	0V	4:3 Normal
0	1	2.1V	4:3 Letter box
1	1		
1	0	4.6V	16:9 Squeeze

Dual/Single power supply select

Control terminal Dual/Single (6pin)	Power supply
Low	Single
High	Dual

[Status registers]

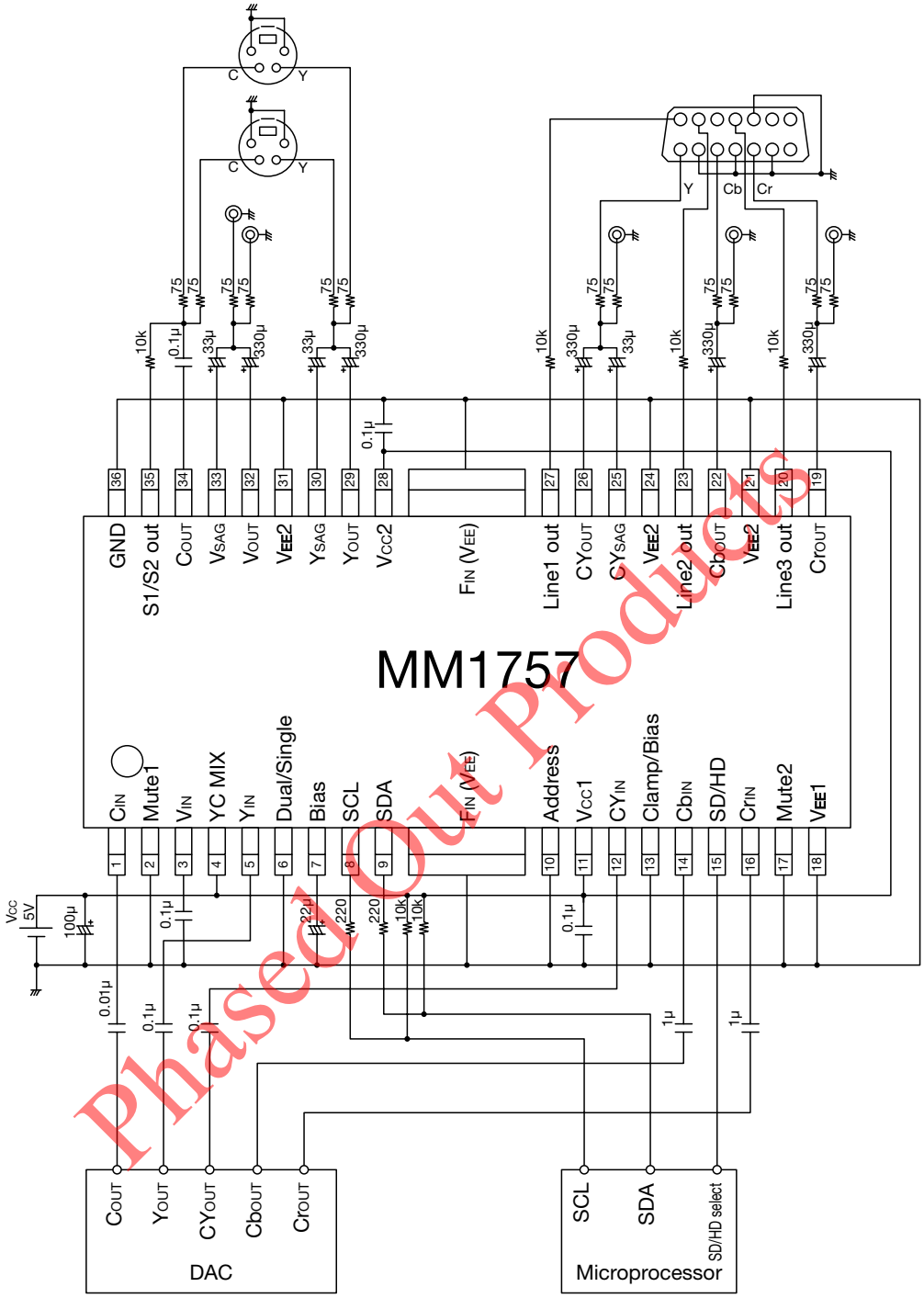
There is no preparation of the status register in MM1757.

A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.

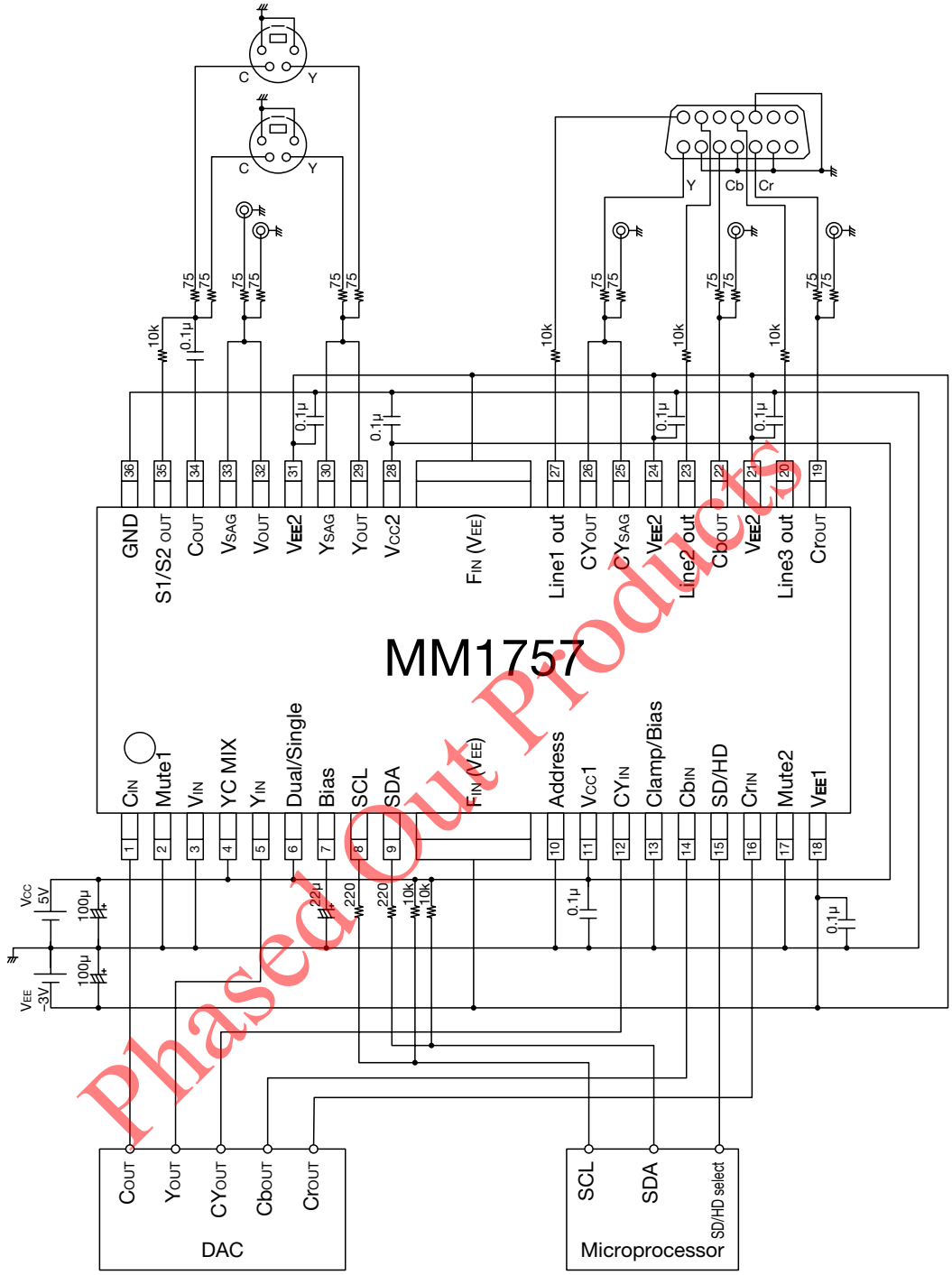
S	Slave address							R/W	A	Status DATA1								NA	P
	1	0	0	1	0	0	0/1	1		1	1	1	1	1	1	1	1		
	Address byte									Status data									

Application Circuit 1 (at the single power supply)



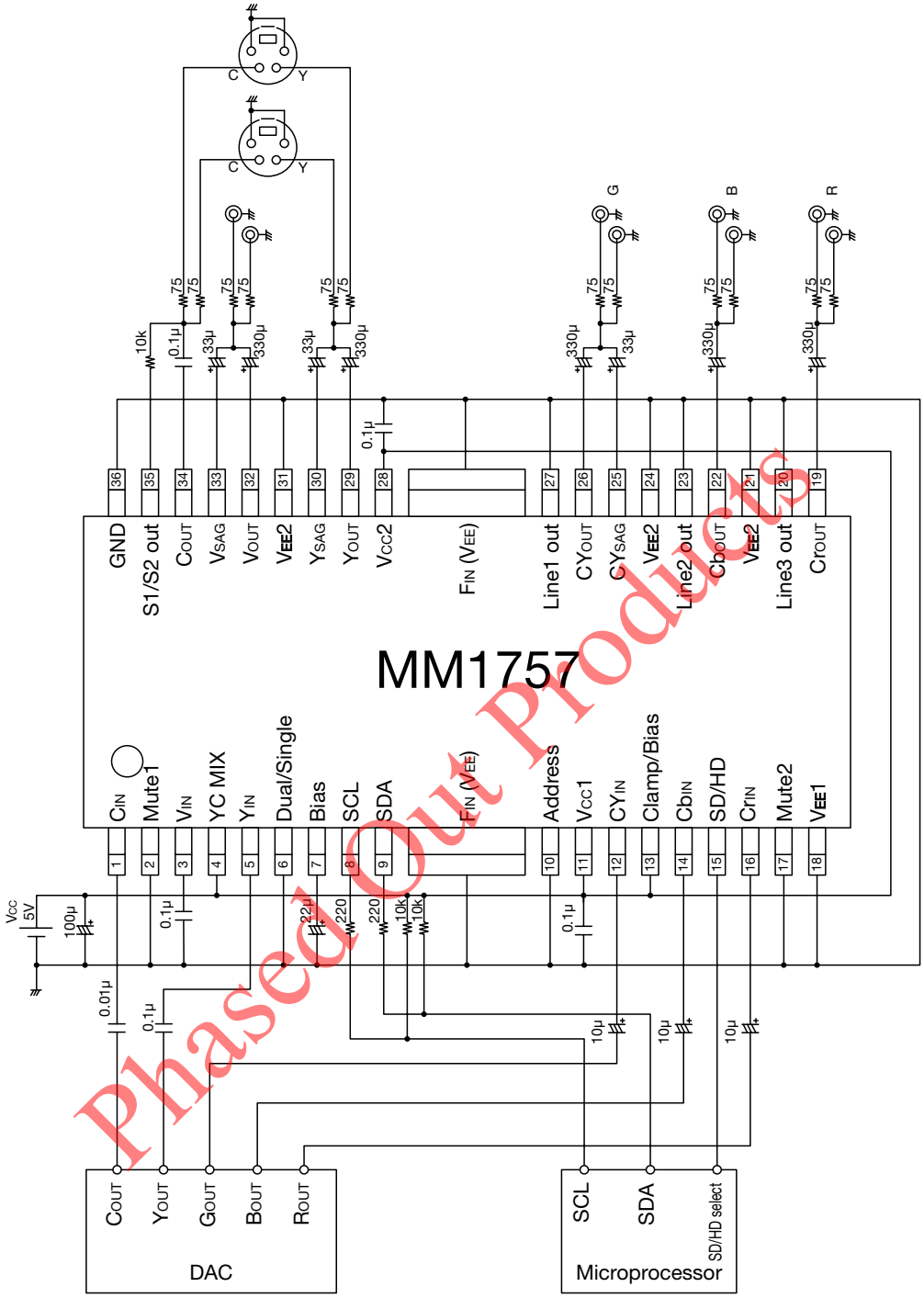
Note1: Please arrange power supply bypass capacitor near the V_{CC} terminal (pin).
Note2: Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Application Circuit 2 (at the dual power supply)



Note1: Please arrange power supply bypass capacitor near the V_{CC}, V_{EE} terminal (pin).
Note2: Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

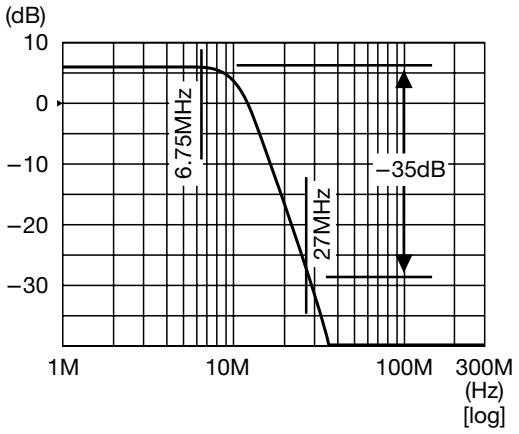
Application Circuit 3 (When RGB signal is used)



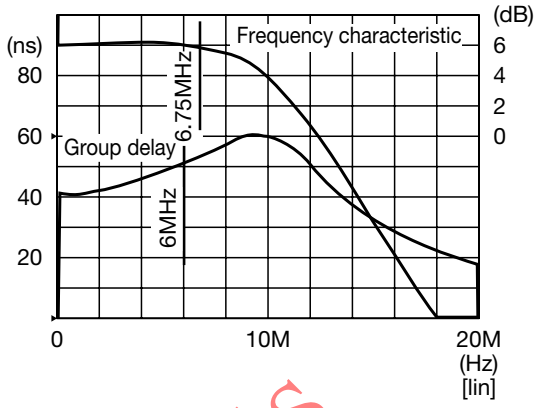
Note1: Please arrange power supply bypass capacitor near the V terminal (pin).
Note2: Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

Characteristics

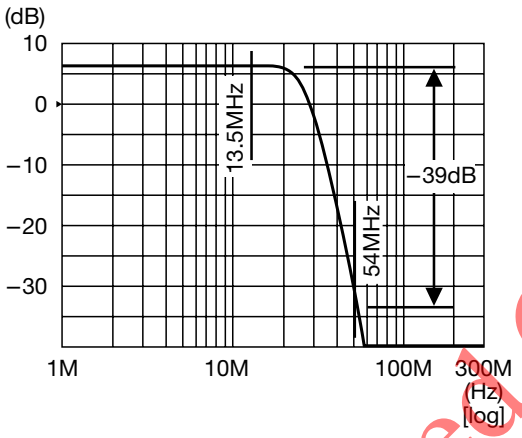
Frequency characteristic (COUT, VOUT, YOUT)



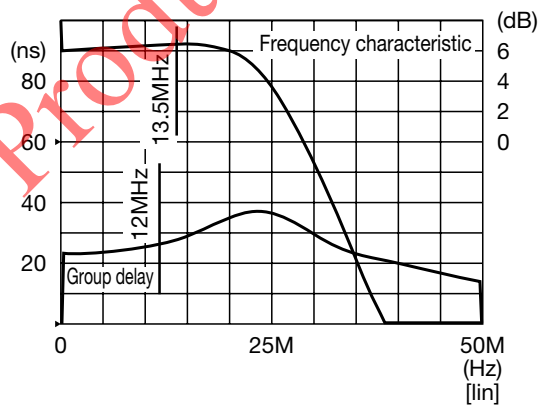
Group delay (COUT, VOUT, YOUT)



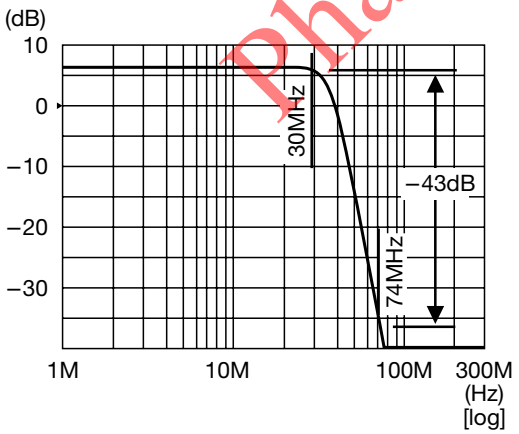
Frequency characteristic (CYOUT, CbOUT, CrOUT) [at SD select]



Group delay (CYOUT, CbOUT, CrOUT) [at SD select]



Frequency characteristic (CYOUT, CbOUT, CrOUT) [at HD select]



Group delay (CYOUT, CbOUT, CrOUT) [at HD select]