

# 2-SCART Compatible AV Switch for DVD Recorders for Europe Monolithic IC MM1763

## Outline

This IC is a one-chip IC integrating an I<sup>2</sup>C BUS controlled AV switch with 4 inputs and 3 outputs with a 6-channel video driver with a built-in LPF. 2 outputs among 3 outputs of the AV switch are 75Ω drivers, which is ideal for analog interface for recording equipment such as 2-SCART compatible DVD recorders for Europe.

## Features

1. Serially controlled with I<sup>2</sup>C BUS
2. Provided in a small package (SSOP-42) with an extensive function of a switch + driver
3. Optimized pin assignment considering the device architecture (non-complicated board layout can be realized)
4. 6-channel video driver including a high performance 4th-order LPF
5. Audio output that is programmable between 0dB and 6dB and includes a newly-developed adjustable gain amplifier
6. Includes auto power saving function when V<sub>CC</sub>=12V is off (between V<sub>CC</sub>=5V, 12V)  
(when V<sub>CC</sub>=12V is on, power saving is also possible by serial control)

## Package

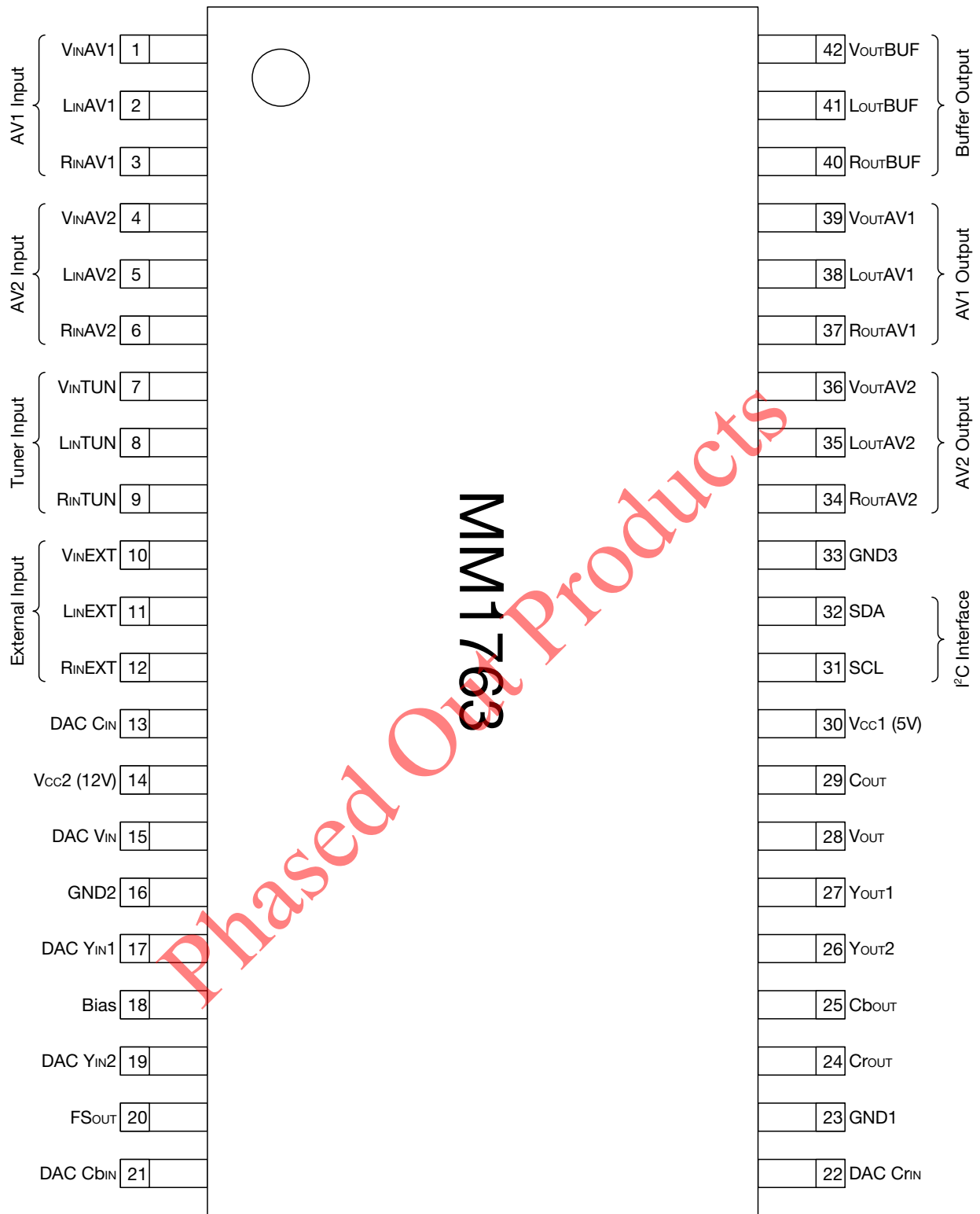
SSOP-42A

## Applications

1. DVD recorders
2. VCRs
3. STBs
4. Recording equipment

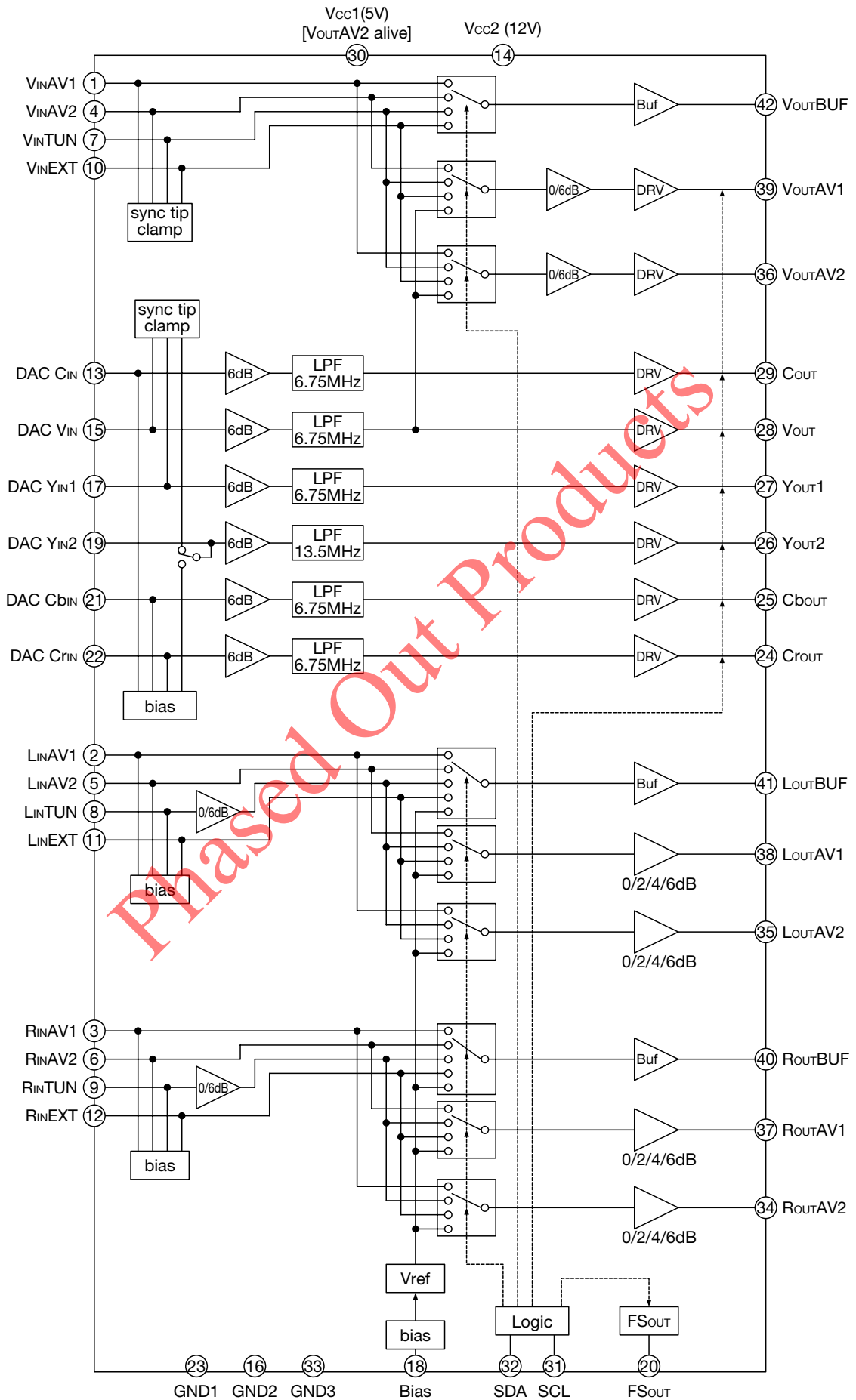
Phased Out Products

Pin Assignment

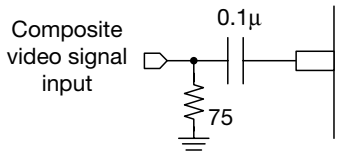
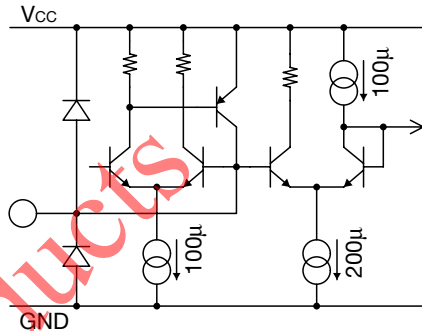
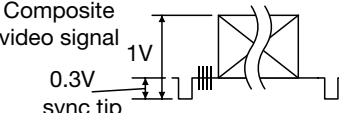
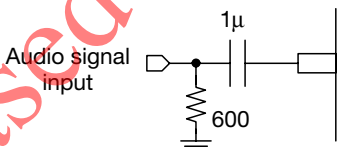
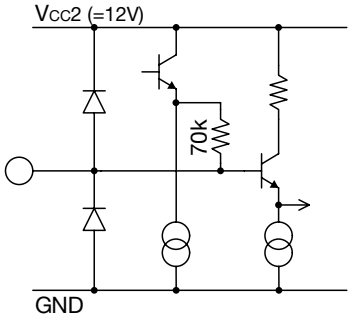
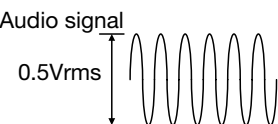


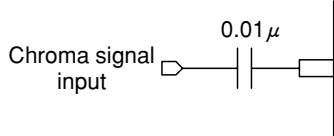
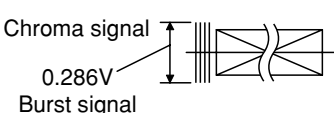
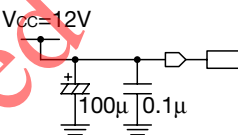
1	V <sub>INAV1</sub>	8	L <sub>INTUN</sub>	15	DAC V <sub>IN</sub>	22	DAC C <sub>TIN</sub>	29	C <sub>OUT</sub>	36	V <sub>OUTAV2</sub>
2	L <sub>INAV1</sub>	9	R <sub>INTUN</sub>	16	GND2	23	GND1	30	V <sub>CC1</sub> (5V)	37	R <sub>OUTAV1</sub>
3	R <sub>INAV1</sub>	10	V <sub>INEXT</sub>	17	DAC Y <sub>IN1</sub>	24	C <sub>ROUT</sub>	31	SCL	38	L <sub>OUTAV1</sub>
4	V <sub>INAV2</sub>	11	L <sub>INEXT</sub>	18	BIAS	25	C <sub>BOU</sub> T	32	SDA	39	V <sub>OUTAV1</sub>
5	L <sub>INAV2</sub>	12	R <sub>INEXT</sub>	19	DAC Y <sub>IN2</sub>	26	Y <sub>OUT2</sub>	33	GND3	40	R <sub>OUTBUF</sub>
6	R <sub>INAV2</sub>	13	DAC C <sub>IN</sub>	20	FS <sub>OUT</sub>	27	Y <sub>OUT1</sub>	34	R <sub>OUTAV2</sub>	41	L <sub>OUTBUF</sub>
7	V <sub>INTUN</sub>	14	V <sub>CC2</sub> (12V)	21	DAC C <sub>bin</sub>	28	V <sub>OUT</sub>	35	L <sub>OUTAV2</sub>	42	V <sub>OUTBUF</sub>

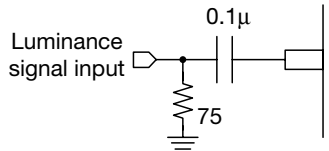
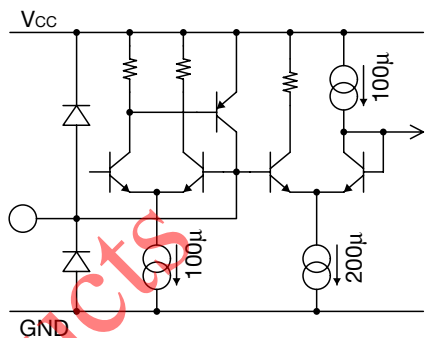
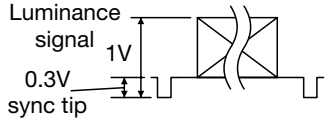
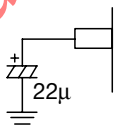
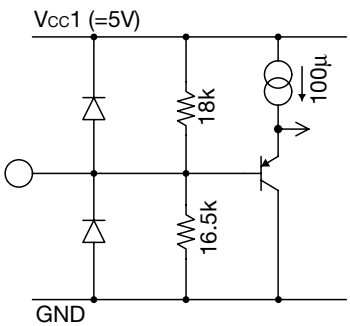
Block Diagram

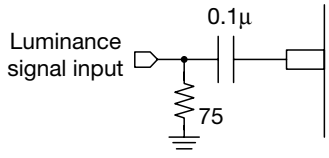
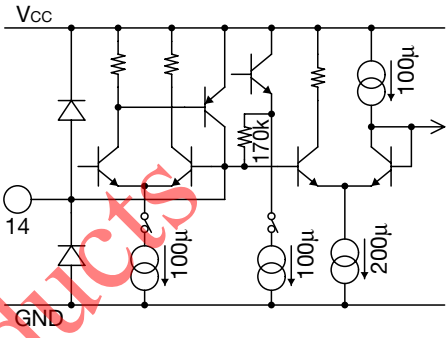
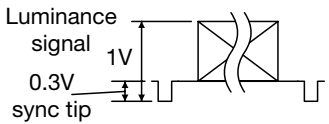


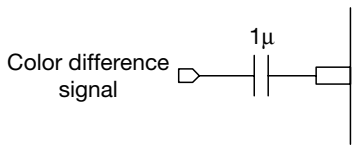
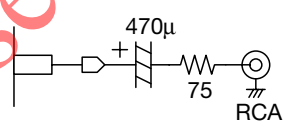
Pin Description

Pin No.	Pin name	Pin description	
		<b>Function</b>	
		Composite signal input Input clamp Pin voltage: 1.1V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
1	V <sub>INAV1</sub>	 <p>Composite video signal input</p> <p>When not using it: open</p>	
4	V <sub>INAV2</sub>		
7	V <sub>INTUN</sub>		
10	V <sub>INEXT</sub>		
15	DAC V <sub>IN</sub>		
		<b>Input signal</b>	
		 <p>Composite video signal</p> <p>1V</p> <p>0.3V sync tip</p>	
		<b>Function</b>	
		Audio signal input Input impedance: 70kΩ typ. Pin voltage: 7.0V typ. Input dynamic range: 3V <sub>rms</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
2	L <sub>INAV1</sub>	 <p>Audio signal input</p> <p>When not using it: open</p>	
3	R <sub>INAV1</sub>		
5	L <sub>INAV2</sub>		
6	R <sub>INAV2</sub>		
8	L <sub>INTUN</sub>		
9	R <sub>INTUN</sub>		
11	L <sub>INEXT</sub>		
12	R <sub>INEXT</sub>		
		<b>Input signal</b>	
		 <p>Audio signal</p> <p>0.5V<sub>rms</sub></p>	

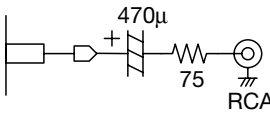
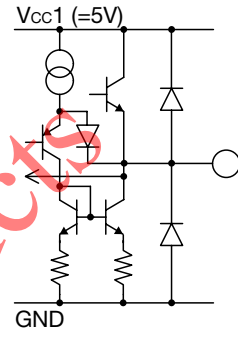
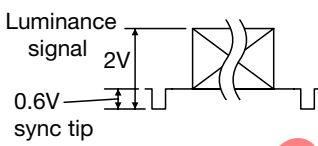
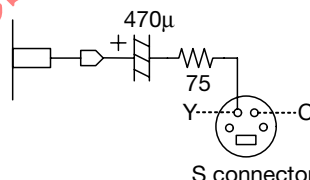
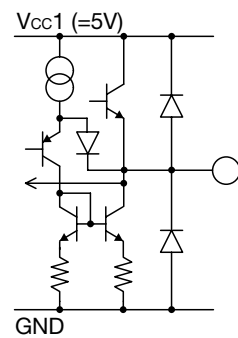
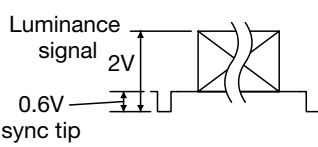
Pin No.	Pin name	Pin description	
13	DAC C <sub>IN</sub>	<b>Function</b>	
		Chroma signal input Input bias Pin voltage: 2.4V typ. Input impedance: 170kΩ typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Chroma signal input</p> <p>0.01 μ</p> <p>When not using it: OPEN</p>	
		<b>Output signal</b>	
		 <p>Chroma signal</p> <p>0.286V</p> <p>Burst signal</p>	
14	V <sub>CC2</sub>	<b>Function</b>	
		Voltage supply It is a supply voltage impression terminal. Please impress 12V. Please arrange a bypass capacitor near the terminal.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>V<sub>CC</sub>=12V</p> <p>100μ</p> <p>0.1μ</p>	
		<b>Output signal</b>	
		DC voltage: +11.2V~+12.8V	
16	GND2	<b>Function</b>	
23	GND1	GND	
33	GND3	Ground	

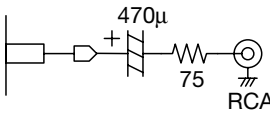
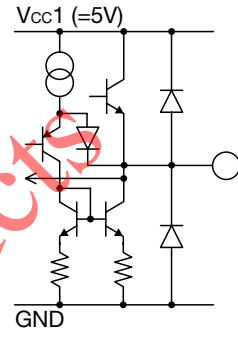
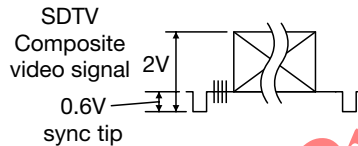
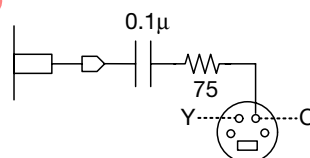
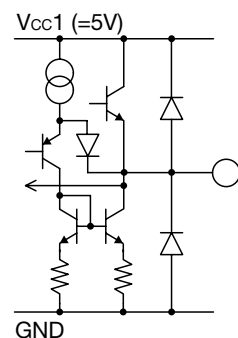
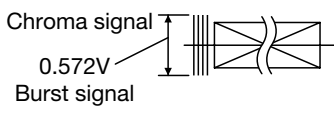
Pin No.	Pin name	Pin description	
17	DAC Y <sub>IN1</sub>	<b>Function</b>	
		Luminance signal input Input clamp Pin voltage: 1.1V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Input signal</b>	
			
18	BIAS	<b>Function</b>	
		BIAS All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.  Input impedance: 8.6kΩ typ.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Output signal</b>	

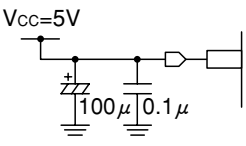
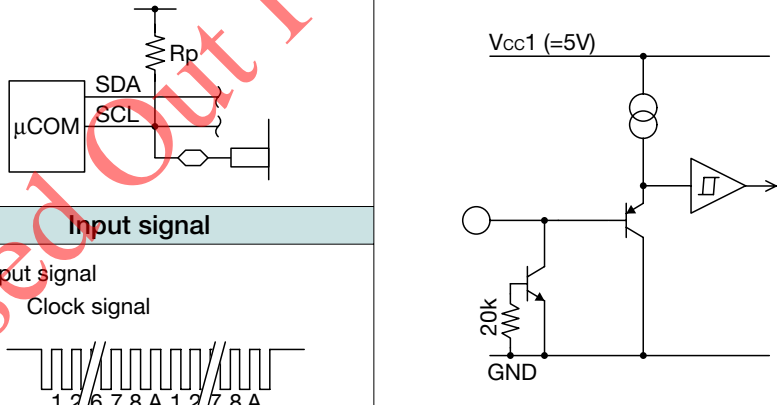

Pin No.	Pin name	Pin description																	
19	DAC Y <sub>IN2</sub>	<b>Function</b>																	
		Luminance signal (G-signal) input Input clamp or bias select Pin voltage: 1.1V typ. (Clamp select) 2.4V typ. (Bias select) Input dynamic range: 1.3V <sub>P-P</sub> min.																	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																
		 <p>When not using it: open</p>																	
<b>Input signal</b>																			
																			
20	FS <sub>OUT</sub>	<b>Function</b>																	
		DC output for SCART interface It is the terminal which outputs Function switch signal of SCART interface. The ternary output of L/M/H is controllable by I <sup>2</sup> C control. (refer to Switch Control Table)  Output impedance: 500Ω typ. Low level output voltage: 0V typ. Middle level output voltage: 6V typ. High level output voltage: 10V typ.																	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																
		When not using it: open  <b>Output signal</b> DC voltage: <table border="1" data-bbox="542 1556 925 1758" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>b01</th> <th>b00</th> <th colspan="2">DC<sub>OUT</sub></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>L</td> <td>Level 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>M</td> <td>Level 1A</td> </tr> <tr> <td>1</td> <td>0</td> <td rowspan="2">H</td> <td rowspan="2">Level 1B</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </tbody> </table>	b01	b00	DC <sub>OUT</sub>		0	0	L	Level 0	0	1	M	Level 1A	1	0	H	Level 1B	1
b01	b00	DC <sub>OUT</sub>																	
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1	0	H	Level 1B																
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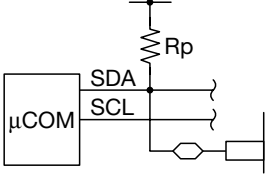
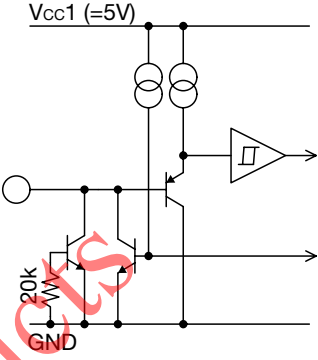
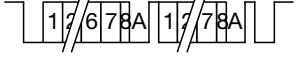
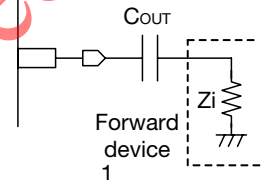
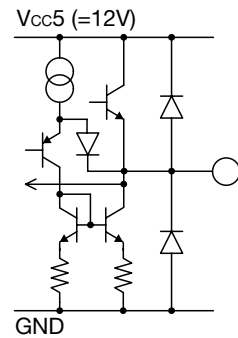
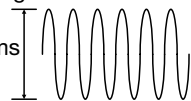
Pin No.	Pin name	Pin description	
21 22	DAC C <sub>bIN</sub> DAC C <sub>rIN</sub>	<b>Function</b>	
		Color difference signal input Input bias Pin voltage: 2.4V typ. Input impedance: 170kΩ typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		When not using it: open <b>Input signal</b> Color difference signal 0.7V	
24 25	C <sub>rOUT</sub> C <sub>bOUT</sub>	<b>Function</b>	
		Color difference output It is a terminal for the Color difference signal external output.  Pin voltage: 2.4V typ. Load resistance: 150Ω × 2 Stray capacitance max.: 20pF	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		When not using it: open <b>Output signal</b> Color difference signal 1.4V	



Pin No.	Pin name	Pin description	
26	Yout2	<b>Function</b>	
		<p>Luminance output (525p) It is a terminal for a Luminance signal (525p) external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Output signal</b>	
			
27	Yout1	<b>Function</b>	
		<p>Luminance output (525i) It is a terminal for a Luminance signal (525i) external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Output signal</b>	
			

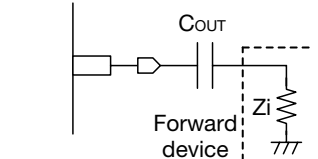
Pin No.	Pin name	Pin description	
		<b>Function</b>	
		<p>Composite video output It is a terminal for a composite video signal external output.</p> <p>Pin voltage: 1.1V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
28 36 39	V <sub>OUT</sub> V <sub>OUTAV2</sub> V <sub>OUTAV1</sub>	 <p>When not using it: open</p>	
		<b>Output signal</b>	
			
		<b>Function</b>	
		<p>Chroma output It is a terminal for the Chroma signal external output.</p> <p>Pin voltage: 2.4V typ. Load resistance: <math>150\Omega \times 2</math> Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
29	C <sub>OUT</sub>	 <p>When not using it: open</p>	
		<b>Output signal</b>	
			

Pin No.	Pin name	Pin description	
30	Vcc1	<b>Function</b>	
		Voltage supply It is a supply voltage impression terminal. Please impress 5V. Please arrange a bypass capacitor near the terminal.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>  DC voltage: +4.5V~+5.5V	
31	SCL	<b>Function</b>	
		Clock input of I <sup>2</sup> C BUS It is the terminal which connects the SCL line of I <sup>2</sup> C BUS.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>  Input signal Clock signal 	

Pin No.	Pin name	Pin description	
32	SDA	<b>Function</b>	
		DATA Input/Output of I <sup>2</sup> C BUS It is the terminal which connects the SDA line of I <sup>2</sup> C BUS.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<div style="display: flex; justify-content: space-around;"> <div style="width: 45%;">  </div> <div style="width: 45%;">  </div> </div>	
<b>Input output signal</b>			
Input signal Control registers Output signal States registers			
			
34 35 37 38	RoutAV2 LoutAV2 RoutAV1 LoutAV1	<b>Function</b>	
		Audio signal output It is a terminal for a audio signal external output.  Pin voltage: 6.3V typ. Load resistance: 600Ω max. Stray capacitance max.: 20pF	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<div style="display: flex; justify-content: space-around;"> <div style="width: 45%;">  <math display="block">C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}</math> <p style="text-align: right;">*f<sub>CL</sub>=1~10Hz</p> <p>When not using it: open</p> </div> <div style="width: 45%;">  </div> </div>	
<b>Output signal</b>			
Audio signal 0.5Vrms			
			

Pin No.	Pin name	Pin description
40 41	RoutBUF LoutBUF	<b>Function</b>
		<p>Audio signal output It is a terminal for a audio signal output.</p> <p>Pin voltage: 6.3V typ. Load resistance: 1kΩ max. Stray capacitance max.: 20pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>
42	VoutBUF	<b>Function</b>
		<p>Composite video output It is a terminal for a composite video signal output.</p> <p>Pin voltage: 1.1V typ. Load resistance: 1kΩ max. Stray capacitance max.: 20pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>

**External circuit**

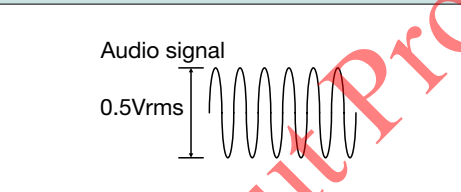


$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$$

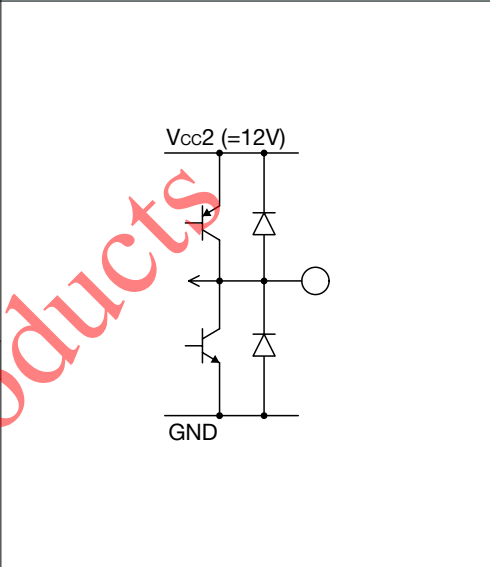
\*f<sub>CL</sub>=1~10Hz

When not using it: open

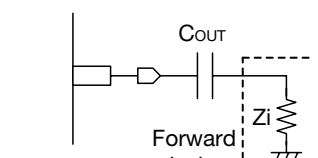
**Output signal**



**Equivalent circuit diagram**



**External circuit**

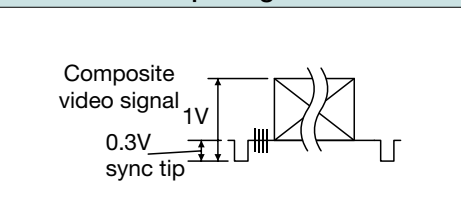


$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$$

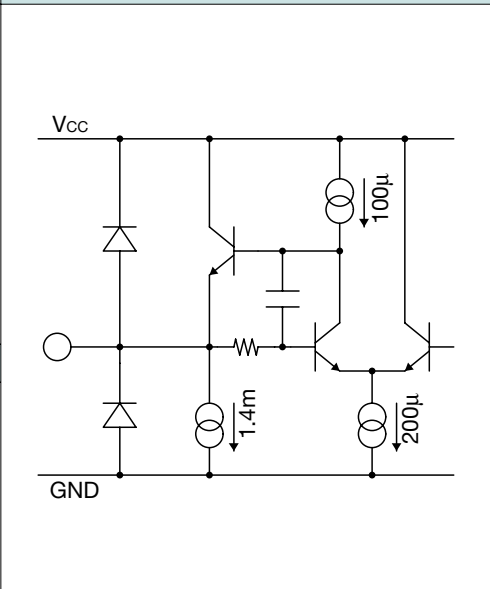
\*f<sub>CL</sub>=1~10Hz

When not using it: open

**Output signal**



**Equivalent circuit diagram**



**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-55~+150	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Supply voltage	V <sub>CC max.</sub>	13	V
Allowable loss (*1)	P <sub>d</sub>	2.4	W

Note1: \*1 Board mounting allowable loss. Board size: 190×150×1.6mm GE

**Recommended Operating Conditions**

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
V <sub>CC1</sub> Operating voltage	V <sub>CC1OP</sub>	4.5~5.5	V
V <sub>CC2</sub> Operating voltage	V <sub>CC2OP</sub>	11.2~12.8	V

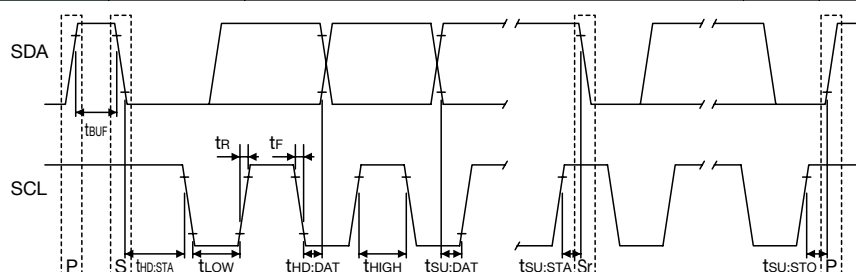
**Electrical Characteristics** (Except where noted otherwise Ta=25°C, V<sub>CC1</sub>=5V, V<sub>CC2</sub>=12V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V <sub>CC1</sub> supply current		I <sub>CC1</sub>	No signal (V <sub>CC</sub> =5V)	75	105	135	mA
V <sub>CC2</sub> supply current		I <sub>CC2</sub>	No signal (V <sub>CC</sub> =12V)	19	26	33	mA
V <sub>CC1</sub> supply current at standby		I <sub>CC3</sub>	No signal (V <sub>CC</sub> =5V)	18	25	32	mA
FS <sub>OUT</sub> Output voltage	H	F <sub>SH</sub>	R <sub>L</sub> =10kΩ	9.5	10.5	12	V
	M	F <sub>SM</sub>		4.5	6	7	V
	L	F <sub>SL</sub>		0	0.01	2	V
Terminal voltage	Video input (clamp)	V <sub>INCn</sub>		0.8	1.1	1.4	V
	Video input (bias)	V <sub>INBn</sub>		2.1	2.4	2.7	V
	Audio input	A <sub>INn</sub>		6.5	7	7.5	V
	Video output (clamp)	V <sub>OUTCn</sub>			1.1		V
	Video output (bias)	V <sub>OUTBn</sub>			2.4		V
	Audio output	A <sub>OUTn</sub>			6.3		V
<b>[V<sub>OUTBUF</sub>]</b>							
Voltage gain		G <sub>Vn</sub>	SIN wave: 1V f=100kHz	-0.3	0	0.3	dB
Frequency characteristic		f <sub>Vn</sub>	SIN wave: 1V 10MHz/100kHz	-1	0	1	dB
Output dynamic range		DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.9		V
Differential gain		DG <sub>Vn</sub>	Staircase signal 1V		0.2	1	%
Differential phase		DP <sub>Vn</sub>	Staircase signal 1V		0.1	1	deg
<b>[V<sub>OUTAV1</sub>, V<sub>OUTAV2</sub>]</b>							
Voltage gain		G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic		f <sub>Vn</sub>	SIN wave: 1V 6.75MHz/100kHz	-1	0	1	dB
Output dynamic range		DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG <sub>Vn</sub>	Staircase signal 1V		2	3	%
Differential phase		DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
<b>[C<sub>OUT</sub>, V<sub>OUT</sub>, Y<sub>OUT1</sub>]</b>						
Voltage gain	G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	f <sub>1Vn</sub>	SIN wave: 1V 6.75MHz/100kHz	-1	0	1	dB
Frequency characteristic 2	f <sub>2Vn</sub>	SIN wave: 1V 27MHz/100kHz		-30	-24	dB
Output dynamic range	DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG <sub>Vn</sub>	Staircase signal 1V		1	2	%
Differential phase	DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg
Signal/Noise	SN <sub>Vn</sub>	BW: 100kHz~6MHz		80		dB
Group delay	t <sub>Vn</sub>	at 100kHz		50	80	ns
Group delay deviation	Δt <sub>Vn</sub>	to 3.58MHz		5	10	ns
		to 4.43MHz		10	20	ns
		to 6MHz		20	28	ns
<b>[Y<sub>OUT2</sub>, C<sub>OUT</sub>, C<sub>ROUT</sub>]</b>						
Voltage gain	G <sub>Vn</sub>	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	f <sub>1V (YOUT2)</sub>	100 [IRE] SIN wave + 40 [IRE] sync 13.5MHz/100kHz	1	0	1	dB
Frequency characteristic 2	f <sub>2V (C<sub>OUT</sub>, C<sub>ROUT</sub>)</sub>	100 [IRE] SIN wave + 40 [IRE] sync 6.75MHz/100kHz	-1	0	1	dB
Frequency characteristic 3	f <sub>3Vn</sub>	100 [IRE] SIN wave + 40 [IRE] sync 54MHz/100kHz		-30	-24	dB
Output dynamic range	DR <sub>Vn</sub>	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG <sub>Vn</sub>	Staircase signal 1V		1	2	%
Differential phase	DP <sub>Vn</sub>	Staircase signal 1V		1	2	deg
Signal/Noise	SN <sub>Vn</sub>	BW: 100kHz~6MHz		80		dB
Group delay	t <sub>Vn</sub>	at 100kHz		25	50	ns
Group delay deviation 1	Δt <sub>1V (YOUT2)</sub>	to 2MHz		1	10	ns
		to 8MHz		2	10	ns
		to 12MHz		10	20	ns
Group delay deviation 2	Δt <sub>2V (C<sub>OUT</sub>)</sub> Δt <sub>2V (C<sub>ROUT</sub>)</sub>	to 1MHz		1	10	ns
		to 4MHz		2	10	ns
		to 6MHz		10	20	ns
<b>[L<sub>OUTBUF</sub>, R<sub>OUTBUF</sub>]</b>						
Voltage gain	G <sub>0An</sub>	SIN wave: 1V <sub>rms</sub> f=1kHz	-0.5	0	0.5	dB
	G <sub>6An</sub>	SIN wave: 0.5V <sub>rms</sub> f=1kHz	5.5	6	6.5	dB
Output dynamic range	DR <sub>An</sub>	SIN wave: 1kHz THD=1%	3			V <sub>rms</sub>
Total harmonic distortion	THD <sub>An</sub>	SIN wave: 1kHz, 0dB V <sub>OUT</sub> =1V <sub>rms</sub> , R <sub>L</sub> =10kΩ 30kHz-LPF		0.005	0.05	%
Output noise voltage	VN <sub>An</sub>	A curve		3		μV <sub>rms</sub>
Output offset voltage	VOF <sub>An</sub>	at the switching		0	±15	mV

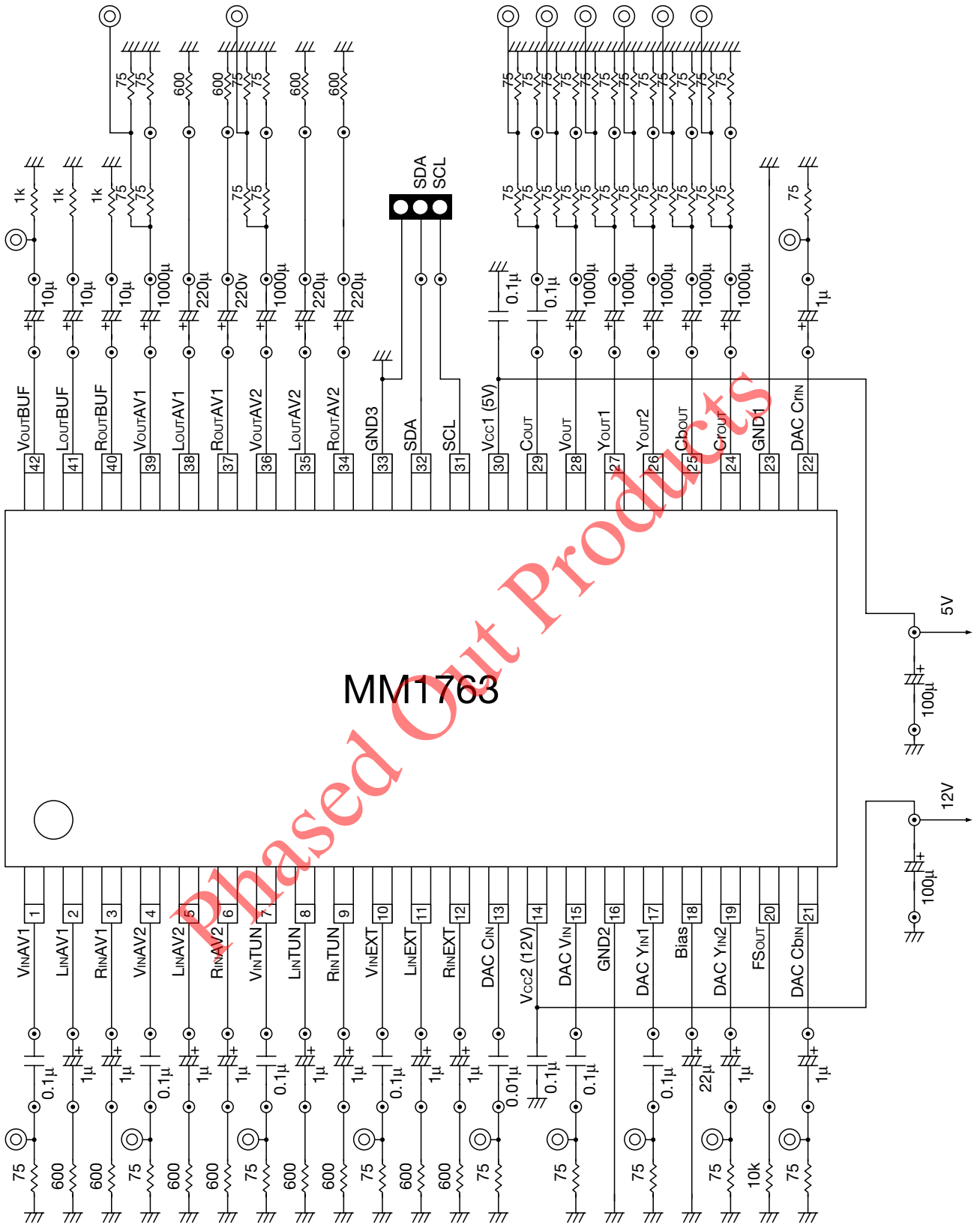
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[L <sub>OUTAV1</sub> , L <sub>OUTAV2</sub> , R <sub>OUTAV1</sub> , R <sub>OUTAV2</sub> ]						
Voltage gain	G0 <sub>An</sub>	SIN wave: 1V <sub>rms</sub> f=1kHz	-0.5	0	0.5	dB
	G2 <sub>An</sub>	SIN wave: 0.79V <sub>rms</sub> f=1kHz	1.5	2	2.5	dB
	G4 <sub>An</sub>	SIN wave: 0.63V <sub>rms</sub> f=1kHz	3.5	4	4.5	dB
	G6 <sub>An</sub>	SIN wave: 0.5V <sub>rms</sub> f=1kHz	5.5	6	6.5	dB
	G8 <sub>An</sub>	SIN wave: 0.4V <sub>rms</sub> f=1kHz	7.5	8	8.5	dB
	G10 <sub>An</sub>	SIN wave: 0.32V <sub>rms</sub> f=1kHz	9.5	10	10.5	dB
	G12 <sub>An</sub>	SIN wave: 0.25V <sub>rms</sub> f=1kHz	11.5	12	12.5	dB
Output dynamic range	DR <sub>An</sub>	SIN wave: 1kHz THD=1%	3			V <sub>rms</sub>
Total harmonic distortion	THD <sub>An</sub>	SIN wave: 1kHz, 0dB V <sub>OUT</sub> =1V <sub>rms</sub> , R <sub>L</sub> =10kΩ 30kHz-LPF		0.005	0.05	%
Output noise voltage	VN <sub>An</sub>	A curve		5		μV <sub>rms</sub>
Output offset voltage	VOF <sub>An</sub>	at the switching		0	±15	mV
Crosstalk	V <sub>OUT</sub>	CT <sub>Vn</sub>		-60	-50	dB
	L <sub>OUT</sub> , R <sub>OUT</sub>	CT <sub>An</sub>		-90	-70	dB
Video input impedance	Z <sub>inVn</sub>	13, 21, 22 pin	120	170	220	kΩ
Audio input impedance	Z <sub>inAn</sub>	L: 2, 5, 8, 11, R: 3, 6, 9, 12 pin	50	70	90	kΩ
Output impedance	Z <sub>OUT</sub>	F <sub>Sout</sub>	300	500	800	Ω
Standby V <sub>CC2</sub> input voltage	L	V <sub>THVCC2L</sub>			2.0	V
	H	V <sub>THVCC2H</sub>	3.5			V
[I <sup>2</sup> C condition]						
Input voltage L	V <sub>IL</sub>		0		0.7	V
Input voltage H	V <sub>IH</sub>		2.1		5.0	V
SDA low level output voltage	V <sub>OL</sub>	SDA sink 3mA	0		0.4	V
High level input current	I <sub>IH</sub>	SDA, SCL=4.5V	-10		10	μA
Low level input current	I <sub>IL</sub>	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f <sub>SCL</sub>				100	kHz
Data transfer wait time	t <sub>BUF</sub>		4.7			μs
SCL start hold time	t <sub>HD;STA</sub>		4.0			μs
SCL low level hold time	t <sub>LOW</sub>		4.7			μs
SCL high level hold time	t <sub>HIGH</sub>		4.0			μs
Start condition setup time	t <sub>SU;STA</sub>		4.7			μs
SDA data hold time	t <sub>HD;DAT</sub>		0			μs
SDA data setup time	t <sub>SU;DAT</sub>		250			ns
SDA, SCL rise time	t <sub>R</sub>				1000	ns
SDA, SCL fall time	t <sub>F</sub>				300	ns
Stop condition setup time	t <sub>SU;STO</sub>		4.0			μs

Note: I<sup>2</sup>C condition

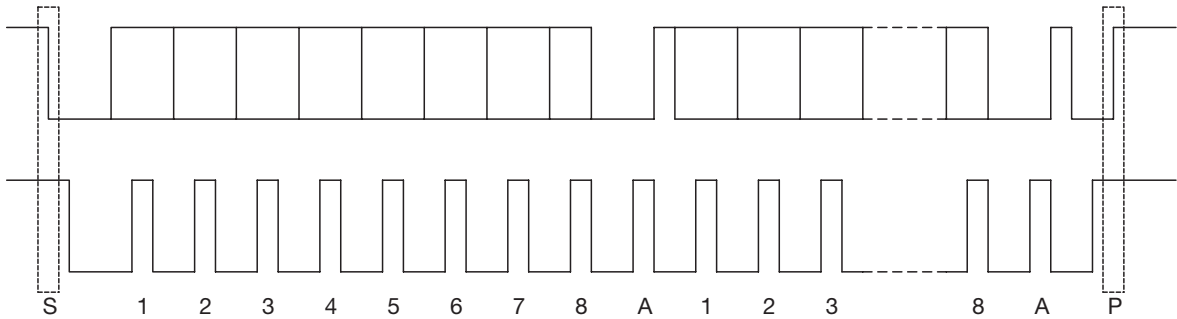




Measuring Circuit



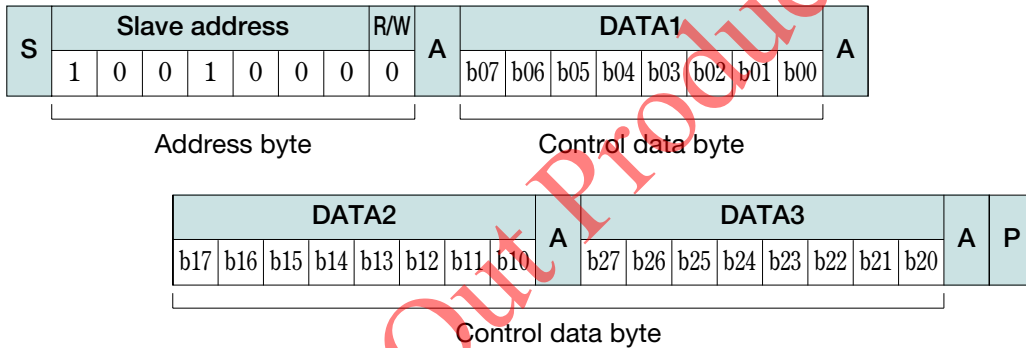
I<sup>2</sup>C BUS



I<sup>2</sup>C BUS is inter IC bus system controlled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[ Control registers ]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used as control register. MM1763 slave address is 90H.

The next figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

[ Control data ]

No.	Control DATA condition							
	b07	b06	b05	b04	b03	b02	b01	b00
DATA1	V <sub>OUT</sub> BUF select		V <sub>OUT</sub> AV1 select		V <sub>OUT</sub> AV2 select		FS CTRL	
	DATA2	b17	b16	b15	b14	b13	b12	b11
	L/R <sub>OUT</sub> BUF select		L/R <sub>OUT</sub> AV1 select		L/R <sub>OUT</sub> AV2 select			L/R <sub>OUT</sub> BUF mute
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	0, 6dB select	clamp bias sel	V <sub>OUT</sub> mute	L/R <sub>OUT</sub> AV1 gain select		L/R <sub>OUT</sub> AV2 gain select		

MM1763 consists of one address byte and three control data bytes (4bytes in total). All data over the limited length (5th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the separate table.

■ Switch Control Table

■ Control register 1 (2nd byte)

Control register 1								V <sub>OUT</sub> BUF	V <sub>OUT</sub> AV1	V <sub>OUT</sub> AV2	FS CTRL
b07	b06	b05	b04	b03	b02	b01	b00	select	select	select	
0	0							V <sub>IN</sub> TUN			
0	1							V <sub>IN</sub> AV1			
1	0							V <sub>IN</sub> AV2			
1	1							V <sub>IN</sub> EXT			
		0	0						V <sub>IN</sub> AV2		
		0	1						V <sub>IN</sub> TUN		
		1	0						V <sub>IN</sub> EXT		
		1	1						DAC V <sub>IN</sub>		
				0	0					V <sub>IN</sub> AV1	
				0	1					V <sub>IN</sub> TUN	
				1	0					V <sub>IN</sub> EXT	
				1	1					DAC V <sub>IN</sub>	
						0	0				Low
						0	1				Middle
						1	0				High
						1	1				High

■ Control register 2 (3rd byte)

Control register 2								L/R <sub>OUT</sub> BUF	L/R <sub>OUT</sub> AV1	L/R <sub>OUT</sub> AV2	L/R <sub>OUT</sub> BUF
b17	b16	b15	b14	b13	b12	b11	b10	select	select	select	mute
0	0							L/R <sub>IN</sub> TUN			
0	1							L/R <sub>IN</sub> AV1			
1	0							L/R <sub>IN</sub> AV2			
1	1							L/R <sub>IN</sub> EXT			
		0	0							mute	
		0	1						L/R <sub>IN</sub> TUN		
		1	0						L/R <sub>IN</sub> AV2		
		1	1						L/R <sub>IN</sub> EXT		
				0	0						mute
				0	1					L/R <sub>IN</sub> TUN	
				1	0					L/R <sub>IN</sub> AV1	
				1	1					L/R <sub>IN</sub> EXT	
							0				on
							1				off

■ Control register 3 (4th byte)

Control register 3								0/6dB	clamp/bias	V <sub>OUT</sub> mute	L/R <sub>OUT</sub> AV1	L/R <sub>OUT</sub> AV2
b27	b26	b25	b24	b23	b22	b21	b20	select	select	CTRL	gain select	gain select
0								0 dB				
1								6 dB				
	0								bias			
	1								clamp			
		0								active		
		1								mute		
			0	0							0 dB	
			0	1							2 dB	
			1	0							4 dB	
			1	1							6 dB	
					0	0						0 dB
					0	1						2 dB
					1	0						4 dB
					1	1						6 dB

[ Status registers ]

There is no preparation of the status register in MM1763. A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.

Phased Out Products

Application Circuit

