2-SCART Compatible AV Switch for DVD Recorders for Europe
Monolithic IC MM1764

Outline

This IC is a one-chip IC integrating an I^2C BUS controlled AV switch with 6 inputs and 3 outputs with a 6-channel video driver with a built-in LPF. 2 outputs among 3 outputs of the AV switch are 75Ω drivers, which is ideal for analog interface for recording equipment such as 2-SCART compatible DVD recorders for Europe.

Features

1. Serially controlled with I^2C BUS
2. Provided in a small package (QFP-64: 0.8mm pitch) with an extensive function of a switch + driver
3. 6-channel video driver including a high performance 4th-order LPF
4. Audio output that is 0dB/6dB programmable and includes a newly-developed adjustable gain amplifier
5. Includes auto power saving function when V_{CC}=12V is off (between V_{CC}=5V, 12V)

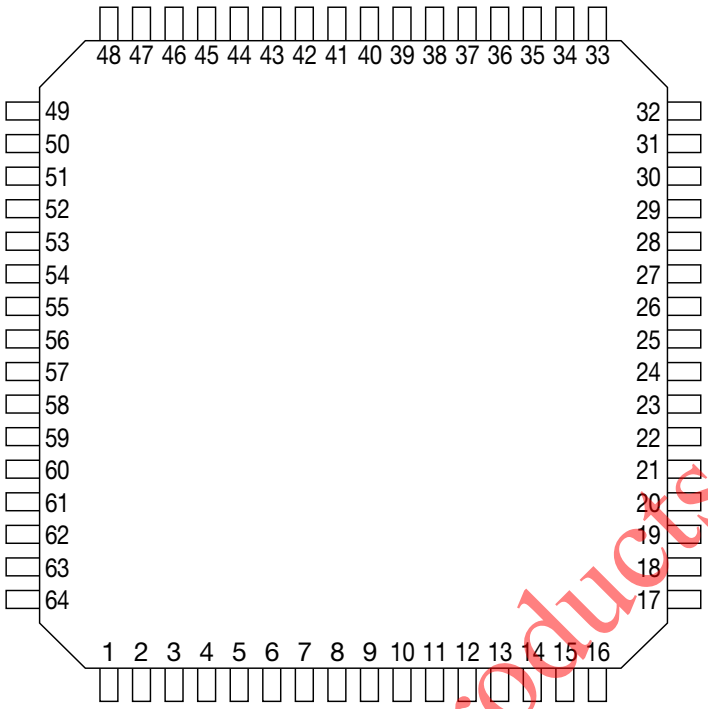
Package

QFP-64E

Applications

1. DVD recorder
2. VCR
3. STB
4. Recording equipment

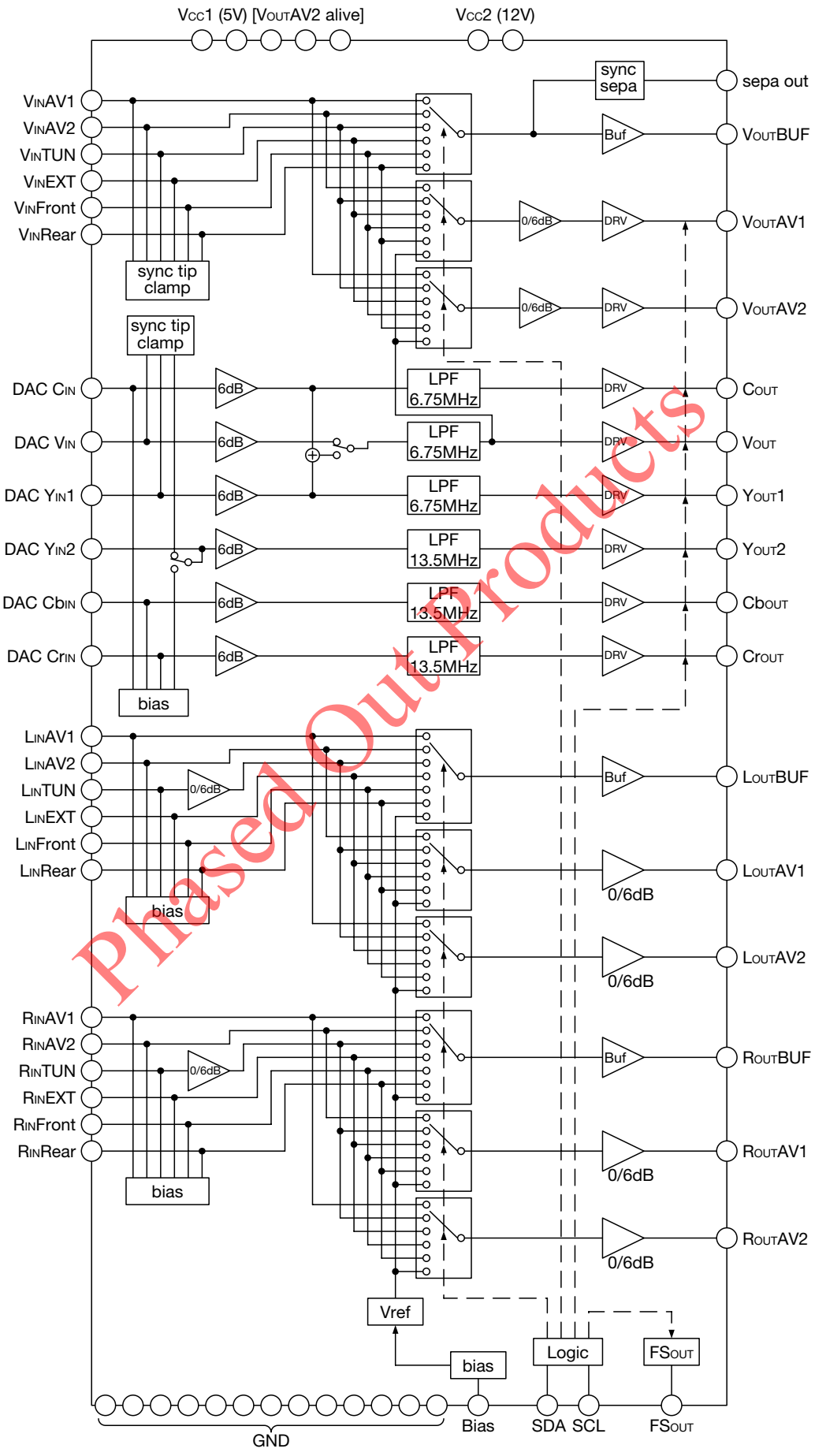
Pin Assignment



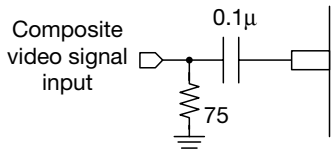
QFP-64E
(TOP VIEW)

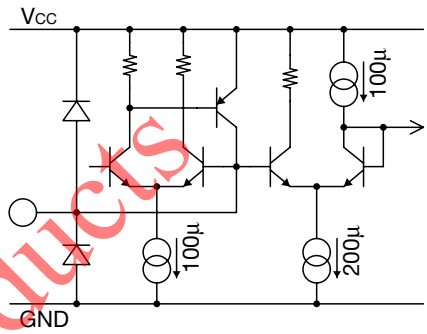
1	VINRear	17	BIAS	33	YOUT1	49	GND1
2	VCC2 (12V)	18	DAC CIN	34	VOUT	50	VOUTAV2
3	LINAV1	19	VCC1 (5V)	35	COUT	51	VOUTAV1
4	LINAV2	20	DAC VIN	36	VCC1 (5V)	52	VOUTBUF
5	LINTUN	21	GND1	37	VCC3 (5V)	53	VCC1 (5V)
6	LINEXT	22	DAC YIN1	38	SCL	54	sepa out
7	LINFront	23	GND1	39	SDA	55	GND1
8	LINRear	24	DAC YIN2	40	GND3	56	VINAV1
9	RINAV1	25	GND1	41	GND2	57	VCC1 (5V)
10	RINAV2	26	DAC CBIN	42	ROUTAV2	58	VINAV2
11	RINTUN	27	GND1	43	ROUTAV1	59	GND1
12	RINEXT	28	DAC CRIN	44	ROUTBUF	60	VINTUN
13	RINFront	29	GND1	45	LOUTAV2	61	GND1
14	RINRear	30	CROUT	46	LOUTAV1	62	VINEXT
15	GND2	31	CBOUT	47	LOUTBUF	63	GND1
16	FSOUT	32	YOUT2	48	VCC2 (12V)	64	VINFront

Block Diagram



Pin Description

<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="4">1
20
56
58
60
62
64</td><td rowspan="4">VINRear
DAC VIN
VINAV1
VINAV2
VINTUN
VINEXT
VINFront</td><td colspan="2">Function
Composite signal input
Input clamp
Pin voltage: 1.1V typ.
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit
 

When not using it: open</td><td>Equivalent circuit diagram
 
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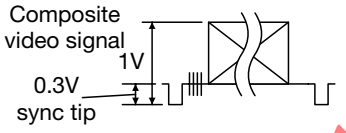
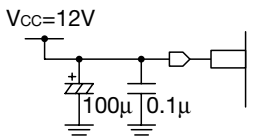
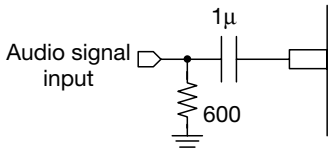
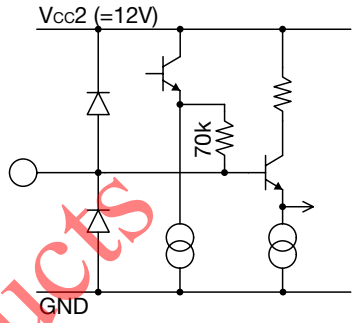
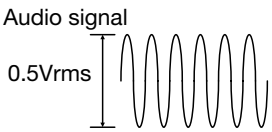
<tr><td colspan="2">Input signal
 
</td></tr>
<tr><td rowspan="4">2
48</td><td rowspan="4">VCC2</td><td colspan="2">Function
Voltage supply
It is a supply voltage impression terminal. Please impress 12V.
Please arrange a bypass capacitor near the terminal.

VCC2: Audio–VCC</td></tr>
<tr><td>External circuit
 
</td><td rowspan="2">Equivalent circuit diagram</td></tr>
<tr><td>Input signal
DC voltage:
+11.2~+12.8V</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>3
4
5
6
7
8
9
10
11
12
13
14</td><td>LINAV1
LINAV2
LINTUN
LINEXT
LINFront
LINRear
RINAV1
RINAV2
RINTUN
RINEXT
RINFront
RINRear</td><td>
Function
Audio signal input
Input impedance: 70k Ω typ.
Pin voltage: 7.0V typ.
Input dynamic range: 3Vrms min.
External circuit


When not using it: open
Equivalent circuit diagram


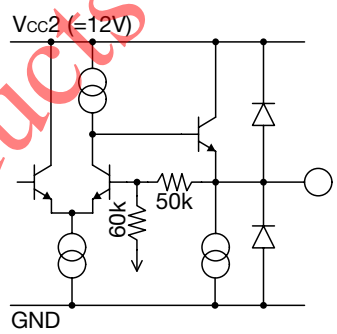
Input signal


</td></tr>
<tr><td>15
21
23
25
27
29
40
41
49
55
59
61
63</td><td>GND2
GND1
GND1
GND1
GND1
GND1
GND3
GND2
GND1
GND1
GND1
GND1
GND1</td><td>
Function
Ground
GND1: Video–GND, GND2: Audio–GND, GND3: Digital–GND
External circuit
Equivalent circuit diagram
Input signal
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>16</td><td>FSOUT</td><td>
Function
DC output for SCART interface
It is the terminal which outputs Function switch signal of SCART interface. The ternary output of L/M/H is controllable by I²C control.(refer to Switch Control Table)

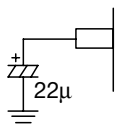
Output impedance: 500Ω typ.
Low level output voltage: 0V typ.
Middle level output voltage: 6V typ.
High level output voltage: 10V typ.

External circuit
When not using it: open

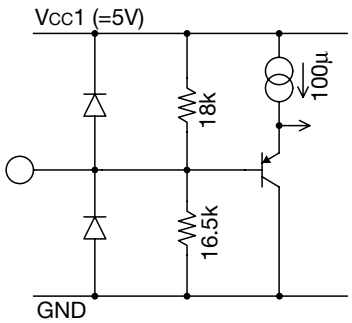
Equivalent circuit diagram


Output signal
DC voltage:
<table>
<tr><th>b01</th><th>b00</th><th colspan="2">DCOUT</th></tr>
<tr><td>0</td><td>0</td><td>L</td><td>Level 0</td></tr>
<tr><td>0</td><td>1</td><td>M</td><td>Level 1A</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">H</td><td rowspan="2">Level 1B</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>17</td><td>BIAS</td><td>
Function
BIAS
All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.

Input impedance: 8.6kΩ typ.

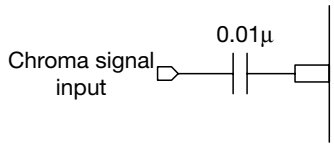
External circuit


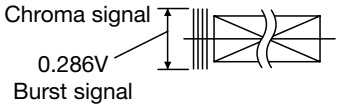
When not using it: open

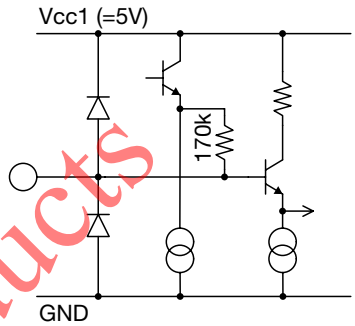
Equivalent circuit diagram


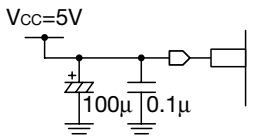
Output signal
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">18</td><td rowspan="4">DAC CIN</td><td>Function</td></tr>
<tr><td>Chroma signal input

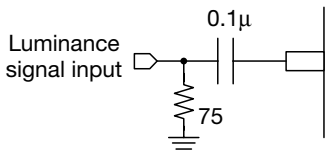
Input bias
Pin voltage: 2.4V typ.
Input impedance: 170kΩ typ.
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

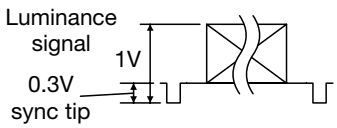
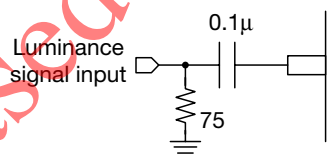
When not using it: open
Input signal:
 

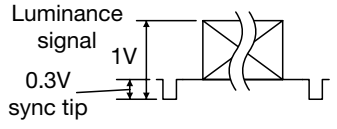
Equivalent circuit diagram:
 
</td></tr>
<tr><td>19
36
37
53
57</td><td>Vcc1
Vcc1
Vcc3
Vcc1
Vcc1</td><td>Function</td></tr>
<tr><td>Voltage supply
It is a supply voltage impression terminal. Please impress 5V.
Please arrange a bypass capacitor near the terminal.

Vcc1: Video–Vcc, Vcc3: Digital–Vcc</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>External circuit:
 

Input signal:
DC voltage:
+4.5~+5.5V
Equivalent circuit diagram:</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="5">22</td><td rowspan="5">DAC YIN1</td><td>Function
Luminance signal input
Input clamp
Pin voltage: 1.1V typ.
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

When not using it: open</td></tr>
<tr><td>Input signal</td></tr>
<tr><td> 
</td></tr>
<tr><td rowspan="5">24</td><td rowspan="5">DAC YIN2</td><td>Function
Luminance signal (G-signal) input
Input clamp or bias select
Pin voltage: 1.1V typ. (Clamp select)
2.4V typ. (Bias select)
Input dynamic range: 1.3VP-P min.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

When not using it: open</td></tr>
<tr><td>Input signal</td></tr>
<tr><td> 
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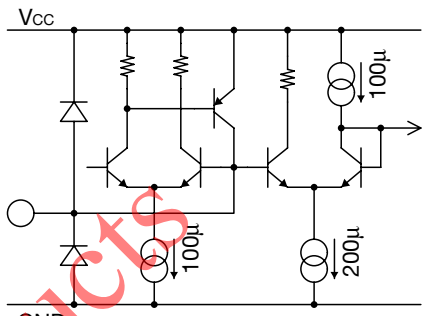
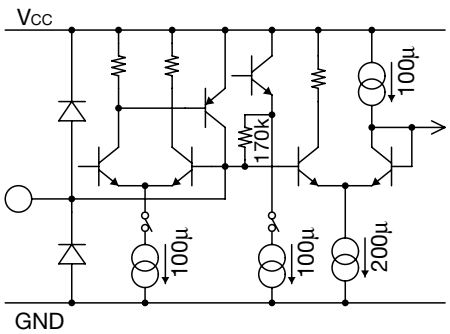
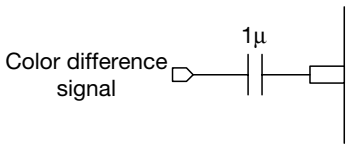
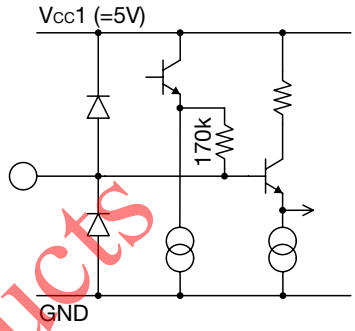
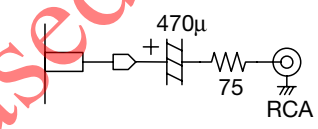
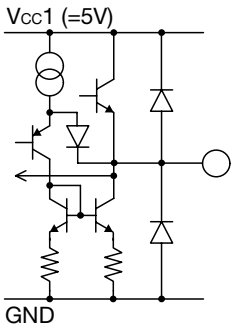




<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">26
28</td><td rowspan="2">DAC Cb_{IN}
DAC Cr_{IN}</td><td>
Function
Color difference signal input
Input bias
Pin voltage: 2.4V typ.
Input impedance: 170kΩ typ.
Input dynamic range: $1.3V_{P-P}$ min.
External circuit


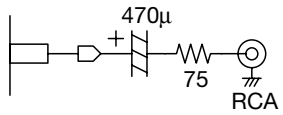
When not using it: open
Input signal
Color difference signal
0.7V
Equivalent circuit diagram


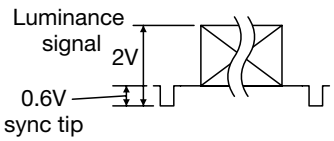
</td></tr>
<tr><td>
Function
Color difference output
It is a terminal for the Color difference signal external output.
Pin voltage: 2.4V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


When not using it: open
Output signal
Color difference signal
1.4V
Equivalent circuit diagram


</td></tr>
<tr><td>30
31</td><td>Cr_{OUT}
Cb_{OUT}</td><td></td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">32</td><td rowspan="4">YOUT2</td><td>Function</td></tr>
<tr><td>Luminance output (525p)
It is a terminal for a Luminance signal (525p) external output.

Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF</td></tr>
<tr><td>External circuit
 

When not using it: open
Output signal
 
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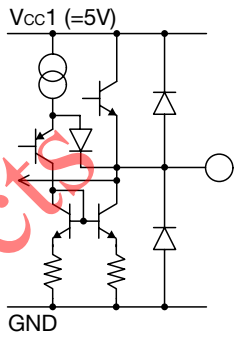
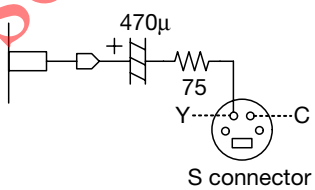
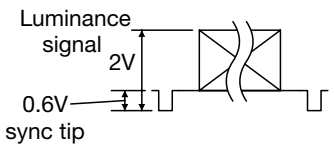
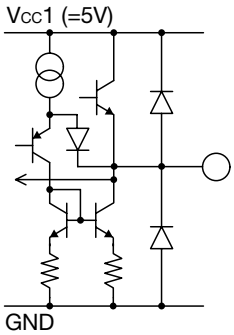
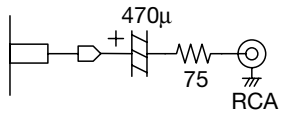
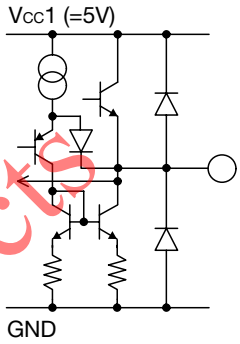
 
</td></tr>
<tr><td rowspan="4">33</td><td rowspan="4">YOUT1</td><td>Function</td></tr>
<tr><td>Luminance output (525i)
It is a terminal for a Luminance signal (525i) external output.

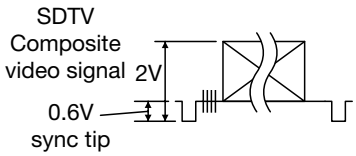
Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF</td></tr>
<tr><td>External circuit
 

When not using it: open
Output signal
 
</td><td>Equivalent circuit diagram
 
</td></tr>
</table>

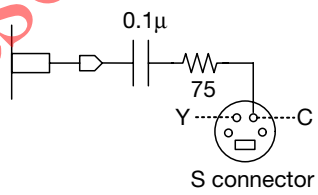
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>34
50
51</td><td>VOUT
VOUTAV2
VOUTAV1</td><td>
Function
Composite video output
It is a terminal for a composite video signal external output.

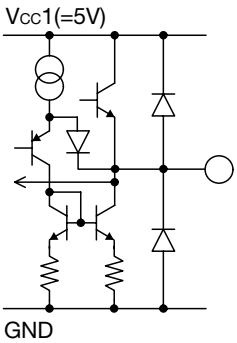
Pin voltage: 1.1V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


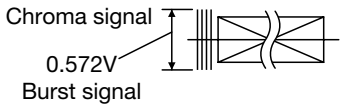
When not using it: open
Equivalent circuit diagram


Output signal


</td></tr>
<tr><td>35</td><td>COUT</td><td>
Function
Chroma output
It is a terminal for the Chroma signal external output.

Pin voltage: 2.4V typ.
Load resistance: 150Ω×2
Stray capacitance max.: 20pF
External circuit


When not using it: open
Equivalent circuit diagram


Output signal


</td></tr>
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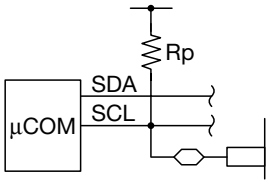
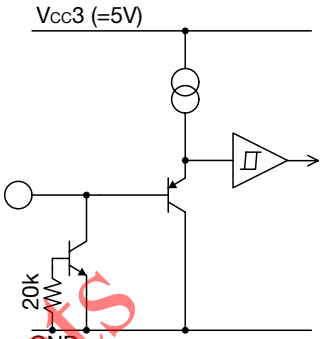
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">38</td><td rowspan="4">SCL</td><td>Function
Clock input of I²C BUS
It is the terminal which connects the SCL line of I²C BUS.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 
</td><td rowspan="2"> 
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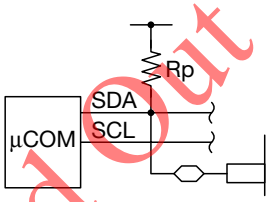
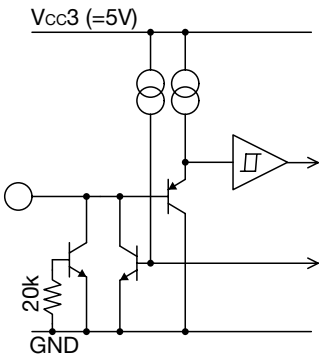
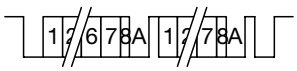
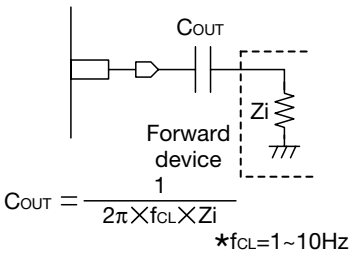
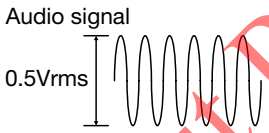
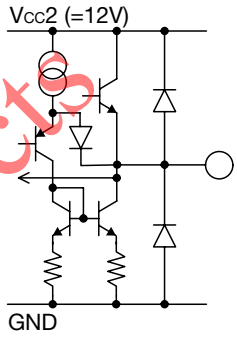
<tr><td>Input signal
Input signal
Clock signal
 
</td></tr>
<tr><td rowspan="4">39</td><td rowspan="4">SDA</td><td>Function
DATA I/O of I²C BUS
It is the terminal which connects the SDA line of I²C BUS.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 
</td><td rowspan="2"> 
</td></tr>
<tr><td>Input output signal
Input signal
Controll registers
Output signal
States registers
 
</td></tr>
</table>

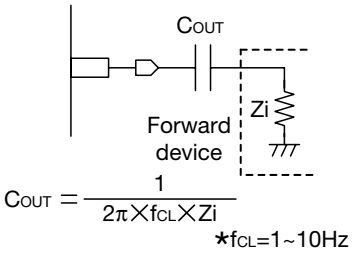
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>42
43
45
46</td><td>ROUTAV2
ROUTAV1
LOUTAV2
LOUTAV1</td><td>
Function
Audio signal output
It is a terminal for a audio signal external output.

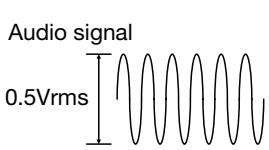
Pin voltage: 6.3V typ.
Load resistance: 600Ω max.
Stray capacitance max.: 20pF
External circuit


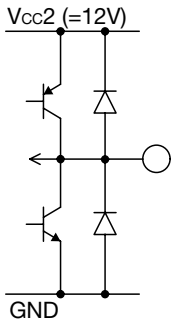
When not using it: open
Output signal


Equivalent circuit diagram


</td></tr>
<tr><td>44
47</td><td>ROUTBUF
LOUTBUF</td><td>
Function
Audio signal output
It is a terminal for a audio signal output.

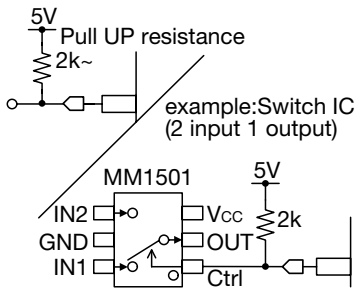
Pin voltage: 6.3V typ.
Load resistance: 1kΩ max.
Stray capacitance max.: 20pF
External circuit


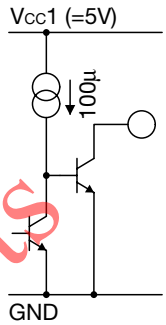
When not using it: open
Output signal


Equivalent circuit diagram


</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">54</td><td rowspan="4">sepa out</td><td>Function</td></tr>
<tr><td>Composite sync output
It is a terminal for a sync output of VOUTBUF (52pin) output signal.

Sync current: 3mA min.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>




Output signal
Composite sync
</td></tr>
</table>

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	TSTG	–55~+150	°C
Operating temperature	TOPR	–20~+75	°C
Supply voltage	VCC max.	13	V
Allowable loss	Pd	700	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	TOPR	–20~+75	°C
Vcc1 Operating voltage	VCC1OP	4.5~5.5	V
Vcc2 Operating voltage	VCC2OP	11.2~12.8	V

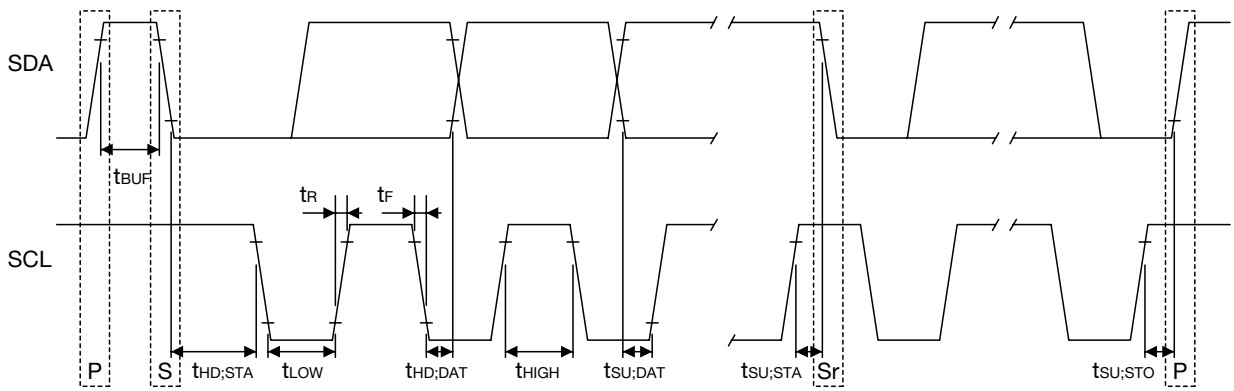
Electrical Characteristics (Except where noted otherwise Ta=25°C, V_{CC1}=5V, V_{CC2}=12V)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{CC} (5V) supply current		I_{CC1}	No signal	74	105	136	mA
V_{CC} (12V) supply current		I_{CC2}	No signal	19	27	35	mA
V_{CC} (5V) supply current at standby		I_{CC3}	No signal	21	29	37	mA
FS_{OUT} Output voltage	H	FS_H	R_L=10kΩ	9.5	10.5	12	V
	M	FS_M		4.5	6	7	V
	L	FS_L		0	0.01	2	V
Terminal voltage	Video input (clamp)	V_{INCn}		0.8	1.1	1.4	V
	Video input (bias)	V_{INBn}		2.1	2.4	2.7	V
	Audio input	A_{INn}		6.5	7.0	7.5	V
	Video output (clamp)	V_{OUTCn}			1.1		V
	Video output (bias)	V_{OUTBn}			2.4		V
	Audio output	A_{OUTn}			6.3		V
[V_{OUT}BUF]							
Voltage gain		G_{Vn}	SIN wave: 1V f=100kHz	–0.3	0	0.3	dB
Frequency characteristic		f_{Vn}	SIN wave: 1V 10MHz/100kHz	–1	0	1	dB
Output dynamic range		DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.9		V
Differential gain		DG_{Vn}	Staircase signal 1V		0.2	1	%
Differential phase		DP_{Vn}	Staircase signal 1V		0.1	1	deg
[V_{OUT}AV1, V_{OUT}AV2]							
Voltage gain		G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic		f_{Vn}	SIN wave: 1V 7MHz/100kHz	–1	0	1	dB
Output dynamic range		DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG_{Vn}	Staircase signal 1V		2	3	%
Differential phase		DP_{Vn}	Staircase signal 1V		1	2	deg
[C_{OUT}, V_{OUT}, Y_{OUT}1]							
Voltage gain		G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1		$f1_{Vn}$	SIN wave: 1V 6.75MHz/100kHz	–1	0	1	dB
Frequency characteristic 2		$f2_{Vn}$	SIN wave: 1V 27MHz/100kHz		–30	–24	dB
Output dynamic range		DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain		DG_{Vn}	Staircase signal 1V		1	2	%
Differential phase		DP_{Vn}	Staircase signal 1V		1	2	deg
Signal/Noise		SN_{Vn}	BW: 100kHz~6MHz		80		dB
Group delay		t_{Vn}	at 100kHz		50	80	ns
Group delay deviation		Δt_{Vn}	to 3.58MHz		5	10	ns
			to 4.43MHz		10	20	ns
			to 6MHz		20	28	ns

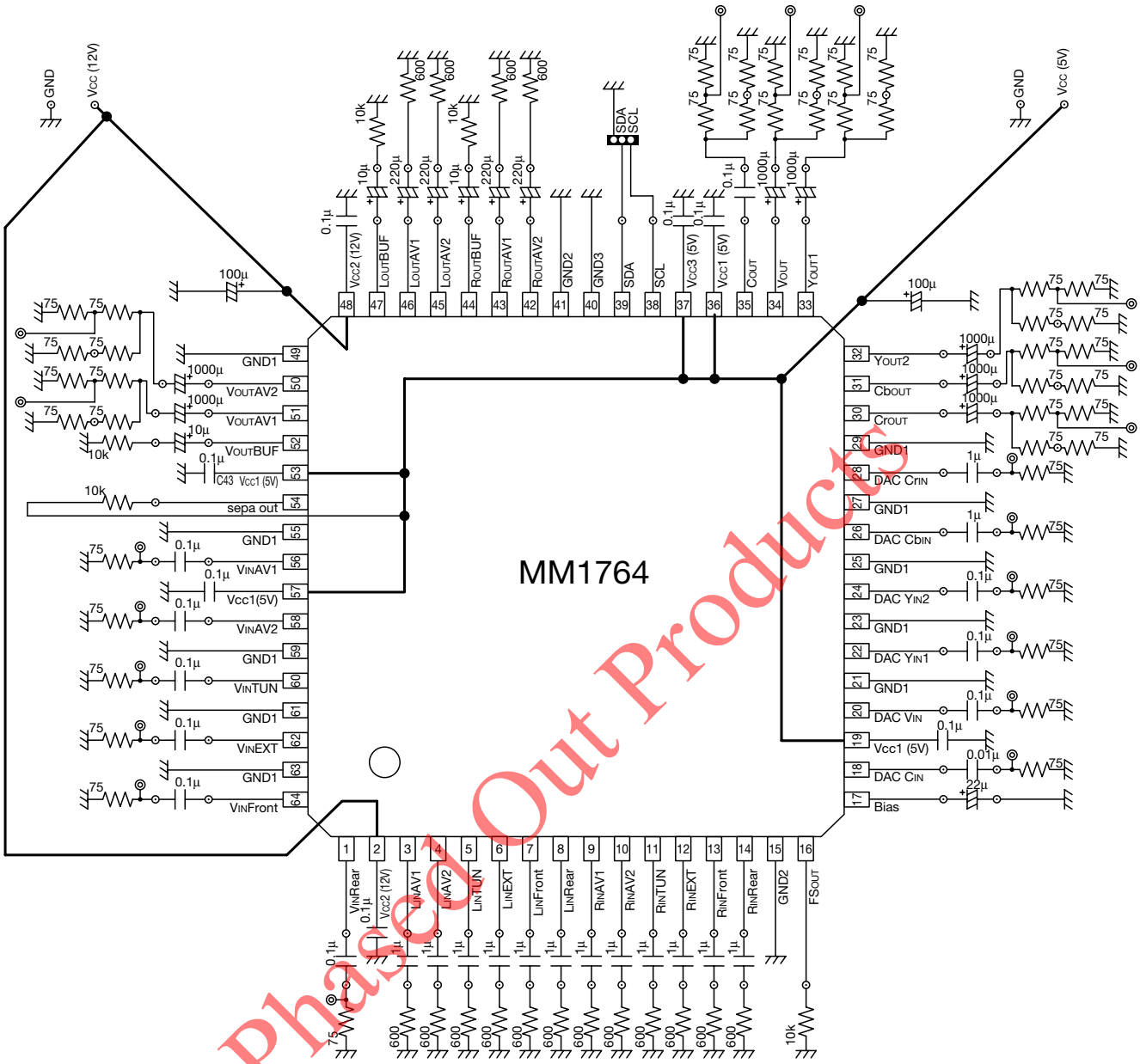
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[YOUT2, CbOUT, CrOUT]						
Voltage gain	G_{Vn}	SIN wave: 1V f=100kHz	5.7	6	6.3	dB
Frequency characteristic 1	$f1_{V\ (YOUT2)}$	100 [IRE] SIN wave + 40 [IRE] sync 13.5MHz/100kHz	–1	0	1	dB
Frequency characteristic 2	$f2_{VCbOUT, CrOUT}$	100 [IRE] SIN wave + 40 [IRE] sync 6.75MHz/100kHz	–1	0	1	dB
Frequency characteristic 3	$f3_{Vn}$	100 [IRE] SIN wave + 40 [IRE] sync 54MHz/100kHz		–30	–24	dB
Output dynamic range	DR_{Vn}	SIN wave: 100kHz THD=1%	2.6	2.8		V
Differential gain	DG_{Vn}	Staircase signal 1V		1	2	%
Differential phase	DP_{Vn}	Staircase signal 1V		1	2	deg
Signal/Noise	SN_{Vn}	BW: 100kHz~6MHz		80		dB
Group delay	t_{Vn}	at 100kHz		25	50	ns
Group delay deviation	$\Delta t1_{V\ (YOUT2)}$	to 2MHz		1	10	ns
		to 8MHz		2	10	ns
		to 12MHz		10	20	ns
Group delay deviation	$\Delta t2_{V\ (CbOUT)}$ $\Delta t2_{V\ (CrOUT)}$	to 1MHz		1	10	ns
		to 4MHz		2	10	ns
		to 6MHz		10	20	ns
[LOUTBUF, ROUTBUF]						
Voltage gain	$G0_{An}$	SIN wave: 1Vrms f=1kHz	–0.5	0	0.5	dB
	$G6_{An}$	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
Output dynamic range	DR_{An}	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion	THD_{An}	SIN wave: 1kHz V_{OUT}=1Vrms		0.005	0.05	%
Output noise voltage	VN_{An}	A curve		3.0		μVrms
Output offset voltage	VOF_{An}	at the switching		0	±15	mV
[LOUTAV1, LOUTAV2, ROUTAV1, ROUTAV2]						
Voltage gain	$G0_{An}$	SIN wave: 1Vrms f=1kHz	–0.5	0	0.5	dB
	$G6_{An}$	SIN wave: 0.5Vrms f=1kHz	5.5	6	6.5	dB
	$G12_{An}$	SIN wave: 0.25Vrms f=1kHz	11.5	12	12.5	dB
Output dynamic range	DR_{An}	SIN wave: 1kHz THD=1%	3			Vrms
Total harmonic distortion	THD_{An}	SIN wave: 1kHz V_{OUT}=1Vrms		0.005	0.05	%
Output noise voltage	VN_{An}	A curve		5		μVrms
Output offset voltage	VOF_{An}	at the switching		0	±15	mV

Item			Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Crosstalk	V_{OUT}		CT_{Vn}			–60	–50	dB
	L_{OUT}, R_{OUT}		CT_{An}			–90	–70	dB
Video input impedance			Z_{inVn}	18, (24), 26, 28 pin	120	170	220	kΩ
Audio input impedance			Z_{inAn}	L: 3~8 pin, R: 9~14 pin	50	70	90	kΩ
Output impedance			Z_{OUT}	FS_{OUT}	300	500	800	Ω
Standby $V_{CC}2$ input voltage		L	$V_{THVCC2L}$				2.0	V
		H	$V_{THVCC2H}$		3.5			V
[Sync out]								
Sync sepa level			V_{SEPA}		15	30	60	mV
Sync sepa output voltage		L	V_{SOL}	2mA sync			0.4	V
		H	V_{SOH}	10kΩ pull-up	4.8			V
[I^2C condition]								
Input voltage L			V_{IL}		0		0.7	V
Input voltage H			V_{IH}		2.1		5.0	V
SDA low level output voltage			V_{OL}	SDA sink 3mA	0		0.4	V
High level input current			I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current			I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock frequency			f_{SCL}				100	kHz
Data transfer wait time			t_{BUF}		4.7			µs
SCL start hold time			$t_{HD;STA}$		4.0			µs
SCL low level hold time			t_{LOW}		4.7			µs
SCL high level hold time			t_{HIGH}		4.0			µs
Start condition setup time			$t_{SU;STA}$		4.7			µs
SDA data hold time			$t_{HD;DAT}$		0			µs
SDA data setup time			$t_{SU;DAT}$		250			ns
SDA, SCL rise time			t_R				1000	ns
SDA, SCL fall time			t_F				300	ns
Stop condition setup time			$t_{SU;STO}$		4.0			µs

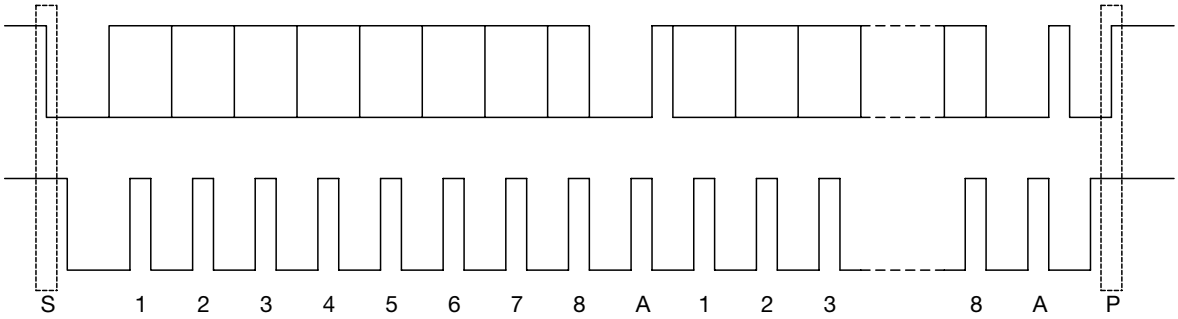
Note: I^2C condition



Measuring Circuit



I²C BUS



I²C BUS is inter IC bus system controled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.

S	Slave address							R/W	A	DATA1								A
	1	0	0	1	0	0	0	0		b07	b06	b05	b04	b03	b02	b01	b00	

Address byte — Control data byte

DATA2								A	DATA3								A	P
b17	b16	b15	b14	b13	b12	b11	b10		b27	b26	b25	b24	b23	b22	b21	b20		

Control data byte

Out of the Address byte, first 7 bits are assigned to the slave address, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used as control register. MM1764 slave address is 90H.
The next page figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

[Control data]

No.	Control DATA condition							
DATA1	b07	b06	b05	b04	b03	b02	b01	b00
	VOUTBUF select			VOUTAV1 select			FS CTRL	
DATA2	b17	b16	b15	b14	b13	b12	b11	b10
	VOUTAV2 select			L/ROUTBUF select			L/R AV1 gain	L/R AV2 gain
DATA3	b27	b26	b25	b24	b23	b22	b21	b20
	L/ROUTAV1 select			L/ROUTAV2 select			mix select	clamp bias sel

MM1764 consists of one address byte and three control data bytes (4bytes in total). All data over the limited length (5th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the separate table.

Switch Control Table

Control register 1 (2nd byte)

Control register 1								VOUTBUF select	VOUTAV1 select	FS CTRL
b07	b06	b05	b04	b03	b02	b01	b00			
0	0	0						VINTUN		
0	0	1						VINAV1		
0	1	0						VINAV2		
0	1	1						VINEXT		
1	0	0						VINFront		
1	0	1								
1	1	0								
1	1	1						VINRear		
			0	0	0				VINAV2	
			0	0	1				VINTUN	
			0	1	0				VINEXT	
			0	1	1				DAC VIN	
			1	0	0				VINFront	
			1	0	1					
			1	1	0					
			1	1	1				VINRear	
						0	0			Low
						0	1			Middle
						1	0			High
						1	1			

Control register 2 (3rd byte)

Control register 2								VOUTAV2 select	L/ROUTBUF select	L/R AV1 gain	L/R AV2 gain
b17	b16	b15	b14	b13	b12	b11	b10				
0	0	0						VINAV1			
0	0	1						VINTUN			
0	1	0						VINEXT			
0	1	1						DAC VIN			
1	0	0						VINFront			
1	0	1									
1	1	0									
1	1	1						VINRear			
			0	0	0				mute		
			0	0	1				L/RINTUN (0dB)		
			0	1	0				L/RINTUN (6dB)		
			0	1	1				L/RINAV1		
			1	0	0				L/RINAV2		
			1	0	1				L/RINEXT		
			1	1	0				L/RINFront		
			1	1	1				L/RINRear		
						0				0 dB	
						1				6 dB	
							0				0 dB
							1				6 dB

Control register 3 (4th byte)

Control register 2								L/ROUTAV1 select	L/ROUTAV2 select	MIX select	bias/clamp select
b27	b26	b25	b24	b23	b22	b21	b20				
0	0	0						mute			
0	0	1						L/RINTUN (0dB)			
0	1	0						L/RINTUN (6dB)			
0	1	1						L/RINAV2			
1	0	0						L/RINEXT			
1	0	1						L/RINFront			
1	1	0						L/RINRear			
1	1	1									
			0	0	0				mute		
			0	0	1				L/RINTUN (0dB)		
			0	1	0				L/RINTUN (6dB)		
			0	1	1				L/RINAV1		
			1	0	0				L/RINEXT		
			1	0	1				L/RINFront		
			1	1	0				L/RINRear		
			1	1	1						
						0				VIN	
						1				Y/Cmix	
							0				bias
							1				clamp

[Status registers]

There is no preparation of the status register in MM1764. A status register returns all the 1 when 1 is set in the R/W bit.

At this time, the control of each switch is not done at all.

Application Circuit