I²C Bus Control Video Switch IC
Monolithic IC MM1793XQ

Outline

With the start of the digital terrestrial broadcasting, we feel the pictures of high-definition quality familiar to ourselves. Together with the advent of the digital terrestrial broadcasting, the FPD is becoming more popular and its price has become reasonable for the consumers. FPD-TVs have beefed up with the additional functions to allow the connection of a variety of external equipment. Against these backgrounds, solutions to implement multiple inputs and multiple functions in one chip have to be developed for the video switches that input the image of high-definition quality.

This IC can support the video signal format of 1080p that is required to input the signal of high-definition image quality. In addition, it has the multiple-function circuit that are composed of 8-bit VCA, LPF switching and FLAG circuits, and this circuit can implement simple development design and the savings in the space for packaging footprint.

Features

1. Integrates the 8-bit VCA circuit that can tune variations between tuners.
2. Integrates the function to monitor the connection of the external input (FLAG function) to lower the load of the microcomputer.
3. Selectable one of three LPF cutoff frequencies so that the selected frequency can be compatible with the resolution and sampling frequency.
   (fc=6.75MHz, 13.5MHz, or 37.5MHz)

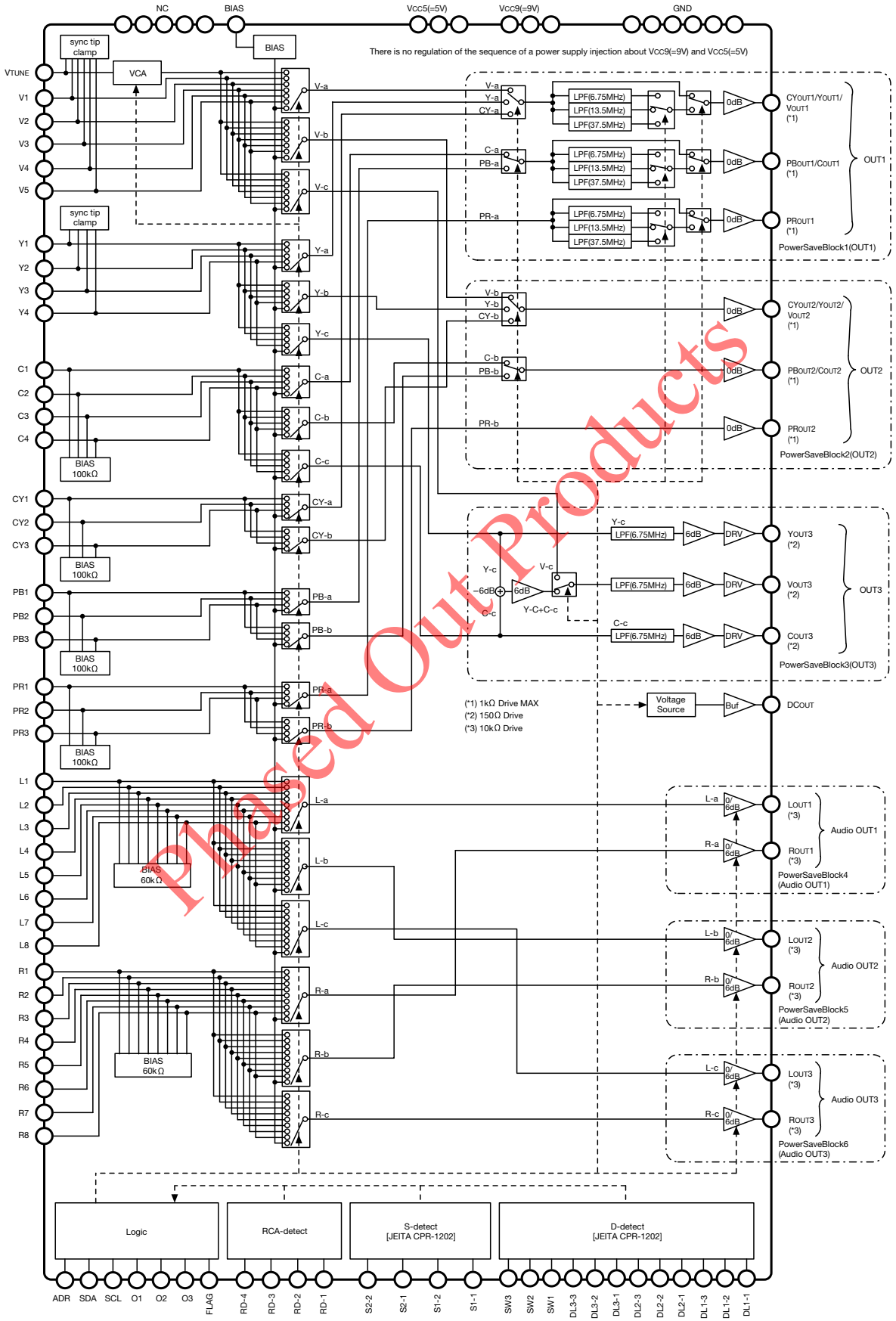
Packages

QFP-100

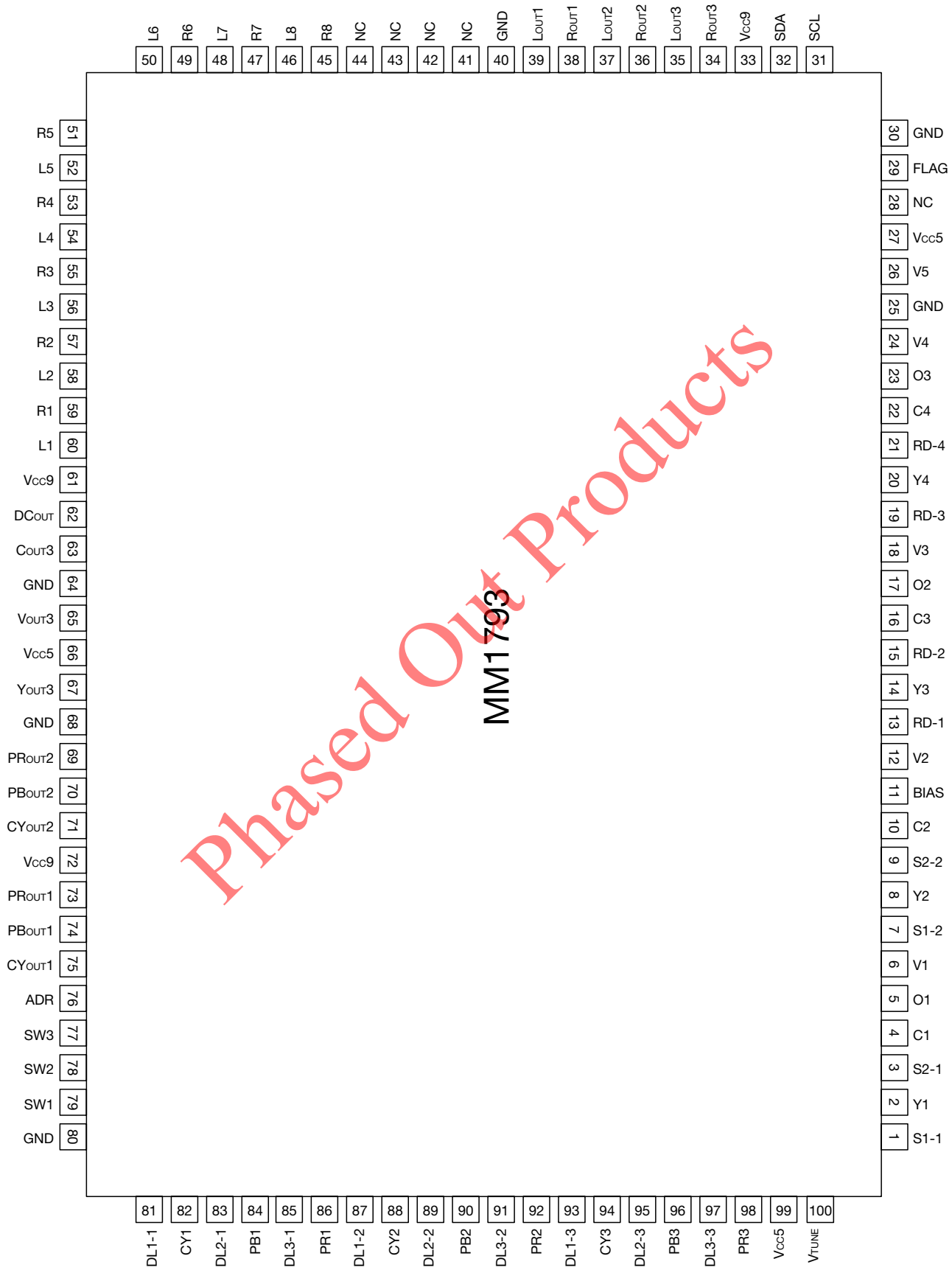
Applications

1. LCD-TV
2. PDP-TV

Block Diagram



Pin Assignment



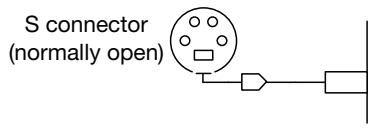
1	S1-1	21	RD-4	41	NC	61	$V_{CC}9$	81	DL1-1
2	Y1	22	C4	42	NC	62	DC_{OUT}	82	CY1
3	S2-1	23	O3	43	NC	63	$C_{OUT}3$	83	DL2-1
4	C1	24	V4	44	NC	64	GND	84	PB1
5	O1	25	GND	45	R8	65	$V_{OUT}3$	85	DL3-1
6	V1	26	V5	46	L8	66	$V_{CC}5$	86	PR1
7	S1-2	27	$V_{CC}5$	47	R7	67	$Y_{OUT}3$	87	DL1-2
8	Y2	28	NC	48	L7	68	GND	88	CY2
9	S2-2	29	FLAG	49	R6	69	$PR_{OUT}2$	89	DL2-2
10	C2	30	GND	50	L6	70	$PB_{OUT}2$	90	PB2
11	BIAS	31	SCL	51	R5	71	$CY_{OUT}2$	91	DL3-2
12	V2	32	SDA	52	L5	72	$V_{CC}9$	92	PR2
13	RD-1	33	$V_{CC}9$	53	R4	73	$PR_{OUT}1$	93	DL1-3
14	Y3	34	$R_{OUT}3$	54	L4	74	$PB_{OUT}1$	94	CY3
15	RD-2	35	$L_{OUT}3$	55	R3	75	$CY_{OUT}1$	95	DL2-3
16	C3	36	$R_{OUT}2$	56	L3	76	ADR	96	PB3
17	O2	37	$L_{OUT}2$	57	R2	77	SW3	97	DL3-3
18	V3	38	$R_{OUT}1$	58	L2	78	SW2	98	PR3
19	RD-3	39	$L_{OUT}1$	59	R1	79	SW1	99	$V_{CC}5$
20	Y4	40	GND	60	L1	80	GND	100	V_{TUNE}

Pin Description

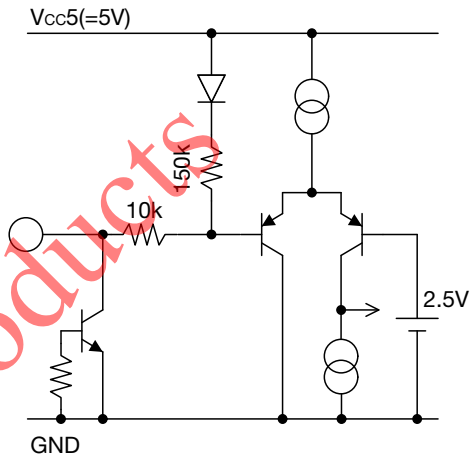
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">1
7</td><td rowspan="4">S1-1
S1-2</td><td>Function

The terminal which detects the connection state of S connector
A detected result is reflected in a status register. (refer to p.48~p.50)

threshold : 2.4V typ.
Input Impedance : 160kΩ typ.</td></tr>
<tr><td>External circuit

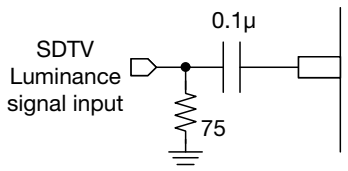
when not using it : Open</td><td rowspan="2">Equivalent circuit diagram

 
</td></tr>
<tr><td>Input signal

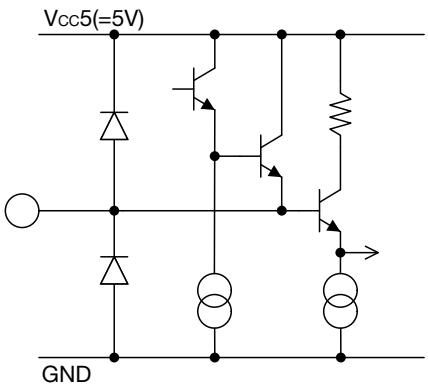
DC voltage : 0V(GND) or OPEN
Note :
When you impress voltage to a terminal, make it less than [6V].</td></tr>
<tr><td rowspan="4">2
8
14
20</td><td rowspan="4">Y1
Y2
Y3
Y4</td><td>Function

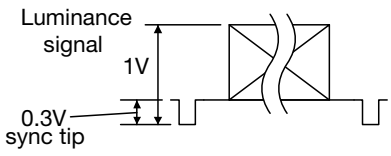
Luminance signal input

Input Clamp.
Pin Voltage : 2.2V typ.
Input Dynamic Range : 1.3 Vp-p min.</td></tr>
<tr><td>External circuit

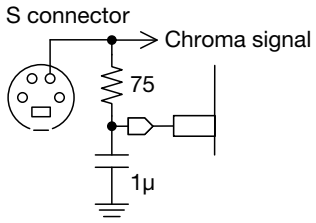
 

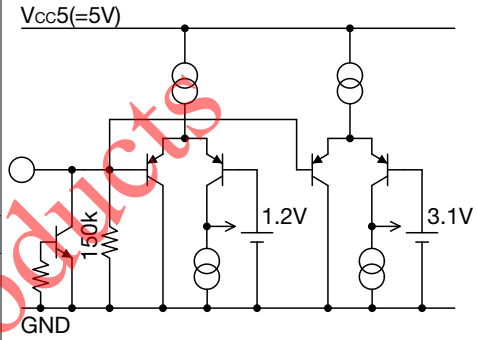
when not using it : Open</td><td rowspan="2">Equivalent circuit diagram

 
</td></tr>
<tr><td>Input signal

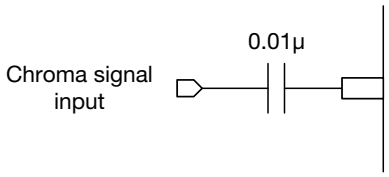
 
</td></tr>
</table>

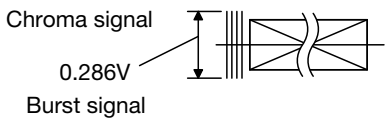
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>3
9</td><td>S2-1
S2-2</td><td>
Function
The terminal which detects the aspect ratio information of S connector.
A detected result is reflected in a status register.(refer to p.48-p.50)

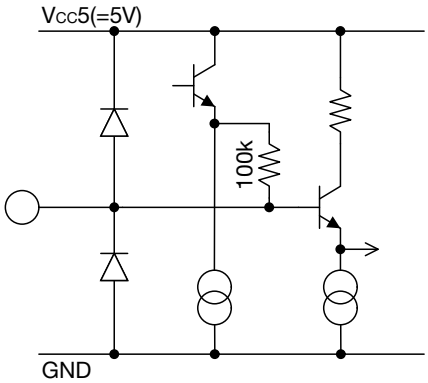
threshold1 : 1.2V typ.
threshold2 : 3.1V typ.
Input Impedance : 150kΩ typ.
External circuit


when not using it : Open
Input signal
DC voltage :
<table>
<tr><th></th><th>S2</th></tr>
<tr><td>L</td><td>0V</td></tr>
<tr><td>M</td><td>1.4–2.4V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
Equivalent circuit diagram


</td></tr>
<tr><td>4
10
16
22</td><td>C1
C2
C3
C4</td><td>
Function
Chroma signal input

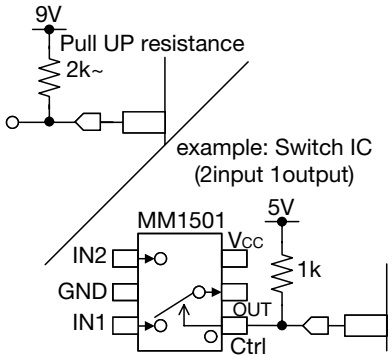
Input Bias
Pin Voltage : 2.9V typ.
Input Impedance : 100kΩ typ.
Input Dynamic Range : 1.3 Vp-p min.
External circuit


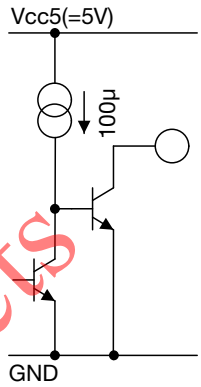
when not using it : Open
Input signal


Equivalent circuit diagram


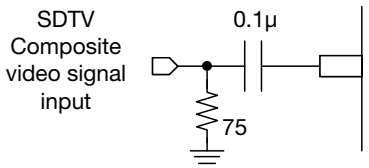
</td></tr>
</table>

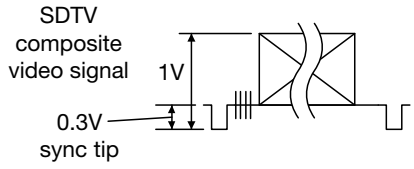
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">5
17
23</td><td rowspan="2">O1
O2
O3</td><td>
Function
Output Port
It is the open collector type general-purpose output port in which I²C control is possible.

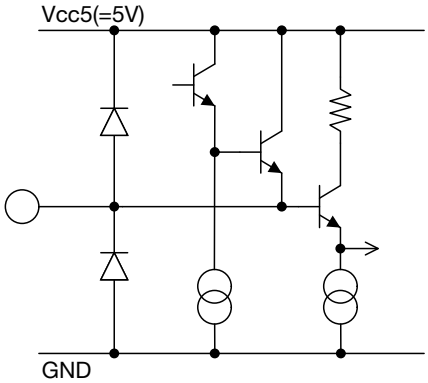
Sink Current : 5mA min.
External circuit


when not using it : Open
Equivalent circuit diagram


Output signal
DC voltage :
<table>
<tr><td>b53</td><td>O1(5pin)</td></tr>
<tr><td>0</td><td>Low</td></tr>
<tr><td>1</td><td>Open(High)</td></tr>
</table>
<table>
<tr><td>b52</td><td>O2(17pin)</td></tr>
<tr><td>0</td><td>Low</td></tr>
<tr><td>1</td><td>Open(High)</td></tr>
</table>
<table>
<tr><td>b51</td><td>O3(23pin)</td></tr>
<tr><td>0</td><td>Low</td></tr>
<tr><td>1</td><td>Open(High)</td></tr>
</table>
</td></tr>
<tr><td>6
12
18
24
26
100</td><td>V1
V2
V3
V4
V5
VTUNE</td><td>
Function
Composite signal input
Built-in VCA circuit (VTUNE Input). (refer to p.44)
Maximum Voltage gain : 1.75V typ.
Minimum Voltage gain : 0.5V typ.
Level Control sensitivity : 4.9mV/bit typ.(at 1Vp-p Input)

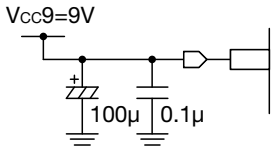
Input Clamp
Pin Voltage : 2.2V typ.
Input Dynamic Range : 1.3 Vp-p min.
External circuit


when not using it : Open
Input signal


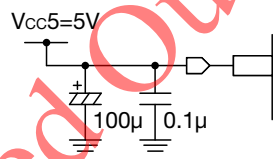
Equivalent circuit diagram


</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>33
61
72</td><td>Vcc9</td><td>
Function
Voltage Supply 1
It is a supply voltage impression terminal. Please impress 9V.
33 pin, 61 pin and 72 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about Vcc9 (9V) and Vcc5 (5V).

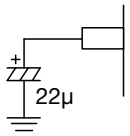
Note : Please arrange a bypass capacitor to the terminal latest as much as possible.
External circuit


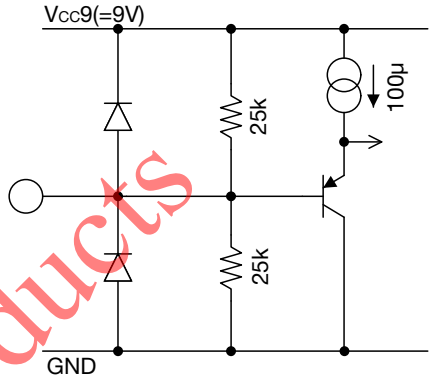
Input signal
DC voltage : +8.0V~+10.0V
Equivalent circuit diagram
—
</td></tr>
<tr><td>27
66
99</td><td>Vcc5</td><td>
Function
Voltage Supply 2
It is a supply voltage impression terminal. Please impress 5V.
27 pin, 66pin and 99 pin short-circuit inside IC.There is no regulation of the sequence of a power supply injection about Vcc9 (9V) and Vcc5 (5V).

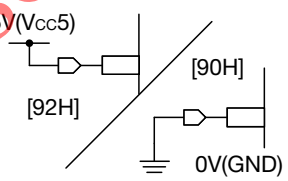
Note : Please arrange a bypass capacitor to the terminal latest as much as possible.
External circuit


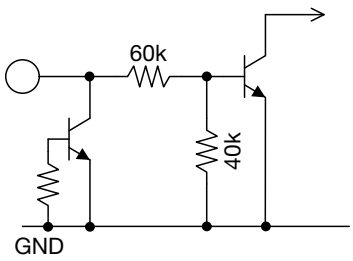
Input signal
DC voltage : +4.5V~+5.5V
Equivalent circuit diagram
—
</td></tr>
<tr><td>25
30
40
64
68
80</td><td>GND</td><td>
Function
GND
It is a GND terminal.
25pin, 30pin, 40pin, 64pin, 68pin and 80pin short-circuit inside IC.
External circuit
—
Input signal
—
Equivalent circuit diagram
—
</td></tr>
</table>

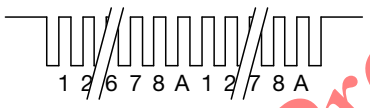
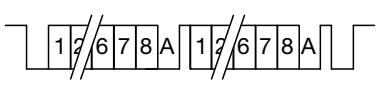
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">11</td><td rowspan="4">BIAS</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">BIAS
All the criteria voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor for criteria voltage stabilization.

Input Impedance : 12.6kΩ typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

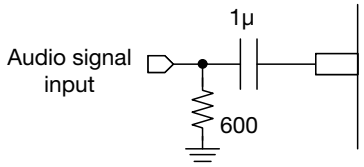
when not using it : Open
Input signal
—</td><td> 
</td></tr>
<tr><td rowspan="4">76</td><td rowspan="4">ADR</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Slave Address select pin
The I²C slave addresses 90H and 92H can be chosen with the voltage impressed to this terminal. It is set to 90H by Low, and is set to 92H by High.

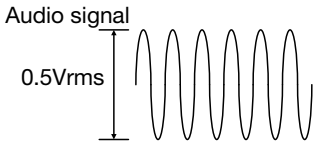
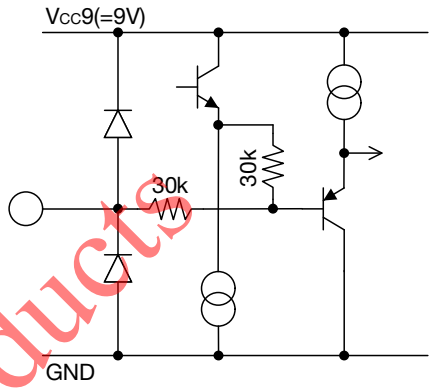
threshold : 1.75V typ.
Input Impedance : 100kΩ typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

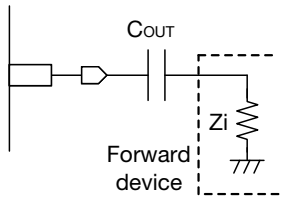
when not using it : Open
Input signal
DC voltage : 0V(GND) or 5V(Vcc5)</td><td> 
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">31</td><td rowspan="4">SCL</td><td>Function</td></tr>
<tr><td>Clock input of I²C bus
It is the terminal which connects the SCL line of I²Cbus.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>Input signal
Input signal
Clock signal
 
</td></tr>
<tr><td rowspan="4">32</td><td rowspan="4">SDA</td><td>Function</td></tr>
<tr><td>DATA I/O of I²C bus
It is the terminal which connects the SDA line of I²Cbus.</td></tr>
<tr><td>External circuit / Equivalent circuit diagram</td></tr>
<tr><td>Input signal
Input signal
Control registers
Output signal
States registers
 
</td></tr>
</table>

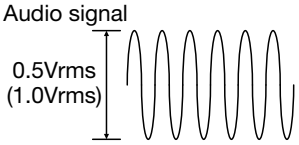
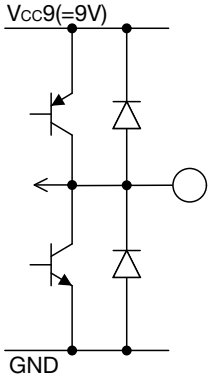
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">45~60</td><td rowspan="4">L1~L8
R1~R8</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Audio line input
Pin to input audio signals.It includes 8 channels; L1-L8, R1-R8.

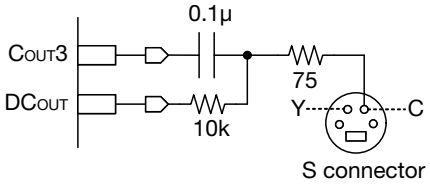
Terminal voltage : 3.80V typ.
Input Impedance : 60kΩ typ.
Input dynamic range : 3Vrms typ.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

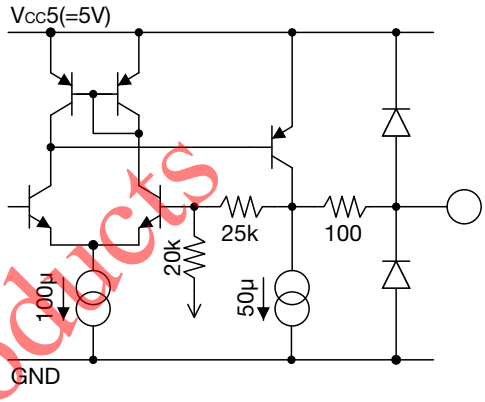
when not using it : connect to GND or Vcc9
Input signal
 
</td><td> 
</td></tr>
<tr><td rowspan="4">34~39</td><td rowspan="4">LOUT1~3
ROUT1~3</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Audio line output
Pin to output audio signals
Voltage gain of 0dB/6dB is controllable by a control registers (b44-b46).
Audio line Output1(b46=0 : 0dB mode, b46=1 : 6dB mode)
Audio line Output2(b45=0 : 0dB mode, b45=1 : 6dB mode)
Audio line Output3(b44=0 : 0dB mode, b44=1 : 6dB mode)

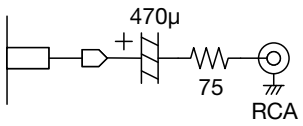
Terminal voltage : 4.50V typ.
Voltage gain : 0dB/6dB typ.
Frequency characteristic : -3dB at 50kHz min.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

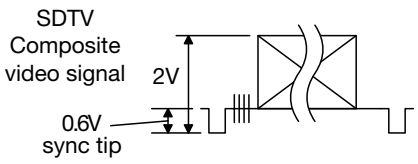
$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$
*f_{CL}=1~10Hz

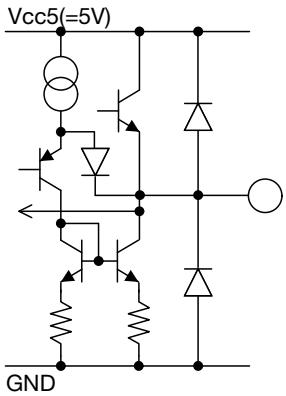
when not using it : Open
Output signal
 
</td><td> 
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">62</td><td rowspan="2">DCOUT</td><td>
Function
DC output for S terminal
It is the terminal which outputs S1/S2 signal of S terminal.
The ternary output of L/M/H is controllable by I2C control. (refer to p.44)
External circuit


when not using it : Open
Output signal
DC voltage :
<table>
<tr><th></th><th>b27</th><th>b26</th><th>DCOUT</th></tr>
<tr><td>L</td><td>0</td><td>0</td><td>0V</td></tr>
<tr><td>M</td><td>0</td><td>1</td><td>2.2V</td></tr>
<tr><td>H</td><td>1</td><td>0</td><td>5V</td></tr>
<tr><td>-</td><td>1</td><td>1</td><td>Hi-Imp</td></tr>
</table>
</td><td>
Equivalent circuit diagram


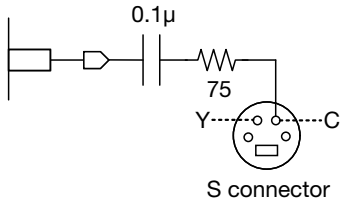
</td></tr>
<tr><td rowspan="2">65</td><td rowspan="2">VOUT3</td><td>
Function
monitor output(composite signal)
It is a terminal for a composite signal external output. V or Y+C (MIX) can be chosen. (refer to p.44)
Pin Voltage : 1.2V typ.
Load Resistance : 150Ω
Stray Capasitance : 20pF max.
External circuit


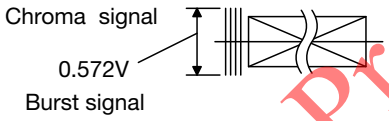
when not using it : Open
Output signal


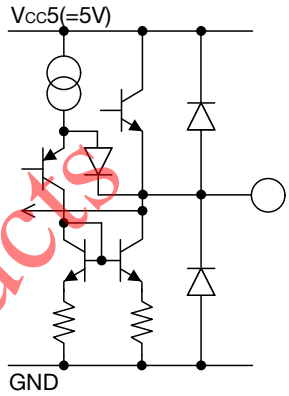
</td><td>
Equivalent circuit diagram


</td></tr>
</table>

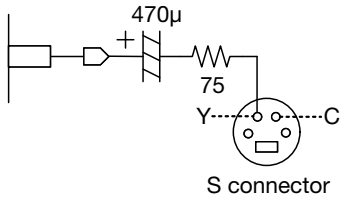
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">63</td><td rowspan="2">COUT3</td><td>
Function
monitor output (chroma signal)
It is a terminal for the chroma signal external output.

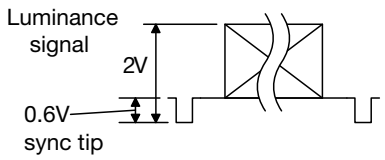
Pin Voltage : 2.4V typ.
Load Resistance : 150Ω
Stray Capasitance : 20pF max.
External circuit


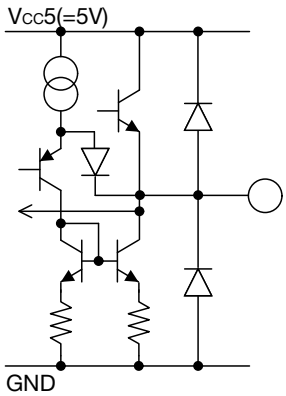
when not using it : Open
Output signal


</td><td>
Equivalent circuit diagram


</td></tr>
<tr><td colspan="2"></td></tr>
<tr><td rowspan="2">67</td><td rowspan="2">YOUT3</td><td>
Function
monitor output (Luminance signal)
It is a terminal for a Luminance signal external output.

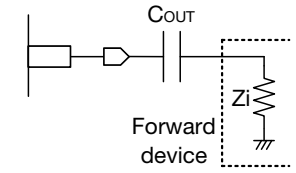
Pin Voltage : 1.2V typ.
Load Resistance : 150Ω
Stray Capasitance : 20pF max.
External circuit


when not using it : Open
Output signal


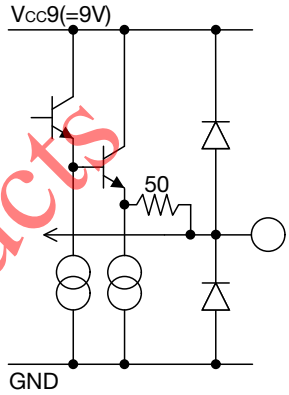
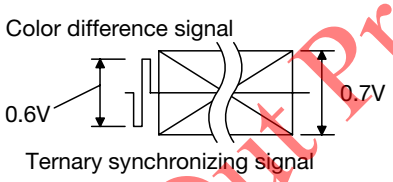
</td><td>
Equivalent circuit diagram


</td></tr>
<tr><td colspan="2"></td></tr>
</table>

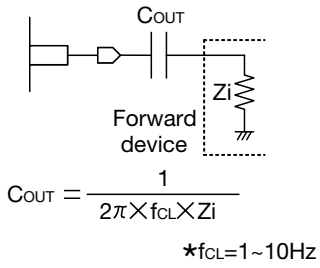
<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="4">69</td><td rowspan="4">PROUT2</td><td colspan="2">Function
Color difference signal output
It is a terminal for a Color difference signal external output.

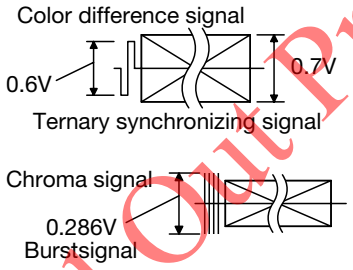
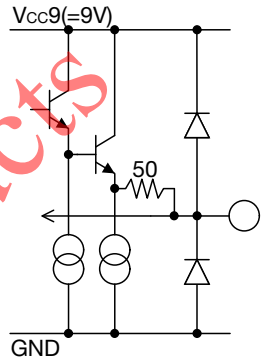
Pin Voltage : 2.4V typ.
Load Resistance : 1kΩ min.
Stray Capasitance : 10pF max.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$
*f_{CL}=1~10Hz

when not using it : Open</td><td> 
</td></tr>
<tr><td>Output signal</td><td></td></tr>
<tr><td> 
</td><td></td></tr>
</table>

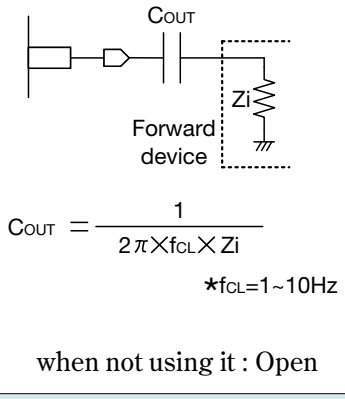
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="5">70</td><td rowspan="5">PBOUT2
/COUT2</td><td>Function</td></tr>
<tr><td>Color difference signal or Chroma signal output
It is a terminal for a Color difference or Chroma signal external output.

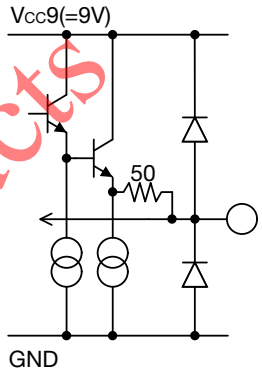
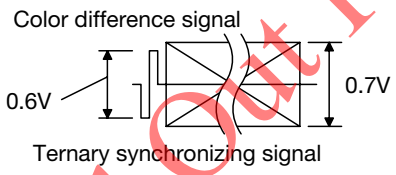
Pin Voltage : 2.4V typ.
Load Resistance : 1kΩ min.
Stray Capasitance : 10pF max.</td></tr>
<tr><td>External circuit</td></tr>
<tr><td> 

when not using it : Open</td></tr>
<tr><td>Output signal</td></tr>
<tr><td> 
</td></tr>
<tr><td colspan="2">Equivalent circuit diagram</td></tr>
<tr><td colspan="2"> 
</td></tr>
</table>

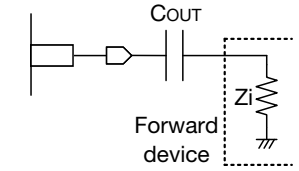
Pin No.	Pin name	Pin description
71	CYOUT2 /YOUT2 /VOUT2	**Function** Color difference signal, Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output. Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capasitance : 10pF max. **External circuit** / **Equivalent circuit diagram** COUT, Zi, Forward device $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$ *f_{CL}=1~10Hz when not using it : Open **Output signal** 1V, Component Y signal, 0.6V, Ternary synchronizing signal Luminance signal, 1V, 0.3V sync tip SDTV Composite video signal, 1V, 0.3V sync tip Vcc9(=9V), 50, GND

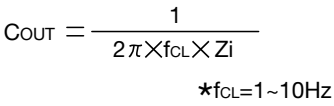
<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="5">73</td><td rowspan="5">PROUT1</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Color difference signal output
It is a terminal for a Color difference signal external output.

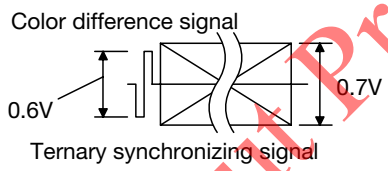
Pin Voltage : 2.4V typ.
Load Resistance : 1kΩ min.
Stray Capasitance : 10pF max.</td></tr>
<tr><td>External circuit</td><td>Equivalent circuit diagram</td></tr>
<tr><td> 

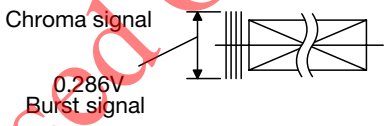
when not using it : Open</td><td rowspan="2"> 
</td></tr>
<tr><td>Output signal</td></tr>
<tr><td colspan="2"> 
</td></tr>
</table>

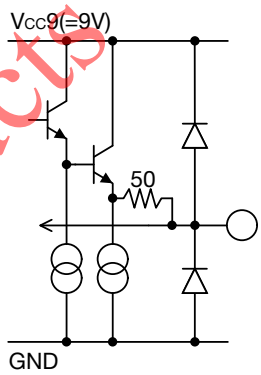
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">74</td><td rowspan="4">PBOUT1
/COUT1</td><td>
Function
Color difference signal or Chroma signal output
It is a terminal for a Color difference or Chroma signal external output.

Pin Voltage : 2.4V typ.
Load Resistance : 1kΩ min.
Stray Capasitance : 10pF max.
</td></tr>
<tr><td>
External circuit




when not using it : Open
</td></tr>
<tr><td>
Output signal


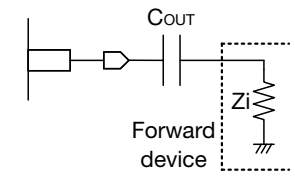


</td></tr>
<tr><td>
Equivalent circuit diagram


</td></tr>
</table>

Pin No.	Pin name	Pin description
75	CYOUT1 /YOUT1 /VOUT1	**Function** Color difference signal , Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output. Pin Voltage : 2.4V typ. Load Resistance : 1kΩ min. Stray Capasitance : 10pF max.

External circuit

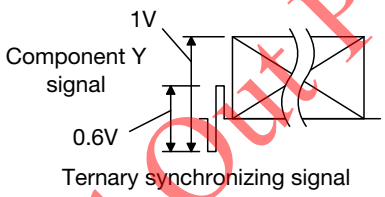


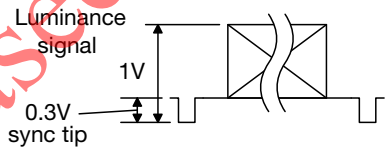
$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Zi}$$

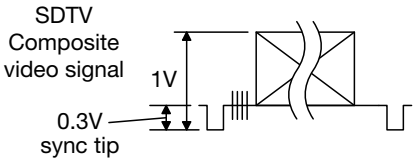
*f_{CL}=1~10Hz

when not using it : Open

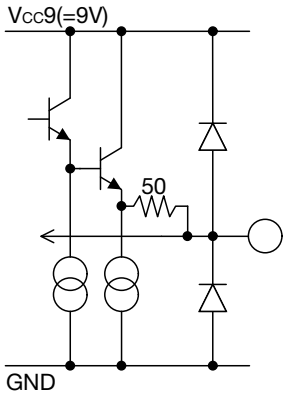
Output signal



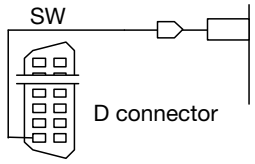




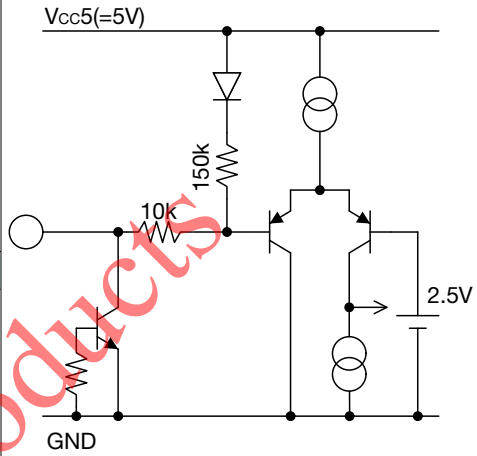
Equivalent circuit diagram



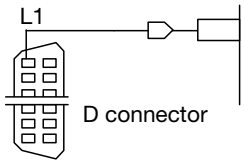
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td>77
78
79</td><td>SW3
SW2
SW1</td><td>
Function
The terminal which detects the connection state of D connector.
A detected result is reflected in a status register. (refer to p.48-p.50)

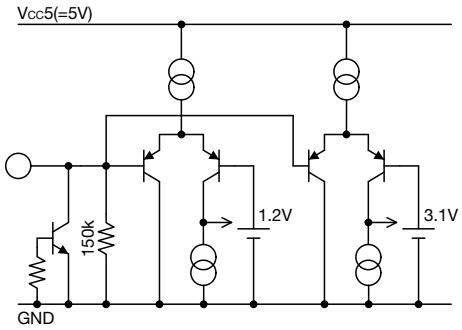
threshold : 2.4V typ.
Input Impedance : 160kΩ typ.
External circuit


when not using it : Open
Input signal
DC voltage : 0V (GND) or OPEN

Note : When you impress voltage to a terminal, make it less than [6V].
Equivalent circuit diagram


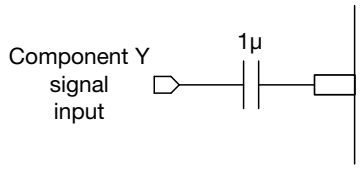
</td></tr>
<tr><td>81
87
93</td><td>DL1-1
DL1-2
DL1-3</td><td>
Function
The terminal which detects the number-of-scanning-lines information on D connector.
A detected result is reflected in a status register.(refer to p.48-50)

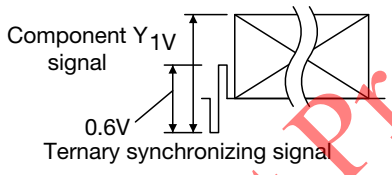
threshold1 : 1.2V typ.
threshold2 : 3.1V typ.
Input Impedance : 150kΩ typ.
External circuit


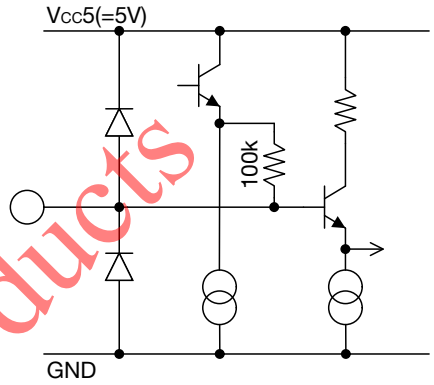
when not using it : Open
Input signal
DC voltage :
<table>
<tr><td>L</td><td>0V</td></tr>
<tr><td>M</td><td>1.4–2.4V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
Equivalent circuit diagram


</td></tr>
</table>

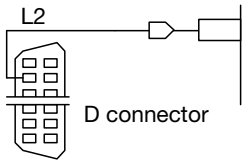
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">82
88
94</td><td rowspan="2">CY1
CY2
CY3</td><td>
Function
Component Y signal input
A RGB signal can also be inputted besides a component Y signal.

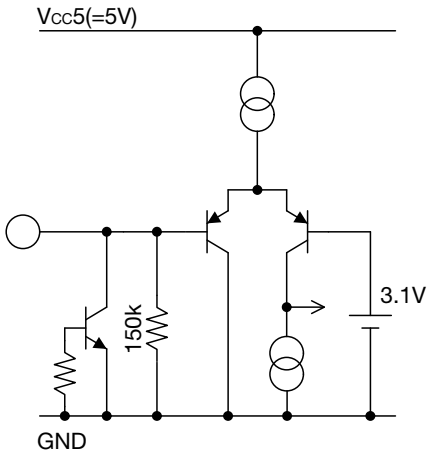
Input Bias
Pin Voltage : 2.9V typ.
Input Impedance : 100kΩ typ.
Input Dynamic Range : 1.6 Vp-p min.
External circuit


when not using it : Open
Input signal


</td><td>
Equivalent circuit diagram


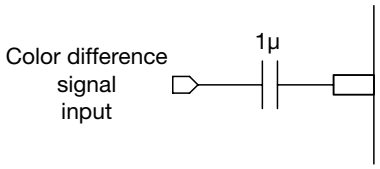
</td></tr>
<tr><td colspan="2"></td></tr>
<tr><td rowspan="2">83
89
95</td><td rowspan="2">DL2-1
DL2-2
DL2-3</td><td>
Function
The terminal which detects the I/P information of D connector.
A detected result is reflected in a status register. (refer to p.48-p.50)

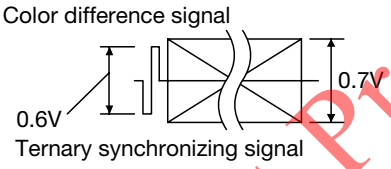
threshold : 3.1V typ.
Input Impedance : 150kΩ typ.
External circuit


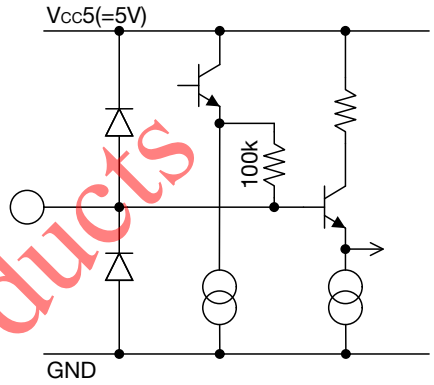
when not using it : Open
Input signal
DC voltage :
<table>
<tr><td></td><td>L2</td></tr>
<tr><td>L</td><td>0V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
</td><td>
Equivalent circuit diagram


</td></tr>
<tr><td colspan="2"></td></tr>
</table>

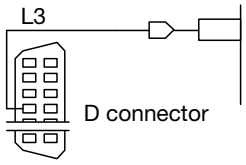
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">84
90
96</td><td rowspan="2">PB1
PB2
PB3</td><td>
Function
Color difference signal input
A RGB signal can also be inputted besides a color-difference signal.

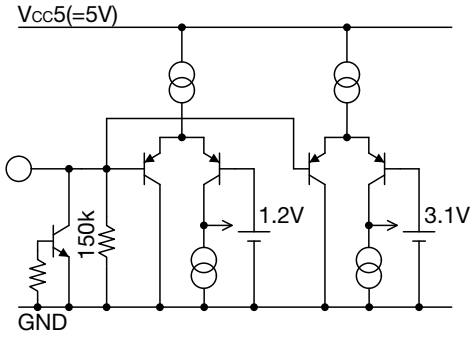
Input Bias
Pin Voltage : 2.9V typ.
Pin Voltage : 100kΩ typ.
Input Impedance : 1.6 Vp-p typ.
External circuit


when not using it : Open
Input signal


Equivalent circuit diagram


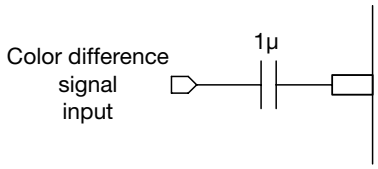
</td></tr>
<tr><td>
Function
The terminal which detects the aspect ratio information of D connector.
A detected result is reflected in a status register. (refer to p.48-p.50)

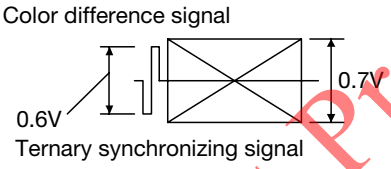
threshold1 : 1.2V typ.
threshold2 : 3.1V typ.
Input Impedance : 150kΩ typ.
External circuit


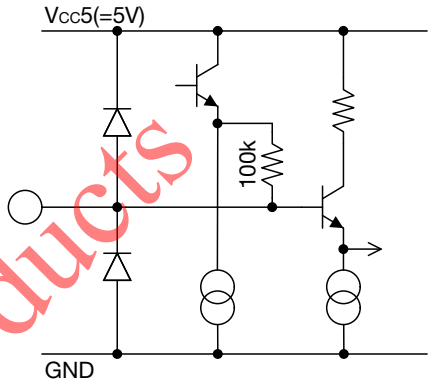
when not using it : Open
Input signal
DC voltage :
<table>
<tr><th></th><th>L3</th></tr>
<tr><td>L</td><td>0V</td></tr>
<tr><td>M</td><td>1.4–2.4V</td></tr>
<tr><td>H</td><td>3.5–5V</td></tr>
</table>
Equivalent circuit diagram


</td></tr>
<tr><td>85
91
97</td><td>DL3-1
DL3-2
DL3-3</td><td></td></tr>
</table>

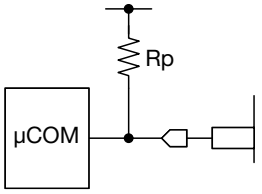
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="2">86
92
98</td><td rowspan="2">PR1
PR2
PR3</td><td>
Function
Color difference signal input
A RGB signal can also be inputted besides a color-difference signal.

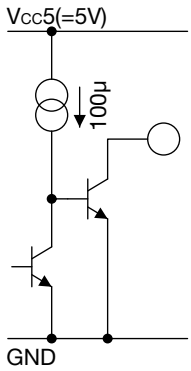
Input Bias
Pin Voltage : 2.9V typ.
Input Impedance : 100kΩ typ.
Input Dynamic Range : 1.6 Vp-p typ.
External circuit


when not using it : Open
Input signal


Equivalent circuit diagram


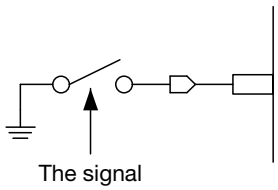
</td></tr>
<tr><td>29</td><td>FLAG</td><td>
Function
The output terminal which monitor and detects a status register
When status register information changes, an output is changed to Low.
When status register information is readed, an output is changed to Open.
It is the open collector type output port.(refer to p.50)

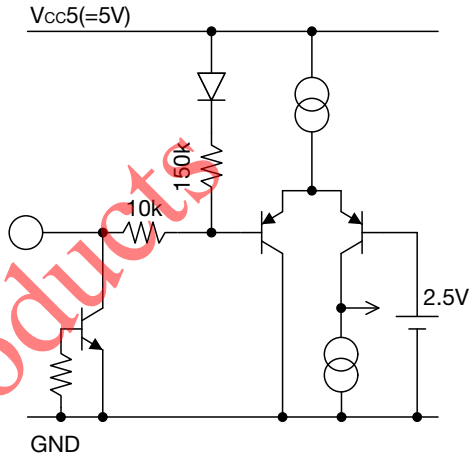
Sink Current : 5mA min.
External circuit


when not using it : Open
Equivalent circuit diagram


Output signal
DC voltage :
<table>
<tr><td>Status register information</td><td>FLAG(29pin)</td></tr>
<tr><td>change</td><td>Low</td></tr>
<tr><td>readed</td><td>Open(High)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">13
15
19
21</td><td rowspan="4">RD-1
RD-2
RD-3
RD-4</td><td>Function
The terminal which detects the connection state of RCA connector
A detected result is reflected in a status register. (refer to p.48-p.50)

threshold : 2.4V typ.
Input Impedance : 160kΩ typ.</td></tr>
<tr><td>External circuit
 

when not using it : Open</td><td>Equivalent circuit diagram
 
</td></tr>
<tr><td>Input signal
DC voltage : 0V (GND) or OPEN

Note : When you impress voltage to a terminal, make it less than [6V].</td><td></td></tr>
<tr><td></td></tr>
<tr><td rowspan="4">28
41
42
43
44</td><td rowspan="4">NC</td><td>Function
None Connection terminal</td></tr>
<tr><td>External circuit
—</td><td>Equivalent circuit diagram
—</td></tr>
<tr><td>Input signal
—</td><td></td></tr>
<tr><td></td></tr>
</table>

Absolute Maximum Ratings (Except where noted otherwise, Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−65~+150	°C
Operating temperature	T_{OPR}	−40~+85	°C
Supply voltage 1	V_{CC9MAX}	−0.2~+10.0	V
Supply voltage 2	V_{CC5MAX}	−0.2~+6.0	V
Input voltage 1	V_{IN1MAX}	−0.2~V_{CC9}+0.2	V
Input voltage 2	V_{IN2MAX}	−0.2~V_{CC5}+0.2	V
Output voltage 1	$V_{OUT9MAX}$	−0.2~V_{CC9}+0.2	V
Output voltage 2	$V_{OUT5MAX}$	−0.2~V_{CC5}+0.2	V
Output current	I_{OUTMAX}	25	mA
Junction temperature	T_{jMAX}	150	°C
Thermal resistance	θ j-c	6.0	°C/W
Power dissipation (Note1)	Pd	3.6	W

Note1 : Board mounting power dissipation. Board size 193×189×1.6mm

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	−40~+85	°C
Operating voltage 1	V_{CC9OP}	+8.0~+10.0	V
Operating voltage 2	V_{CC5OP}	+4.5~+5.5	V

Electrical Characteristics (Except where noted otherwise, Ta=25°C, $V_{CC}9$=9V, $V_{CC}5$=5V,VCA GAIN SELECT='66H')

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Current consumption							
Current consumption	$V_{CC}9$ (9V)	$I_{CC9\text{-}0}$	[I²C BUS DATA= ' ALL 0 ']	36	60	84	mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}0}$		60	100	140	
All Power save Current consumption							
Current consumption (at All PS mode)	$V_{CC}9$ (9V)	$I_{CC9\text{-}0}$	[b05,b15,b25,b56,b55,b54 = ' 1,1,1,1,1,1 ']	5	10	15	mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}0}$		30	50	70	
Block Current consumption							
Current consumption (at OUT1 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V1}$	Icc[b05 = ' 0 ']–Icc[b05 = ' 1 ']		30		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V1}$			15		
Current consumption (at OUT2 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V2}$	Icc[b15 = ' 0 ']–Icc[b15 = ' 1 ']		15		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V2}$			5		
Current consumption (at OUT3 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}V3}$	Icc[b25 = ' 0 ']–Icc[b25 = ' 1 ']		0		mA
	$V_{CC}5$ (5V)	$I_{CC5\text{-}V3}$			30		
Current consumption (at AUDIO OUT1 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A1}$	Icc[b56 = ' 0 ']–Icc[b56 = ' 1 ']		4		mA
Current consumption (at AUDIO OUT2 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A2}$	Icc[b55 = ' 0 ']–Icc[b55 = ' 1 ']		4		mA
Current consumption (at AUDIO OUT3 block)	$V_{CC}9$ (9V)	$I_{CC9\text{-}A3}$	Icc[b54 = ' 0 ']–Icc[b54 = ' 1 ']		4		mA

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Input pin voltage							
Input pin voltage 1 (V,Y)		V_{in1}	100,6,12,18,24,26,2,8,14,20 pin	1.7	2.2	2.7	V
Input pin voltage 2 (C,CY,PB,PR)		V_{in2}	4,10,16,22,82,84,86,88,90,92,94,96,98 pin	2.3	2.9	3.5	V
Input pin voltage 3 (L,R)		V_{in3}	45 ~ 60 pin	3.2	3.8	4.4	V
Output pin voltage (OUT1,2)							
Output pin voltage 1		V_{out1}	69,70,71,73,74,75 pin	2.0	2.4	2.8	V
Output pin voltage (OUT3)							
Output pin voltage 2 (V,Y)		V_{out2}	65,67 pin	0.8	1.2	1.6	V
Output pin voltage 3 (C)		V_{out3}	63 pin	2.0	2.4	2.8	V
Output pin voltage (Audio OUT1,2,3)							
Audio output pin voltage (L,R)		V_{out4}	34 ~ 39 pin	4.1	4.5	4.9	V
S-DCOUT pin output voltage							
S-DCOUT pin output voltage	L	$V_{DCOUT\,L}$	62 pin RL=10kΩ+100kΩ	GND	0.1	0.5	V
	M	$V_{DCOUT\,M}$	62 pin RL=10kΩ+100kΩ	1.6	2.1	2.4	V
	H	$V_{DCOUT\,H}$	62 pin RL=10kΩ+100kΩ	4.3	4.6	$V_{CC}5$	V
Bias input impedance							
CIN input impedance		Z_{CIN}	4,10,16,22 pin	70	100	130	kΩ
CYIN input impedance		Z_{CYIN}	82,88,94 pin	70	100	130	kΩ
PbIN input impedance		Z_{PbIN}	84,90,96 pin	70	100	130	kΩ
PrIN input impedance		Z_{PrIN}	86,92,98 pin	70	100	130	kΩ
LIN input impedance		Z_{LIN}	60,58,56,54,52,50,48,46 pin	47	60	73	kΩ
RIN input impedance		Z_{RIN}	59,57,55,53,51,49,47,45 pin	47	60	73	kΩ

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V_{TUNE} (100pin) electrical characteristics							
VCA Maximum Voltage gain		Gv_{VCAmax}	Vout (V_{TUNE}=Vin1+1V) –Vout (V_{TUNE}=Vin1) 71,75 pin [VCA GAIN SELECT='FFH']	1.40	1.75	2.10	V
VCA Minimum Voltage gain		Gv_{VCAmin}	Vout (V_{TUNE}=Vin1+1V) –Vout (V_{TUNE}=Vin1) 71,75 pin [VCA GAIN SELECT='00H']	0.40	0.50	0.60	V
VCA Level Control sensitivity		S_{VCA}	SIN wave : 1V f=100kHz 71,75 pin	0	4.9	9.8	mV/bit
VCA Level linearity error (Note2)		LE_{VCA}	SIN wave : 1V f=100kHz 71,75 pin	–1.5		1.5	LSB
VOUT3 (65pin) electrical characteristics							
VOUT3 Voltage gain		Gv_{VOUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB
VOUT3 Frequency characteristic	with filter	$f1_{VOUT3}$	SIN wave : 1V 6.75MHz/100kHz	–1.0	0.0	1.0	dB
		$f2_{VOUT3}$	SIN wave : 1V 27MHz/100kHz		–33.0	–24.0	dB
VOUT3 Input dynamic range		DR_{VOUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V
VOUT3 Group delay	with filter	$t_{GD\ VOUT3}$	at 100kHz		55		ns
VOUT3 Group delay deviation 1	with filter	$\Delta t1_{GD\ VOUT3}$	to 3.58MHz		4	20	ns
VOUT3 Group delay deviation 2	with filter	$\Delta t2_{GD\ VOUT3}$	to 4.43MHz		6	20	ns
VOUT3 Group delay deviation 3	with filter	$\Delta t3_{GD\ VOUT3}$	to 6MHz		13	20	ns
VOUT3 Crosstalk		CT_{VOUT3}	SIN wave : 1V f=4.43MHz		–60	–55	dB

Note2 : VCA Level linearity error 1LSB=(GvVCAmax-GvVCAmin)/255

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
YOUT3 (67pin) electrical characteristics							
YOUT3 Voltage gain		Gv_{YOUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB
YOUT3 Frequency characteristic	with filter	$f1_{YOUT3}$	SIN wave : 1V 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		$f2_{YOUT3}$	SIN wave : 1V 27MHz/100kHz		−33.0	−24.0	dB
YOUT3 Input dynamic range		DR_{YOUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V
YOUT3 Group delay	with filter	$t_{GD\ YOUT3}$	at 100kHz		55		ns
YOUT3 Group delay deviation 1	with filter	$\Delta t1_{GD\ YOUT3}$	to 3.58MHz		4	20	ns
YOUT3 Group delay deviation 2	with filter	$\Delta t2_{GD\ YOUT3}$	to 4.43MHz		6	20	ns
YOUT3 Group delay deviation 3	with filter	$\Delta t3_{GD\ YOUT3}$	to 6MHz		13	20	ns
YOUT3 Crosstalk		CT_{YOUT3}	SIN wave : 1V f=4.43MHz		−60	−55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
COUT3(63pin) electrical characteristics							
COUT3 Voltage gain		Gv_{COUT3}	SIN wave : 1V f=100kHz	5.7	6.0	6.3	dB
COUT3 Frequency characteristic	with filter	$f1_{COUT3}$	SIN wave : 1V 6.75MHz/100kHz	−1.0	0.0	1.0	dB
		$f2_{COUT3}$	SIN wave : 1V 27MHz/100kHz		−33.0	−24.0	dB
COUT3 Input dynamic range		DR_{COUT3}	SIN wave : 100kHz THD=1.0%	1.3	1.4		V
COUT3 Group delay	with filter	$t_{GD\ COUT3}$	at 100kHz		55		ns
COUT3 Group delay deviation 1	with filter	$\Delta t1_{GD\ COUT3}$	to 3.58MHz		4	20	ns
COUT3 Group delay deviation 2	with filter	$\Delta t2_{GD\ COUT3}$	to 4.43MHz		6	20	ns
COUT3 Group delay deviation 3	with filter	$\Delta t3_{GD\ COUT3}$	to 6MHz		13	20	ns
COUT3 Crosstalk		CT_{COUT3}	SIN wave : 1V f=4.43MHz		−60	−55	dB
CYOUT1(75pin) electrical characteristics							
CYOUT1 Voltage gain		Gv_{CYOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
CYOUT1 Frequency characteristic Peak		$fpeak_{CYOUT1}$	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB
CYOUT1 Frequency characteristic	without filter	$f1_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz	−3.0	−1.0	1.0	dB
	with filter1	$f11_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz	−3.0	−1.0	1.0	dB
		$f12_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 27MHz/100kHz		−55.0	−50.0	dB
	with filter2	$f21_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz	-3.0	-1.0	1.0	dB
		$f22_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 54MHz/100kHz		−55.0	−50.0	dB
	with filter3	$f31_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz	−3.0	−1.0	1.0	dB
		$f32_{CYOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		−35.0	−25.0	dB
CYOUT1 Input dynamic range		DR_{CYOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CYOUT1 (75pin) electrical characteristics							
CYOUT1 Group delay	with filter1	$t1_{GD\ CYOUT1}$	at 100kHz		80		ns
	with filter2	$t2_{GD\ CYOUT1}$	at 100kHz		45		ns
	with filter3	$t3_{GD\ CYOUT1}$	at 100kHz		25		ns
CYOUT1 Group delay deviation 11	with filter1	$\Delta t11_{GD\ CYOUT1}$	to 3.58MHz		4	20	ns
CYOUT1 Group delay deviation 12		$\Delta t12_{GD\ CYOUT1}$	to 4.43MHz		6	20	ns
CYOUT1 Group delay deviation 13		$\Delta t13_{GD\ CYOUT1}$	to 6MHz		15	30	ns
CYOUT1 Group delay deviation 21	with filter2	$\Delta t21_{GD\ CYOUT1}$	to 3.58MHz		4	20	ns
CYOUT1 Group delay deviation 22		$\Delta t22_{GD\ CYOUT1}$	to 4.43MHz		6	20	ns
CYOUT1 Group delay deviation 23		$\Delta t23_{GD\ CYOUT1}$	to 12MHz		15	30	ns
CYOUT1 Group delay deviation 31	with filter3	$\Delta t31_{GD\ CYOUT1}$	to 3.58MHz		1	20	ns
CYOUT1 Group delay deviation 32		$\Delta t32_{GD\ CYOUT1}$	to 4.43MHz		1	20	ns
CYOUT1 Group delay deviation 33		$\Delta t33_{GD\ CYOUT1}$	to 24MHz		5	20	ns
CYOUT1 Crosstalk		CT_{CYOUT1}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PbOUT1 (74pin) electrical characteristics							
PbOUT1 Voltage gain		Gv_{PbOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
PbOUT1 Frequency characteristic Peak		$fpeak_{PbOUT1}$	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB
PbOUT1 Frequency characteristic	without filter	$f1_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz	−3.0	−1.0	1.0	dB
	with filter1	$f11_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz	−3.0	−1.0	1.0	dB
		$f12_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 27MHz/100kHz		−55.0	−50.0	dB
	with filter2	$f21_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz	−3.0	−1.0	1.0	dB
		$f22_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 54MHz/100kHz		−55.0	−50.0	dB
	with filter3	$f31_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz	−3.0	−1.0	1.0	dB
		$f32_{PbOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		−35.0	−25.0	dB
PbOUT1 Input dynamic range		DR_{PbOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
PbOUT1 Group delay	with filter1	$t1_{GD\ PbOUT1}$	at 100kHz		80		ns
	with filter2	$t2_{GD\ PbOUT1}$	at 100kHz		45		ns
	with filter3	$t3_{GD\ PbOUT1}$	at 100kHz		25		ns
PbOUT1 Group delay deviation 11	with filter1	$\Delta t11_{GD\ PbOUT1}$	to 3.58MHz		4	20	ns
PbOUT1 Group delay deviation 12		$\Delta t12_{GD\ PbOUT1}$	to 4.43MHz		6	20	ns
PbOUT1 Group delay deviation 13		$\Delta t13_{GD\ PbOUT1}$	to 6MHz		15	30	ns

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PbOUT1 (74pin) electrical characteristics							
PbOUT1 Group delay deviation 21	with filter2	$\Delta t21_{GD\ PbOUT1}$	to 3.58MHz		4	20	ns
PbOUT1 Group delay deviation 22		$\Delta t22_{GD\ PbOUT1}$	to 4.43MHz		6	20	ns
PbOUT1 Group delay deviation 23		$\Delta t23_{GD\ PbOUT1}$	to 12MHz		15	30	ns
PbOUT1 Group delay deviation 31	with filter3	$\Delta t31_{GD\ PbOUT1}$	to 3.58MHz		1	20	ns
PbOUT1 Group delay deviation 32		$\Delta t32_{GD\ PbOUT1}$	to 4.43MHz		1	20	ns
PbOUT1 Group delay deviation 33		$\Delta t33_{GD\ PbOUT1}$	to 24MHz		5	20	ns
PbOUT1 Crosstalk		CT_{PbOUT1}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB
PrOUT1 (73pin) electrical characteristics							
PrOUT1 Voltage gain		Gv_{PrOUT1}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
PrOUT1 Frequency characteristic Peak		$fpeak_{PrOUT1}$	0.3V SYNC+0.7V SIN wave f=100kHz~100MHz	0.0	0.5	1.0	dB
PrOUT1 Frequency characteristic	without filter	$f1_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz	−3.0	−1.0	1.0	dB
	with filter1	$f11_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 6.75MHz/100kHz	−3.0	−1.0	1.0	dB
		$f12_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 27MHz/100kHz		−55.0	−50.0	dB
	with filter2	$f21_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 13.5MHz/100kHz	−3.0	−1.0	1.0	dB
		$f22_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 54MHz/100kHz		−55.0	−50.0	dB
	with filter3	$f31_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 37.5MHz/100kHz	−3.0	−1.0	1.0	dB
		$f32_{PrOUT1}$	0.3V SYNC+0.7V SIN wave 100MHz/100kHz		−35.0	−25.0	dB
PrOUT1 Input dynamic range		DR_{PrOUT1}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
PrOUT1 (73pin) electrical characteristics							
PrOUT1 Group delay	with filter1	$t1_{GD\ PrOUT1}$	at 100kHz		80		ns
	with filter2	$t2_{GD\ PrOUT1}$	at 100kHz		45		ns
	with filter3	$t3_{GD\ PrOUT1}$	at 100kHz		25		ns
PrOUT1 Group delay deviation 11	with filter1	$\Delta t11_{GD\ PrOUT1}$	to 3.58MHz		4	20	ns
PrOUT1 Group delay deviation 12		$\Delta t12_{GD\ PrOUT1}$	to 4.43MHz		6	20	ns
PrOUT1 Group delay deviation 13		$\Delta t13_{GD\ PrOUT1}$	to 6MHz		15	30	ns
PrOUT1 Group delay deviation 21	with filter2	$\Delta t21_{GD\ PrOUT1}$	to 3.58MHz		4	20	ns
PrOUT1 Group delay deviation 22		$\Delta t22_{GD\ PrOUT1}$	to 4.43MHz		6	20	ns
PrOUT1 Group delay deviation 23		$\Delta t23_{GD\ PrOUT1}$	to 12MHz		15	30	ns
PrOUT1 Group delay deviation 31	with filter3	$\Delta t31_{GD\ PrOUT1}$	to 3.58MHz		1	20	ns
PrOUT1 Group delay deviation 32		$\Delta t32_{GD\ PrOUT1}$	to 4.43MHz		1	20	ns
PrOUT1 Group delay deviation 33		$\Delta t33_{GD\ PrOUT1}$	to 30MHz		12	20	ns
PrOUT1 Crosstalk		CT_{PrOUT1}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CYOUT2 (71pin) electrical characteristics						
CYOUT2 Voltage gain	Gv_{CYOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
CYOUT2 Frequency characteristic Peak	$fpeak_{CYOUT2}$	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
CYOUT2 Frequency characteristic	$f1_{CYOUT2}$	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	−3.0	−1.0	0.0	dB
CYOUT2 Input dynamic range	DR_{CYOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
CYOUT2 Crosstalk	CT_{CYOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB
PbOUT2 (70pin) electrical characteristics						
PbOUT2 Voltage gain	Gv_{PbOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
PbOUT2 Frequency characteristic Peak	$fpeak_{PbOUT2}$	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
PbOUT2 Frequency characteristic	$f1_{PbOUT2}$	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	−3.0	−1.0	0.0	dB
PbOUT2 Input dynamic range	DR_{PbOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
PbOUT2 Crosstalk	CT_{PbOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB
PrOUT2 (69pin) electrical characteristics						
PrOUT2 Voltage gain	Gv_{PrOUT2}	0.3V SYNC+0.7V SIN wave f=100kHz	−0.3	0.0	0.3	dB
PrOUT2 Frequency characteristic Peak	$fpeak_{PrOUT2}$	0.3V SYNC+0.7V SIN wave f=100kHz~50MHz	0.0	0.5	1.0	dB
PrOUT2 Frequency characteristic	$f1_{PrOUT2}$	0.3V SYNC+0.7V SIN wave 50MHz/100kHz	−3.0	−1.0	0.0	dB
PrOUT2 Input dynamic range	DR_{PrOUT2}	SIN wave : 100kHz THD=1.0%	1.6	2.0		V
PrOUT2 Crosstalk	CT_{PrOUT2}	0.3V SYNC+0.7V SIN wave f=4.43MHz		−60	−55	dB
Group delay deviation between each channels (OUT1~OUT3)						
Group delay deviation between C and Y	$\Delta t1_{chGD}$	between C and Y at 3.58MHz		0	10	ns
Group delay deviation between CY and Pb (Pr)	$\Delta t2_{chGD}$	between CY and Pb (Pr) at 8MHz		0	10	ns

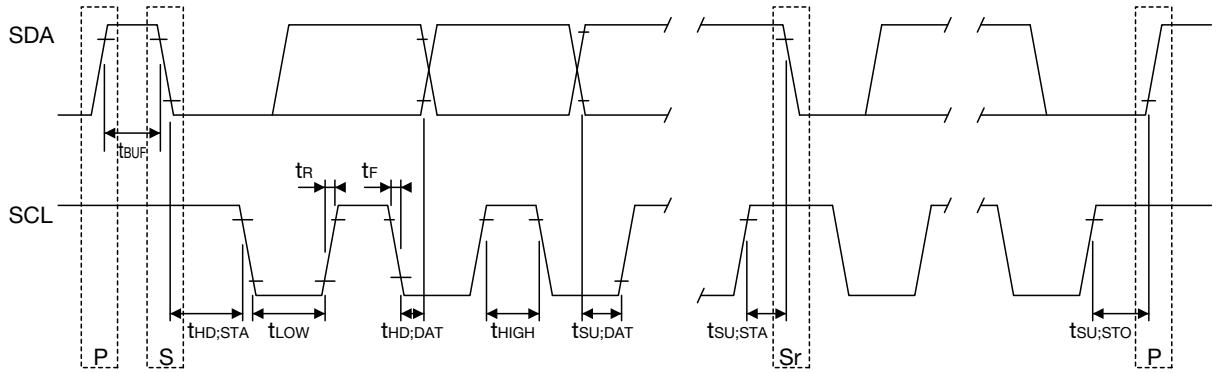
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
L,ROUT (34~39pin) electrical characteristics							
L,ROUT Voltage gain	0dB	Gv1L, ROUT	SIN wave : 1Vrms f=1kHz	−0.3	0.0	0.3	dB
	6dB	Gv2 L, ROUT	SIN wave : 1Vrms f=1kHz	5.7	6.0	6.3	dB
L,ROUT Frequency characteristic	0dB	f1L, ROUT	SIN wave : 1Vrms f=50kHz	−3.0			dB
	6dB	f2L, ROUT	SIN wave : 1Vrms f=50kHz	−3.0			dB
Total harmonic distortion		THD	SIN wave : 1Vrms f=1kHz, Gv=0dB		0.03	0.05	%
Input dynamic range		DR	f=1kHz, THD=0.5% Gv=0dB	2.8	3.0		Vrms
Crosstalk		CT	SIN wave 1Vrms f=1kHz		−90	−80	dB
Ripple rejection		PSRR	Vcc = 9V+0.1Vrms (SIN wave) at 100Hz		−50	−40	dB
Output offset voltage		VOFF1	DC offset at the switching time, Gv=0dB	−15	0	15	mV
		VOFF2	DC offset at the switching time, Gv=6dB	−30	0	30	
S/N ratio		S/N1	1kHz, A curve, 1Vrms Gv=0dB		−90	−80	dB
		S/N2	1kHz, A curve, 1Vrms Gv=6dB		−80	−70	dB

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
O1 (5pin) electrical characteristics							
O1 pin low level output voltage		V_{O1}	O1 pin sink 5mA	GND		0.4	V
O1 pin Leak current (at the time of OFF)		I_{O1}	O1=5.0V	-10		10	µA
O2 (17pin) electrical characteristics							
O2 pin low level output voltage		V_{O2}	O2 pin sink 5mA	GND		0.4	V
O2 pin Leak current (at the time of OFF)		I_{O2}	O2=5.0V	-10		10	µA
O3 (23pin) electrical characteristics							
O3 pin low level output voltage		V_{O3}	O3 pin sink 5mA	GND		0.4	V
O3 pin Leak current (at the time of OFF)		I_{O3}	O3=5.0V	-10		10	µA
FLAG (29pin) electrical characteristics							
FLAG pin low level output voltage		V_{FLAG}	FLAG pin sink 5mA	GND		0.4	V
FLAG pin Leak current (at the time of OFF)		I_{FLAG}	FLAG=5.0V	-10		10	µA
DL1 (81,87,93pin) electrical characteristics							
DL1Input Voltage1	Low	$V1_{L\ DL1}$		GND		1.0	V
	Middle	$V1_{M\ DL1}$		1.3		2.7	V
	High	$V1_{H\ DL1}$		3.5		$V_{CC}5$	V
DL2 (83,89,95pin) electrical characteristics							
DL2 Input Voltage	Low	$V_{L\ DL2}$		GND		2.7	V
	High	$V_{H\ DL2}$		3.5		$V_{CC}5$	V
DL3 (85,91,97pin) electrical characteristics							
DL3 Input Voltage	Low	$V_{L\ DL3}$		GND		1.0	V
	Middle	$V_{M\ DL3}$		1.3		2.7	V
	High	$V_{H\ DL3}$		3.5		$V_{CC}5$	V

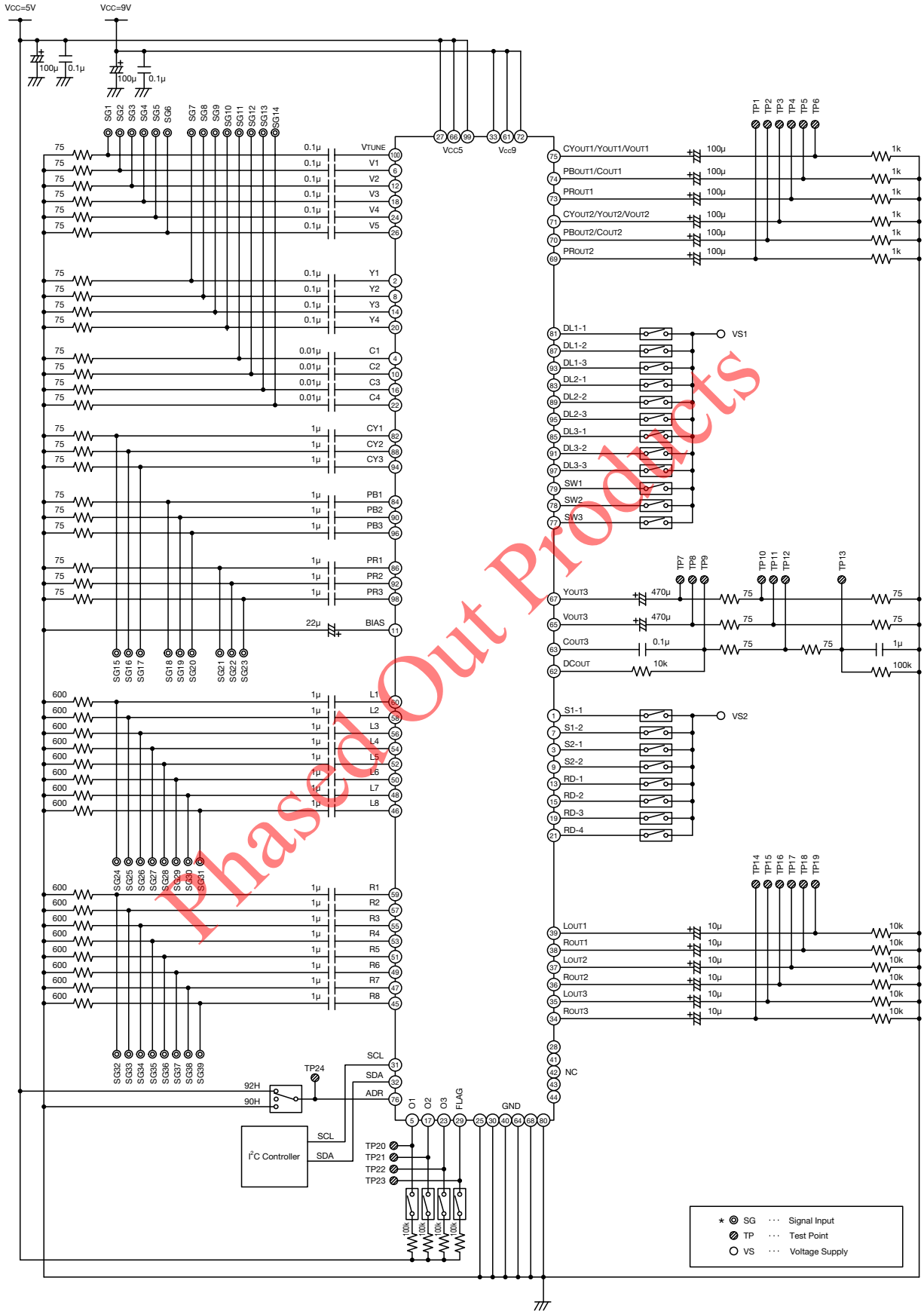
Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Units
SW (79,78,77pin) electrical characteristics							
SW Input Voltage	Low	$V_{L\,SW}$		GND		2.0	V
	High	$V_{H\,SW}$		3.0		Vcc5	V
SW output current at terminal voltage "Low"		I_{SW}	SW=GND	19	27	35	µA
S2 (3,9pin) electrical characteristics							
S2 Input Voltage1	Low	$V1_{L\,S2/FS}$	S, D-Detect Mode	GND		1.0	V
	Middle	$V1_{M\,S2/FS}$		1.3		2.7	V
	High	$V1_{H\,S2/FS}$		3.5		Vcc5	V
S1 (1,7rpin) electrical characteristics							
S1 Input Voltage	Low	$V_{L\,S1}$		GND		2.0	V
	High	$V_{H\,S1}$		3.0		Vcc5	V
S1 output current at terminal voltage "Low"		I_{S1}	S1=GND	19	27	35	µA
ADR (76pin) electrical characteristics							
ADR Input Voltage	Low	$V_{L\,ADR}$	90H select	GND		0.8	V
	High	$V_{H\,ADR}$	92H select	2.5		Vcc5	V
ADR input current at terminal voltage "High"		I_{ADR}	ADR=5.0V	50	70	90	µA
RD (13,15,19,21pin) electrical characteristics							
RD Input Voltage	Low	$V_{L\,RD}$		GND		2.0	V
	High	$V_{H\,RD}$		3.0		Vcc5	V
RD output current at terminal voltage "Low"		I_{RD}	RD=GND	19	27	35	µA

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C condition (note3)						
Input voltage L	V_{IL}		GND		0.8	V
Input voltage H	V_{IH}		2.2		$V_{CC}5$	V
SDA low level output voltage	V_{OL}	SDA sink 3mA	GND		0.4	V
High level input current	I_{IH}	SDA, SCL=4.5V	–10		10	µA
Low level input current	I_{IL}	SDA, SCL=0.4V	–10		10	µA
Clock frequency	f_{SCL}				400	kHz
Data transfer wait time	t_{BUF}		1.3			µs
SCL start hold time	$t_{HD;STA}$		0.6			µs
SCL low level hold time	t_{LOW}		1.3			µs
SCL high level hold time	t_{HIGH}		0.6			µs
Start condition setup time	$t_{SU;STA}$		0.6			µs
SDA data hold time	$t_{HD;DAT}$		0			µs
SDA data setup time	$t_{SU;DAT}$		100			ns
SDA,SCL rise time	t_R				300	ns
SDA,SCL fall time	t_F				300	ns
Stop condition setup time	$t_{SU;STO}$		0.6			µs

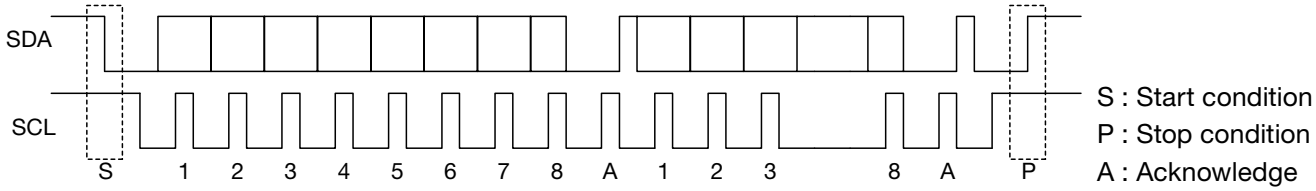
Note 3 : I²C condition



Measuring Circuit

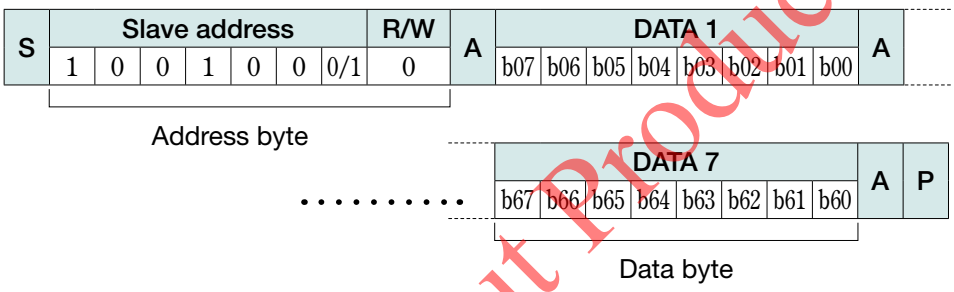


I²C BUS



I²C BUS is is inter bus system controled by 2 lines (SDA,SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the Start conditions.

[Control registers]
Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address,while the residual 1bit is assigned to the R/W bit.
Set the R/W bit to 0 when data are used control registers.
As MM1793 slave address, either 90H or 92H can be selected according to the ADR terminal conditions.
When ADR terminal is L,90H is selected.
The following figure indicates the control contents of control registers and switches.
Each bit of control registers is reset to 0,when power-on.

MM1793 consists of one address byte and 7 control data bytes (8bytes in total).
All data over the limited length (9th and subsequent bytes) are fully neglected.
For details of the control contents of switches, refer to the another table.

Even if a 9V power supply and 5V power supply are independently blacked out as a power sequence,
I²C control is properly performed after power is recovered.

Table of control registers

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	OUT1 LPF select		OUT1 Power Save		OUT1 LINE SELECT			
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
			OUT2 Power Save		OUT2 LINE SELECT			
DATA3 [00H]	b27	b26	b25	b24	b23	b22	b21	b20
	DCout Voltage		OUT3 Power Save		OUT3 LINE SELECT			
DATA4 [00H]	b37	b36	b35	b34	b33	b32	b31	b30
	Audio OUT1 LINE SELECT				Audio OUT2 LINE SELECT			
DATA5 [00H]	b47	b46	b45	b44	b43	b42	b41	b40
		AO1 GAIN SW	AO2 GAIN SW	AO3 GAIN SW	Audio OUT3 LINE SELECT			
DATA6 [00H]	b57	b56	b55	b54	b53	b52	b51	b50
		AO1 Power Save	AO2 Power Save	AO3 Power Save	O1	O2	O3	
DATA7 [00H]	b67	b66	b65	b64	b63	b62	b61	b60
	VCA GAIN SELECT							

* [00H] is in the initial state of control registers.

Details of the contents of control (1)

OUT1 LINE SELECT

b03	b02	b01	b00	CYout1 (75pin)	PBout1 (74pin)	PRout1 (73pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V_{TUNE}	Mute	Mute
0	0	1	0	V1	Mute	Mute
0	0	1	1	V2	Mute	Mute
0	1	0	0	V3	Mute	Mute
0	1	0	1	V4	Mute	Mute
0	1	1	0	V5	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

OUT2 LINE SELECT

b13	b12	b11	b10	CYout2 (71pin)	PBout2 (70pin)	PRout2 (69pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V_{TUNE}	Mute	Mute
0	0	1	0	V1	Mute	Mute
0	0	1	1	V2	Mute	Mute
0	1	0	0	V3	Mute	Mute
0	1	0	1	V4	Mute	Mute
0	1	1	0	V5	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

Details of the contents of control (2)

OUT3 LINE SELECT (*1)

b23	b22	b21	b20	Vout3 (65pin)	Yout3 (67pin)	Cout3 (63pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	Y1+C1	Y1	C1
0	0	1	0	Y2+C2	Y2	C2
0	0	1	1	Y3+C3	Y3	C3
0	1	0	0	Y4+C4	Y4	C4
0	1	0	1	Mute	Mute	Mute
0	1	1	0	Mute	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Mute	Mute	Mute
1	0	0	1	VTUNE	Mute	Mute
1	0	1	0	V1	Mute	Mute
1	0	1	1	V2	Mute	Mute
1	1	0	0	V3	Mute	Mute
1	1	0	1	V4	Mute	Mute
1	1	1	0	V5	Mute	Mute
1	1	1	1	Mute	Mute	Mute

(*1) When DCout is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

LPF Cutoff Frequency Select OUT1 (73,74,75pin)

b07	b06	LPF fc
0	0	through
0	1	37.5MHz
1	0	13.5MHz
1	1	6.75MHz

Powersave

OUT1 (73,74,75pin)

b05	Conditions
0	Active
1	PowerSave

OUT2 (69,70,71pin)

b15	Conditions
0	Active
1	PowerSave

OUT3 (63,65,67pin)

b25	Conditions
0	Active
1	PowerSave

OUTPUT PORT Control

O1 (5pin)

b53	Conditions
0	Low
1	Open

O2 (17pin)

b52	Conditions
0	Low
1	Open

O3 (23pin)

b51	Conditions
0	Low
1	Open

DCout (62pin) OUTPUT VOLTAGE

b27	b26	VOLTAGE
0	0	0V
0	1	2.2V
1	0	5V
1	1	Hi-Impedance (*2)

(*2) When DCout is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

Details of the contents of control (3)

VCA GAIN SELECT

b67	b66	b65	b64	b63	b62	b61	b60	Hex	Dec	Gv(*3) [V]	Gv[dB]
0	0	0	0	0	0	0	0	00	00	0.500	−6.02
0	0	0	0	0	0	0	1	01	01	0.505	−5.94
0	0	0	0	0	0	1	0	02	02	0.510	−5.85
0	0	0	0	0	0	1	1	03	03	0.515	−5.77
0	0	0	0	0	1	0	0	04	04	0.520	−5.69
0	0	0	0	0	1	0	1	05	05	0.525	−5.60
0	0	0	0	0	1	1	0	06	06	0.529	−5.52
0	0	0	0	0	1	1	1	07	07	0.534	−5.44
0	0	0	0	1	0	0	0	08	08	0.539	−5.36
0	0	0	0	1	0	0	1	09	09	0.544	−5.29
0	0	0	0	1	0	1	0	0A	10	0.549	−5.21
0	0	0	0	1	0	1	1	0B	11	0.554	−5.13
0	0	0	0	1	1	0	0	0C	12	0.559	−5.05
0	0	0	0	1	1	0	1	0D	13	0.564	−4.98
0	0	0	0	1	1	1	0	0E	14	0.569	−4.90
0	0	0	0	1	1	1	1	0F	15	0.574	−4.83
0	1	0	1	1	1	1	0	5E	94	0.961	−0.35
0	1	0	1	1	1	1	1	5F	95	0.966	−0.30
0	1	1	0	0	0	0	0	60	96	0.971	−0.26
0	1	1	0	0	0	0	1	61	97	0.975	−0.22
0	1	1	0	0	0	1	0	62	98	0.980	−0.17
0	1	1	0	0	0	1	1	63	99	0.985	−0.13
0	1	1	0	0	1	0	0	64	100	0.990	−0.09
0	1	1	0	0	1	0	1	65	101	0.995	−0.04
0	1	1	0	0	1	1	0	66	102	1.000	0.00
0	1	1	0	0	1	1	1	67	103	1.005	0.04
0	1	1	0	1	0	0	0	68	104	1.010	0.08
0	1	1	0	1	0	0	1	69	105	1.015	0.13
0	1	1	0	1	0	1	0	6A	106	1.020	0.17
0	1	1	0	1	0	1	1	6B	107	1.025	0.21
0	1	1	0	1	1	0	0	6C	108	1.029	0.25
0	1	1	0	1	1	0	1	6D	109	1.034	0.29
1	1	1	1	0	0	0	0	F0	240	1.676	4.49
1	1	1	1	0	0	0	1	F1	241	1.681	4.51
1	1	1	1	0	0	1	0	F2	242	1.686	4.54
1	1	1	1	0	0	1	1	F3	243	1.691	4.56
1	1	1	1	0	1	0	0	F4	244	1.696	4.59
1	1	1	1	0	1	0	1	F5	245	1.701	4.61
1	1	1	1	0	1	1	0	F6	246	1.706	4.64
1	1	1	1	0	1	1	1	F7	247	1.711	4.66
1	1	1	1	1	0	0	0	F8	248	1.716	4.69
1	1	1	1	1	0	0	1	F9	249	1.721	4.71
1	1	1	1	1	0	1	0	FA	250	1.725	4.74
1	1	1	1	1	0	1	1	FB	251	1.730	4.76
1	1	1	1	1	1	0	0	FC	252	1.735	4.79
1	1	1	1	1	1	0	1	FD	253	1.740	4.81
1	1	1	1	1	1	1	0	FE	254	1.745	4.84
1	1	1	1	1	1	1	1	FF	255	1.750	4.86

(*3) Gv=Vout(VTUNE=Vin1+1V)-Vout(VTUNE=Vin1)at 71,75 pin
Gv=0.50+(1.25/255)* 'Dec'
Above Gv is a design theoretical value.

Details of the contents of control (4)

Audio OUT1 LINE SELECT

b37	b36	b35	b34	Lout1 (39pin)	Rout1 (38pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT2 LINE SELECT

b33	b32	b31	b30	Lout2 (37pin)	Rout2 (36pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT3 LINE SELECT

b43	b42	b41	b40	Lout3 (35pin)	Rout3 (34pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	Mute	Mute
1	0	1	0	Mute	Mute
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Details of the contents of control (5)

Audio GAIN SW

OUT1 (38,39pin)

b46	GAIN
0	0dB
1	6dB

OUT2 (36,37pin)

b45	GAIN
0	0dB
1	6dB

OUT3 (34,35pin)

b44	GAIN
0	0dB
1	6dB

Audio Powersave

OUT1 (38,39pin)

b56	Conditions
0	Active
1	PowerSave

OUT2 (36,37pin)

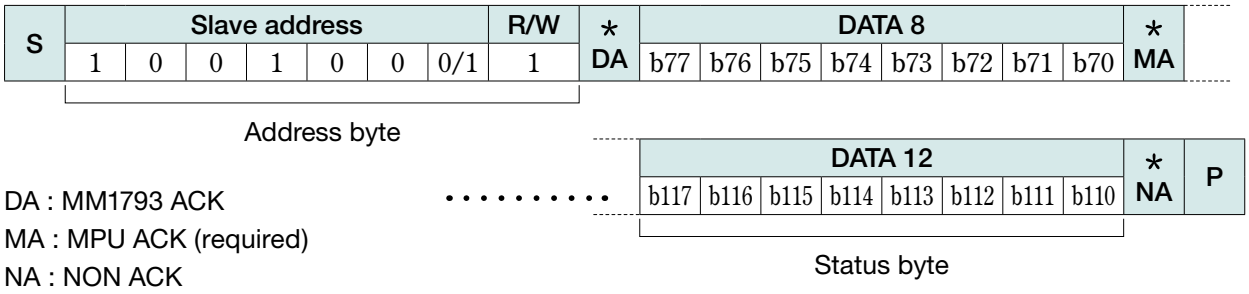
b55	Conditions
0	Active
1	PowerSave

OUT3 (34,35pin)

b54	Conditions
0	Active
1	PowerSave

Status registers

Status registers are data to inform the master of the device status.
The data format is set as shown in the following figure.



DA : MM1793 ACK
MA : MPU ACK (required)
NA : NON ACK

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers.
As MM1793 slave address, either 91H or 93H can be selected according to the ADR terminal conditions.
When ADR terminal is L, 91H is selected.
Set the confirmation acknowledgement after the end of status register to non-ACK.
The following figure shows the correspondence of the output data of status registers.

Table of status registers (*2)

No.	DATA condition							
DATA8	b77	b76	b75	b74	b73	b72	b71	b70
			SW1 DETECT	DL1-1 DETECT		DL2-1 DETECT	DL3-1 DETECT	
DATA9	b87	b86	b85	b84	b83	b82	b81	b80
			SW2 DETECT	DL1-2 DETECT		DL2-2 DETECT	DL3-2 DETECT	
DATA10	b97	b96	b95	b94	b93	b92	b91	b90
			SW3 DETECT	DL1-3 DETECT		DL2-3 DETECT	DL3-3 DETECT	
DATA11	b107	b106	b105	b104	b103	b102	b101	b100
			S1-1 DETECT	S2-1 DETECT		S1-2 DETECT	S2-2 DETECT	
DATA12	b117	b116	b115	b114	b113	b112	b111	b110
			RD-1 DETECT		RD-2 DETECT	RD-3 DETECT		RD-4 DETECT

(*2) Control registers (DATA1 to DATA7) are not affected when reading status resisters (DATA8 to DATA12).

Output data of status registers & threshold (1)

It is based on CPR1202 which is the specification of JEITA.
(Except where noted otherwise, Ta=25°C, Vcc9=9V, Vcc5=5V)

S1-1~S1-2 (1,7,pin) DETECT

S1-1~S1-2 voltage	Conditions	S1-2	S1-1
		b102	b105
GND≦VDC≦2.0V	CONNECTED	1	1
3.0V≦VDC≦Vcc5	UNCONNECTED	0	0

S2-1~S2-2 (3,9pin) DETECT (Aspect)

S2-1~S2-2 voltage	Aspect	S2-2		S2-1	
		b101	b100	b104	b103
GND≦VDC≦1.0V	4 : 3	0	0	0	0
1.3V≦VDC≦2.7V	Letterbox	0	1	0	1
3.5V≦VDC≦Vcc5	16 : 9	1	0	1	0

DL1-1,DL1-2,DL1-3 (81,87,93pin) DETECT (Scanning Line)

DL1-1~DL1-3 voltage	Scanning Line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
GND≦VDC≦1.0V	480	0	0	0	0	0	0
1.3V≦VDC≦2.7V	720	0	1	0	1	0	1
3.5V≦VDC≦Vcc5	1080	1	0	1	0	1	0

DL2-1,DL2-2,DL2-3 (83,89,95pin) DETECT (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
GND≦VDC≦2.7V	Interlace	0	0	0
3.5V≦VDC≦Vcc5	Progressive	1	1	1

DL3-1,DL3-2,DL3-3 (85,91,97pin) DETECT (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
GND≦VDC≦1.0V	4 : 3	0	0	0	0	0	0
1.3V≦VDC≦2.7V	Letterbox	0	1	0	1	0	1
3.5V≦VDC≦Vcc5	16 : 9	1	0	1	0	1	0

SW1~SW3 (79,78,77pin) DETECT

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
GND≦VDC≦2.0V	CONNECTED	1	1	1
3.0V≦VDC≦Vcc5	UNCONNECTED	0	0	0

RD-1~RD-4 (13,15,19,21pin) DETECT

RD1-1~RD1-4 voltage	Conditions	RD-4	RD-3	RD-2	RD-1
		b110	b112	b113	b115
GND≦VDC≦2.0V	UNCONNECTED	0	0	0	0
3.0V≦VDC≦Vcc5	CONNECTED	1	1	1	1

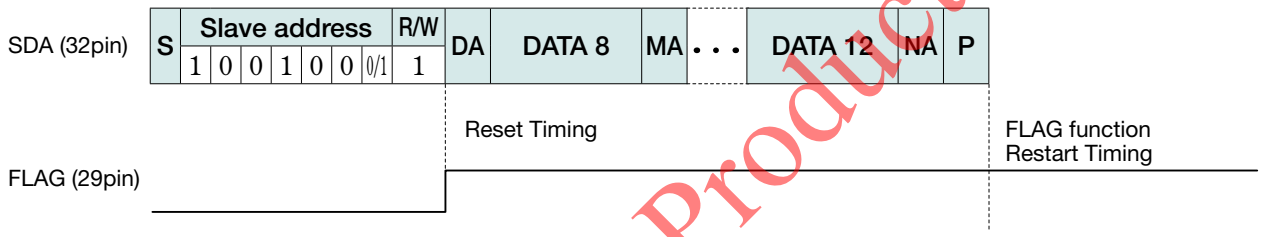
The output which monitor and detects a status register

MM1793 is Built-in the function which detects change of a status register and is outputted to a FLAG terminal.
When status register information changes, an output is changed from Open (High) to Low at FLAG terminal.
It is the open collector type output port.

Status register information	FLAG (29pin)
change	Low
readed	Open (High)

⁎ About Reset of a FLAG terminal (shift to a detection waiting state from a detection state)

When status register information is readed, an output is changed to Open at FLAG terminal.
(Reset) Reset timing from Low to Open (High) of a FLAG terminal is at the R/W bit detection time.

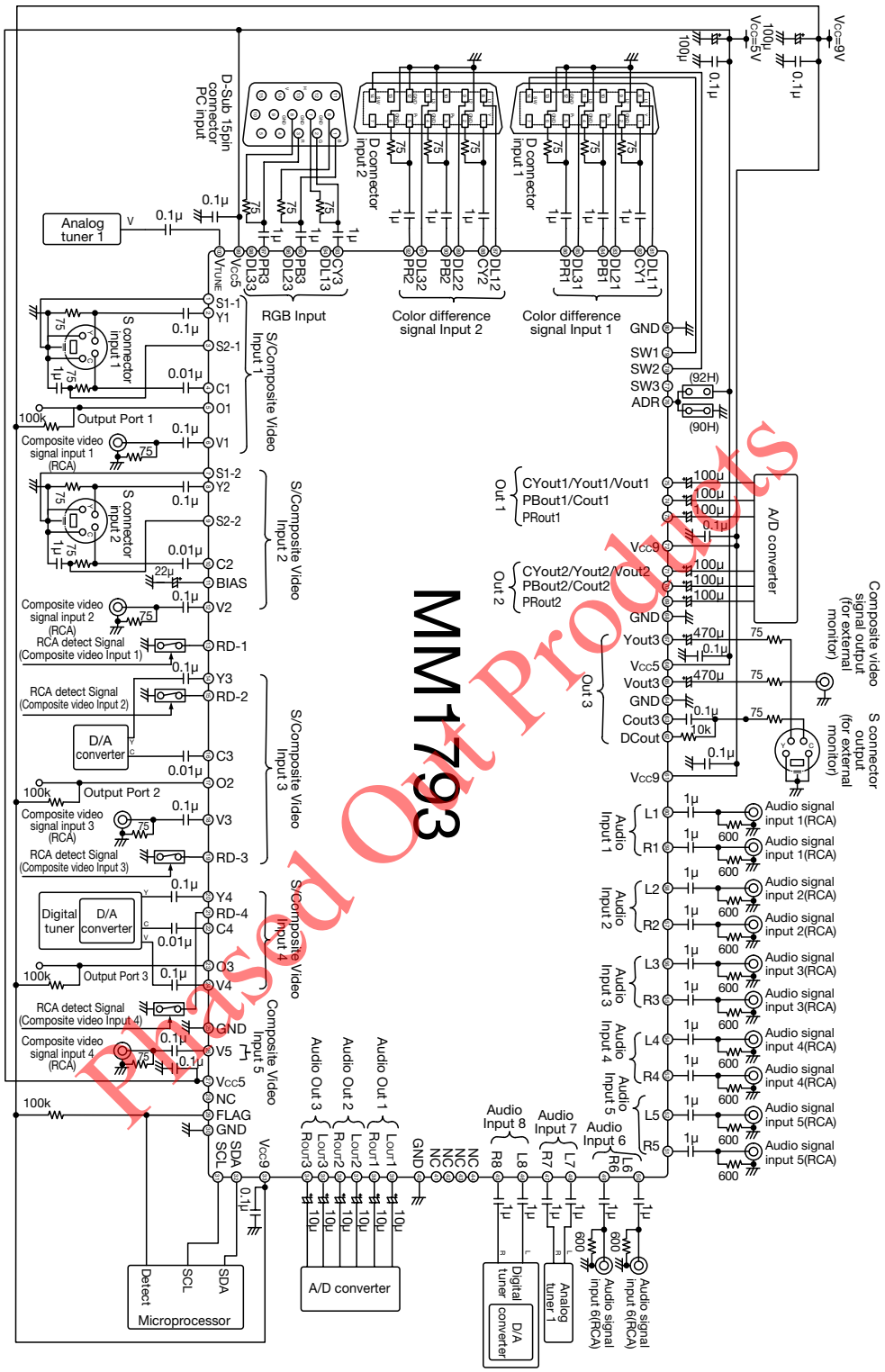


Note : FLAG terminal information does not become fixed by S/D distinction terminal may operate transitionally when power-on. Because, please carry out reading of a status register after a power-on and reset a FLAG terminal.

- Please do not use the interruption function of the master which used the trigger from Low to Open (High) of a FLAG terminal (29Pin).
  Because it is reading about a status register at the time of reset timing, the device status may be unable to be normally transmitted to a master

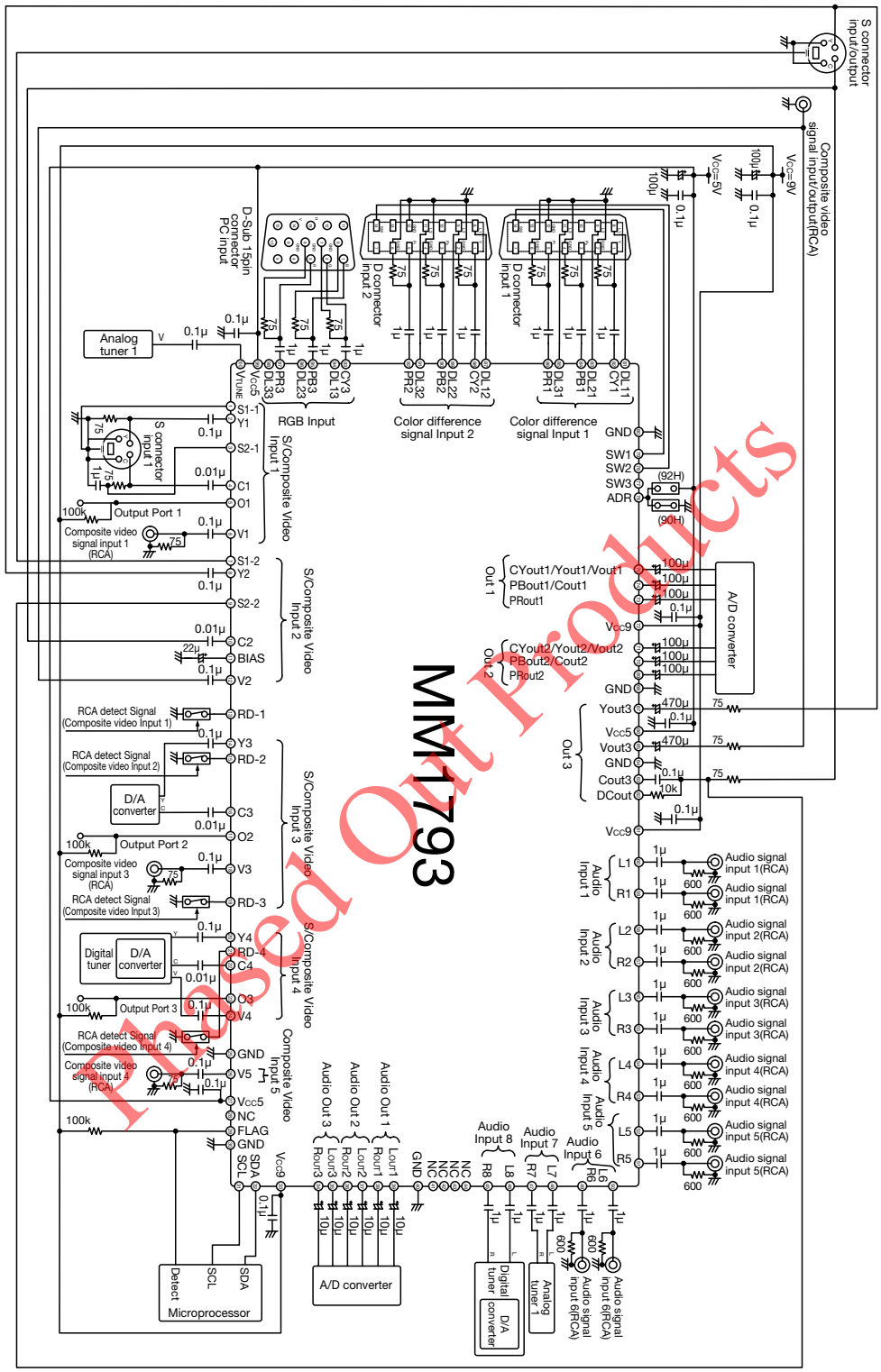
- FLAG functional restart timing is after Stop condition detection of I²C bus.
  For the reason, change of the status register between reset timing-Stop Condition is undetectable.
  At the time of status register reading which used the FLAG function, please read repeatedly by the master and check the adjustment of a status register.

Application Circuit 1



Note : Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.
We shall not be liable for any trouble or damage caused by using this circuit.
In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

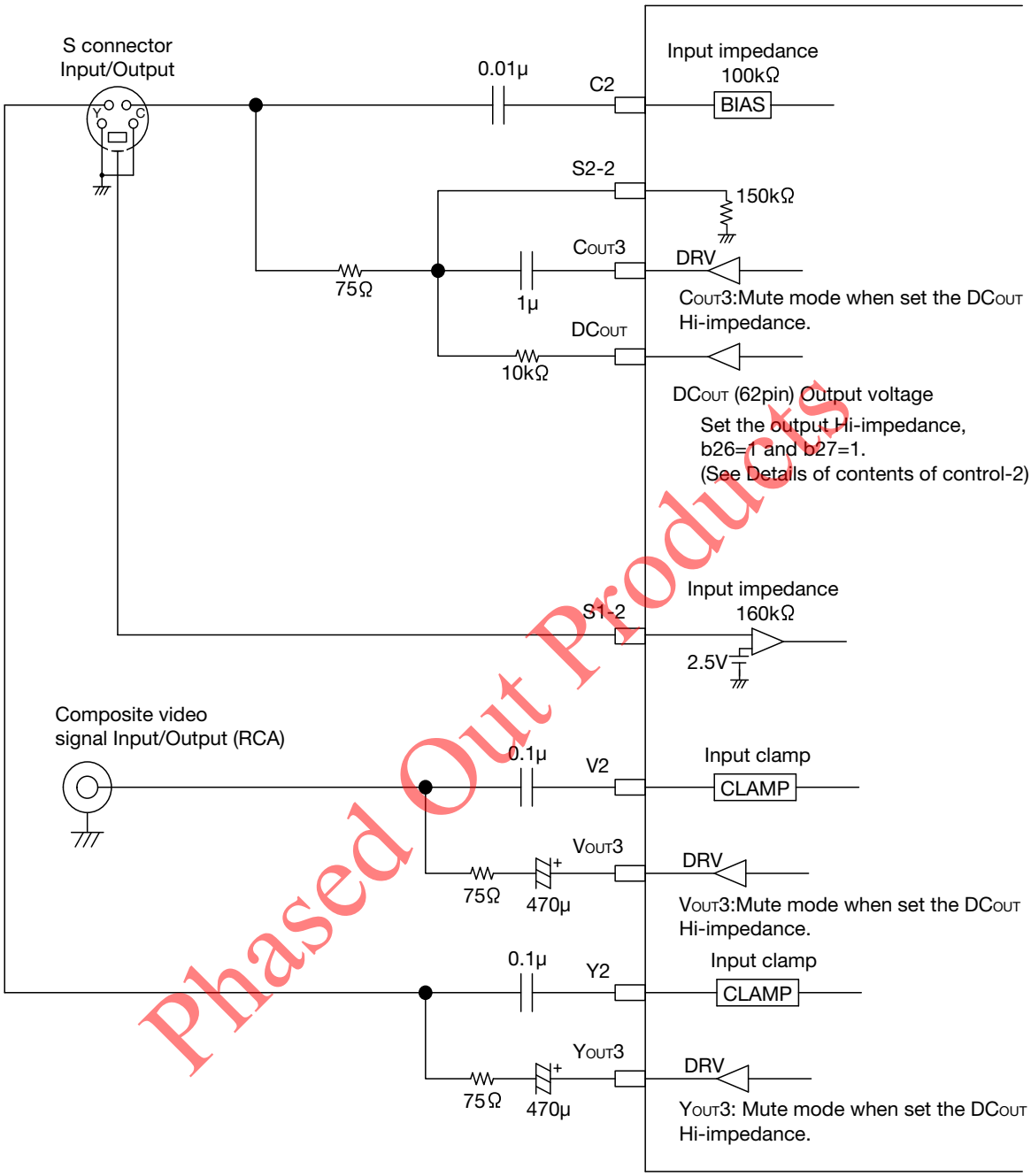
Application Circuit 2



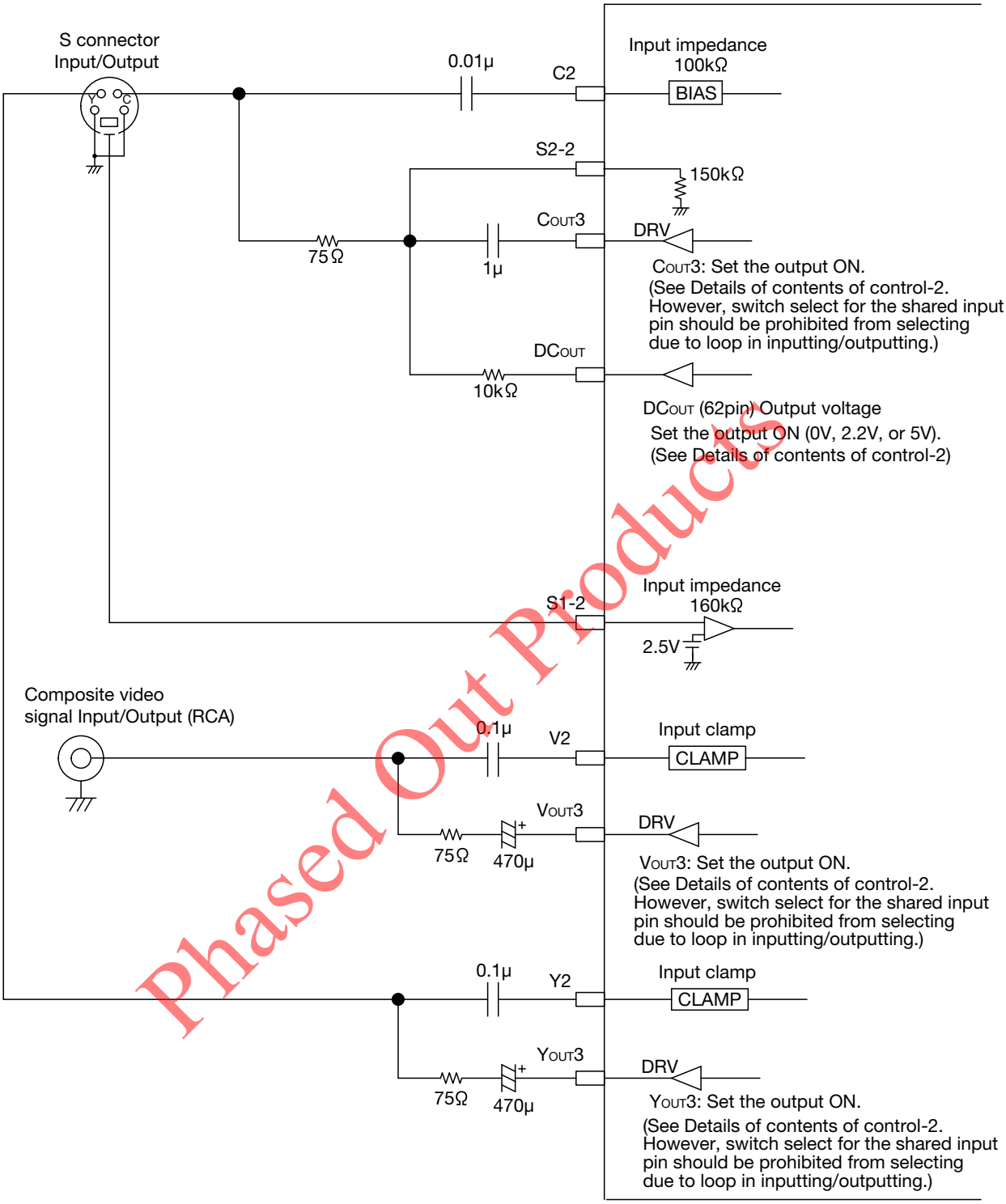
Note : Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.
We shall not be liable for any trouble or damage caused by using this circuit.
In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, we shall not be liable for any such problem, nor grant a license therefore.

Application circuit as an output or an input pin

(1) Settings when used as an input pin

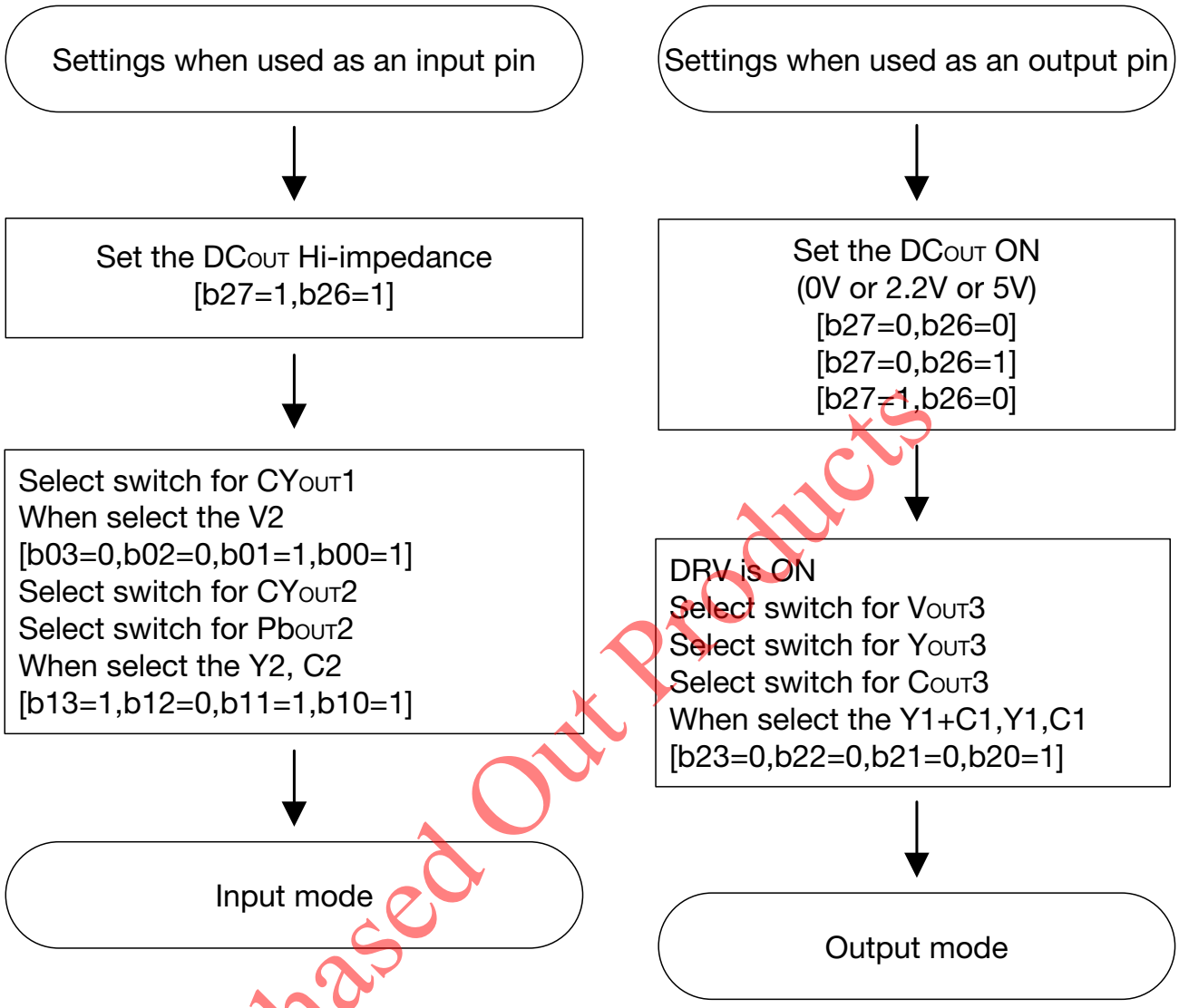


(2) Settings when used as an output pin



Applications as an output or an input pin

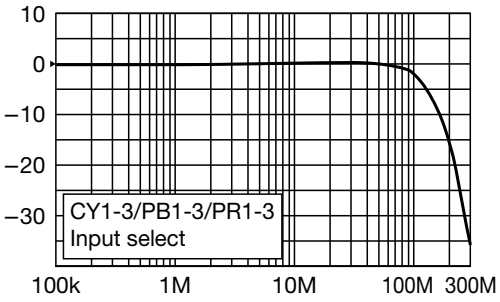
This is a flowchart applying to the Application Circuit2



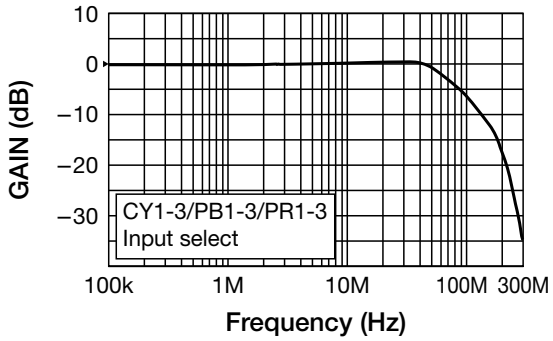
Characteristics (Except where noted otherwise, Ta=25°C, Vcc9=9V, Vcc5=5V, VCA GAIN SELECT='66H')

Frequency characteristic 1

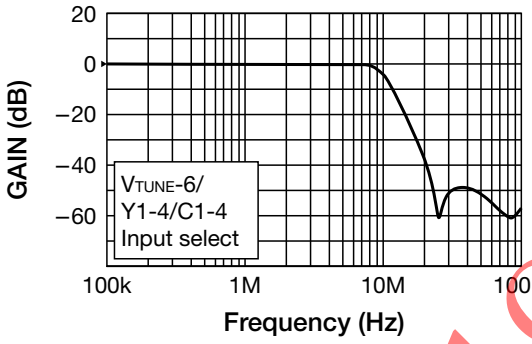
OUT1 THRU



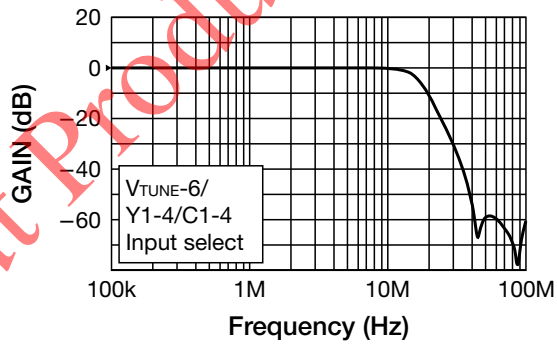
OUT2 THRU



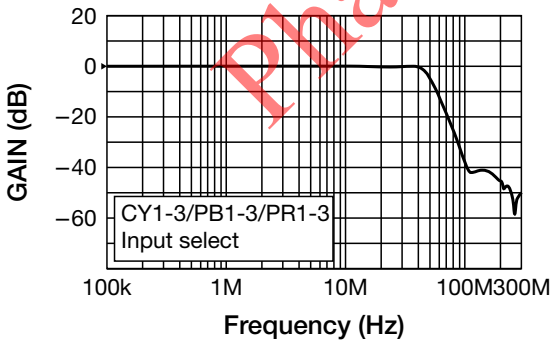
OUT1 LPF1(fc=6.75MHz)



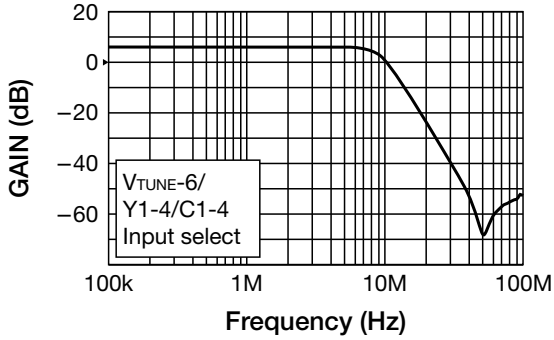
OUT1 LPF2 (fc=13.5MHz)



OUT1 LPF3 (fc=37.5MHz)

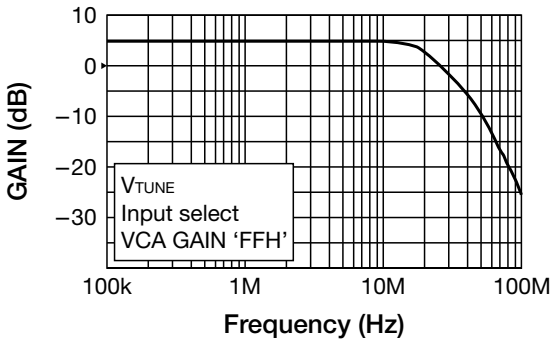


OUT3 (fc=6.75MHz)

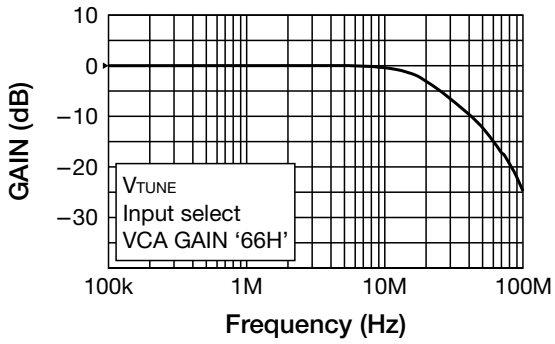


Frequency characteristic 2

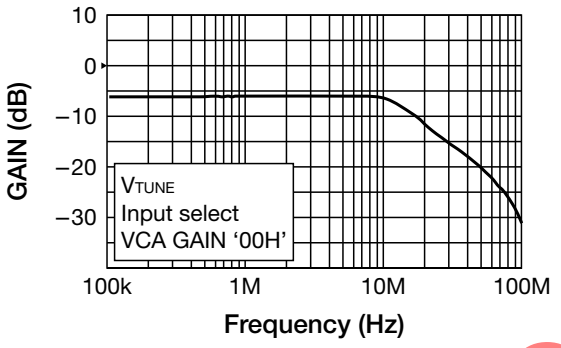
VTUNE—OUT1 THRU



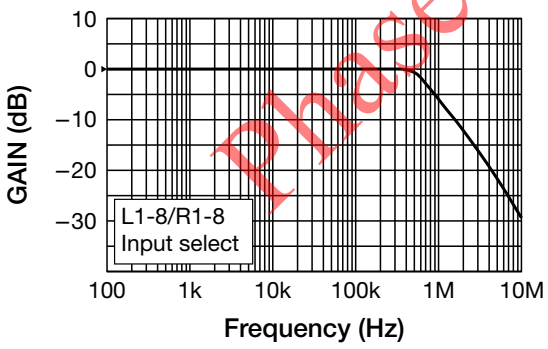
VTUNE—OUT1 THRU



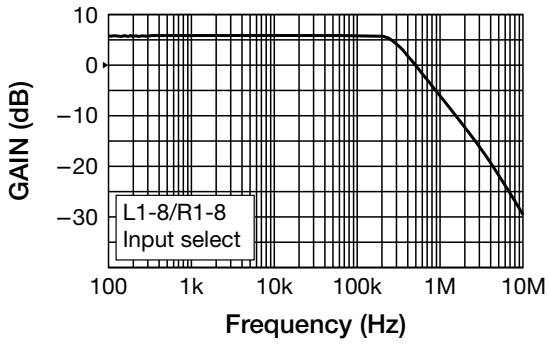
VTUNE—OUT1 THRU



AUDIO—OUT (0dB)

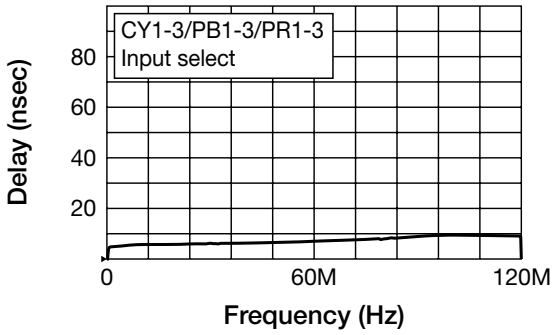


AUDIO—OUT (6dB)

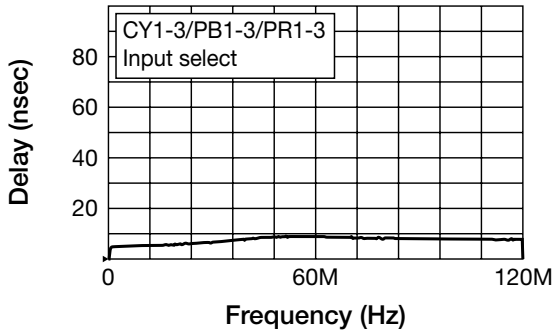


Group delay 1

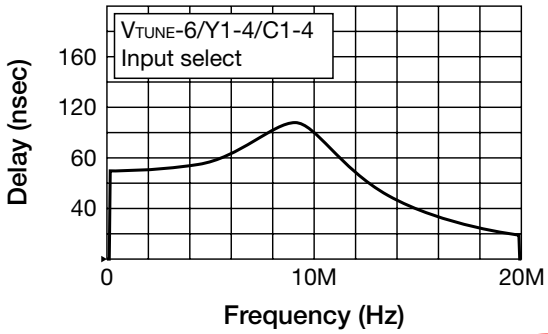
OUT1 THRU



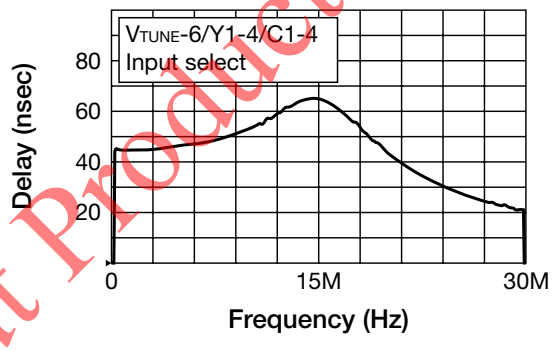
OUT2 THRU



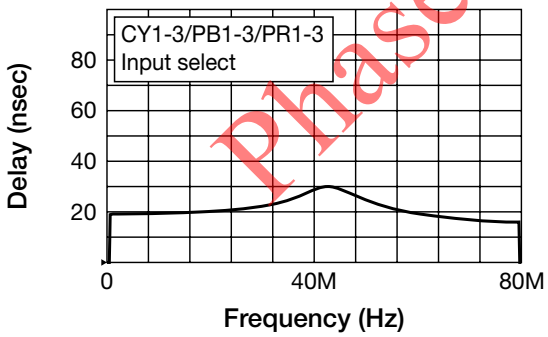
OUT1 LPF1 (fc=6.75MHz)



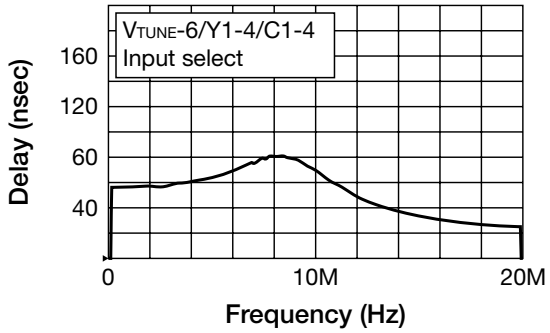
OUT1 LPF2 (fc=13.5MHz)



OUT1 LPF3 (fc=37.5MHz)

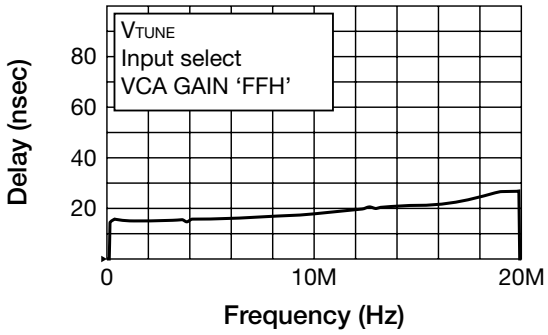


OUT3 (fc=6.75MHz)

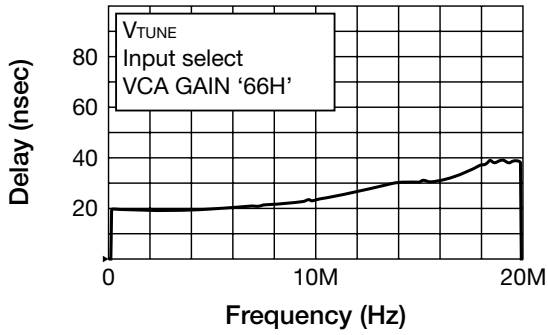


Group delay 2

VTUNE—OUT1 THRU



VTUNE—OUT1 THRU



VTUNE—OUT1 THRU