75Ω Driver IC for HD
Monolithic IC MM1797 Series

Outline

This IC is a video driver IC that realizes the frequency characteristics necessary for analog high definition signals. It deletes S video signals (Y/C) from the video signals to be output to maintain only the composite signals (CVBS) and the component signals (PY/Pb/Pr).
This feature helps its package to be miniaturized and the mounting area to be reduced. As a video output driver, this IC is best suited to a BD/DVD player.

Features

1. Built-in LPF whose passband is 30 MHz for 1080i or 720p/XGA HD video signals.
2. Rank A : Use of a new SAG correction circuit (patent pending) and reduction in the output coupling capacitance.
   Rank C : Use of a positive power supply and a negative power supply to eliminate the output coupling capacitance.
   Rank D/E : Use of a simple output circuit without “C” and elimination of output coupling capacitance.
3. Any additional electrostatic protection circuit is not required since the video output terminal has passed the ESD aerial discharge test (conforming to IEC610000-4-2).

		A-rank	C-rank	D-rank	E-rank
Input Signal		CVBS, Y, Pb, Pr (4ch)			
Output Signal		CVBS, Y, Pb, Pr (4ch)			
Supply Voltage		+5V single	+3.3V, −5V dual	+3V or +3.3V single	
Output Circuit		New sag correction circuit 220µF, 2.2µF	Out capacitor – less		
SD/HD LPF Select		○ H, M, L	○ H, L	× LPF HD Hold	
Mute		All channel		PY, Pb, Pr	
LPF	CVBS (High : pass BW, Low : stop BW)	6.75MHz 27MHz	6.75MHz 47.25MHz	6.75MHz 27MHz	
LPF	Y/Pb/Pr – SD (High : pass BW, Low : stop BW)	13.5MHz 54MHz			
LPF	Y/Pb/Pr – HD (High : pass BW, Low : stop BW)	30MHz 74MHz	30MHz 112MHz	27MHz 74MHz	30MHz 148MHz
Package		TSOP-16B (0.65mm pitch)			
Note				If the 75Ω termination on the TV side is AC termination, the signal may not be output.	

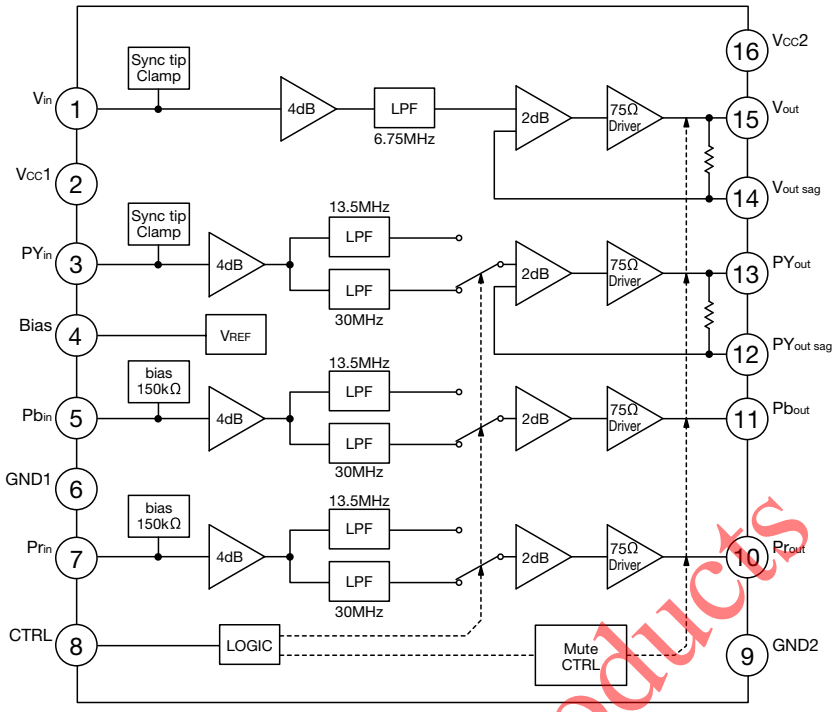
Packages

TSOP-16B

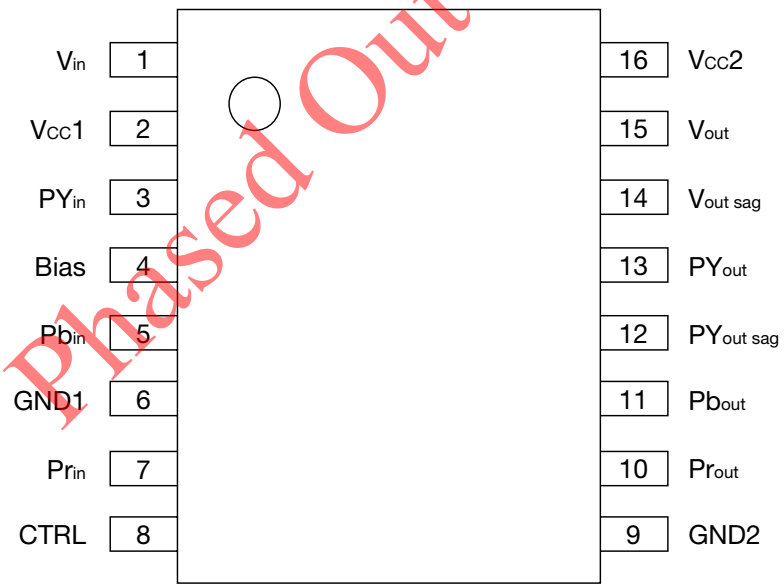
Applications

1. BD/DVD Players
2. Set Top Boxes

Block Diagram



Pin Assignment

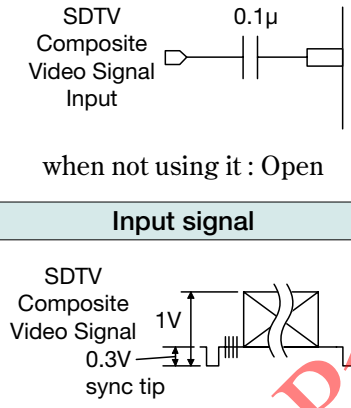


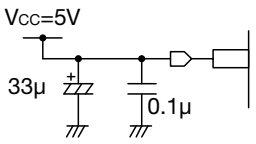
TSOP-16B
(TOP VIEW)

1	Vin	9	GND2
2	Vcc1	10	Prout
3	PYin	11	Pbout
4	Bias	12	PYout sag
5	Pbin	13	PYout
6	GND1	14	Vout sag
7	Prin	15	Vout
8	CTRL	16	Vcc2

Pin Description

<table>
<tr><th>Pin No.</th><th>Pin name</th><th colspan="2">Pin description</th></tr>
<tr><td rowspan="4">1</td><td rowspan="4">V_{in}</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Composite Video Signal Input
Pin to input composite video signals
Clamp input pin

Pin voltage : 1.3V (typ.)</td></tr>
<tr><td>External circuit</td><td>Internal equivalent circuit</td></tr>
<tr><td> 
</td></tr>
<tr><td rowspan="4">2
16</td><td rowspan="4">$V_{CC}1$
$V_{CC}2$</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Voltage Supply
Pin to apply a positive supply voltage. Apply 5V.
Pin2 and Pin16 are not shorted inside the IC.
$V_{CC}2$ is connected to an output stage circuit, and $V_{CC}1$ is connected to a circuit other than an output stage circuit.

Note : Please arrange power supply bypass capacitor near the terminal.</td></tr>
<tr><td>External circuit</td><td>Internal equivalent circuit</td></tr>
<tr><td> 
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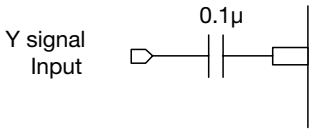
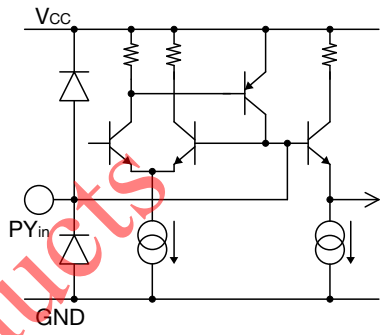
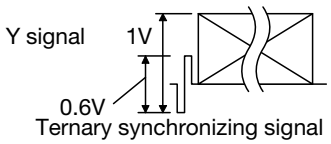
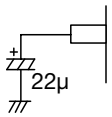
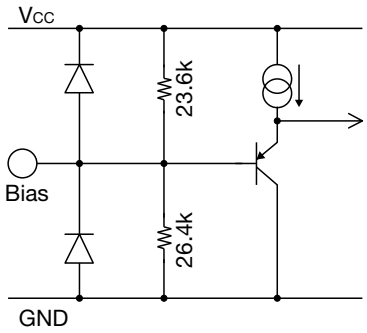
</table>

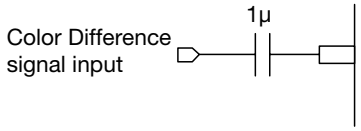
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="5">3</td><td rowspan="5">PY_{in}</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">Y Signal Input (for HD)
Pin to input Y signals.
Clamp input pin.

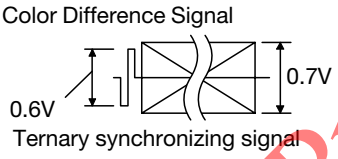
Pin voltage : 1.3V (typ.)</td></tr>
<tr><td>External circuit</td><td>Internal equivalent circuit</td></tr>
<tr><td>Y signal Input
 

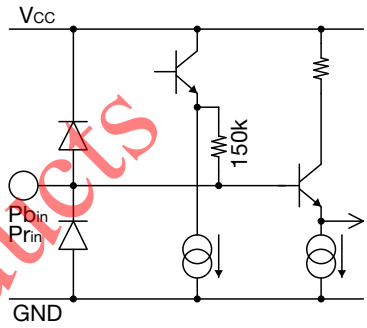
when not using it : Open</td><td rowspan="2"> 
</td></tr>
<tr><td>Input signal
 
</td></tr>
<tr><td rowspan="5">4</td><td rowspan="5">Bias</td><td colspan="2">Function</td></tr>
<tr><td colspan="2">bias
All the reference voltages used inside the IC are produced according to the resistance divider of this pin.
Pin to stabilize reference voltages, and reduce both power supply ripple and crosstalk by decreasing impedance with an external 22µF.</td></tr>
<tr><td>External circuit</td><td>Internal equivalent circuit</td></tr>
<tr><td> 

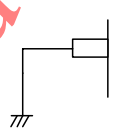
when not using it : Open</td><td rowspan="2"> 
</td></tr>
<tr><td>Input signal</td></tr>
</table>

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">5
7</td><td rowspan="4">Pb_{in}
Pr_{in}</td><td>Function</td></tr>
<tr><td>Color Difference Signal Input (for HD)
Pin to input color difference signals.
Bias input pin.

Pin voltage : 2.6V (typ.)
Input impedance : 150kΩ (typ.)</td></tr>
<tr><td>External circuit / Internal equivalent circuit</td></tr>
<tr><td>


when not using it : Open
Input signal


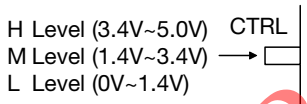


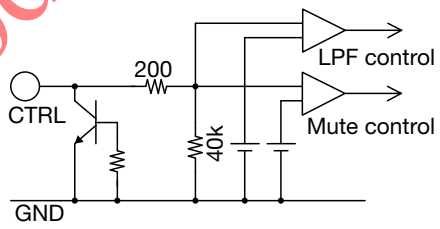
</td></tr>
<tr><td rowspan="4">6
9</td><td rowspan="4">GND1
GND2</td><td>Function</td></tr>
<tr><td>Ground
Ground pin.</td></tr>
<tr><td>External circuit / Internal equivalent circuit</td></tr>
<tr><td>

Input signal
</td></tr>
</table>

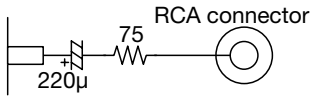
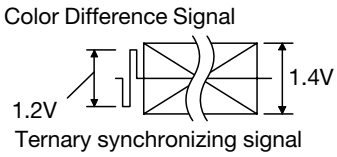
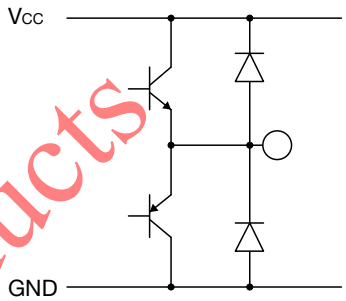
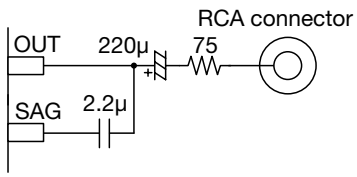
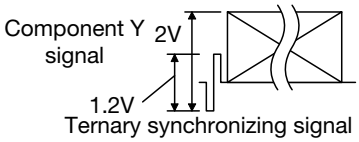
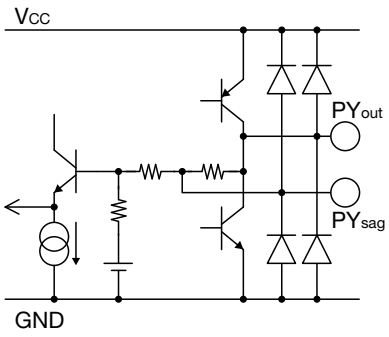
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Pin description</th></tr>
<tr><td rowspan="4">8</td><td rowspan="4">CTRL</td><td>Function</td></tr>
<tr><td>LPF select
Mute control

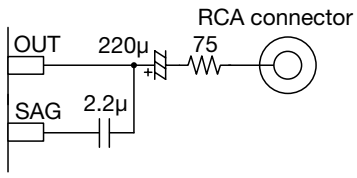
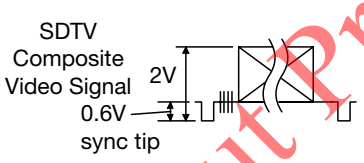
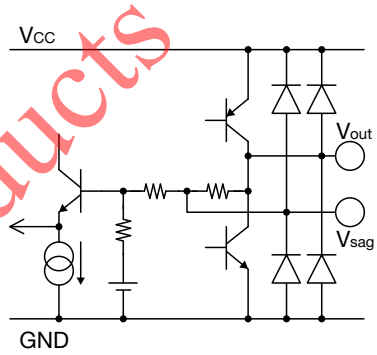
LPF band selection and all output mute ON/OFF of PY/Pb/Pr can be selected according to the voltage applied to this pin.
L level applied ··· Mute ON
M level applied ··· Mute OFF, LPF passband 13.5MHz selected
H level applied ··· Mute OFF, LPF passband 30MHz selected

L level input voltage : max.0.4V
M level input voltage : min.1.4V max.3.0V
H level input voltage : min.3.5V max.5.0V

Input impedance : 40kΩ (typ.)</td></tr>
<tr><td>External circuit
 

Input signal</td><td>Internal equivalent circuit
 
</td></tr>
</table>

Pin No.	Pin name	Pin description
10 11	Pb_{out} Pr_{out}	**Function** Color Difference Signal Pb/Pr Output Pin to output color difference signals. Bias output pin. Pin voltage : 2.70V (typ.) Output Dynamic Range : 2.8Vp-p (typ.) Keep the wire as short as possible between each video output pin and 75Ω. **External circuit**  **Input signal**  **Internal equivalent circuit** 
12 13	$PY_{out\ sag}$ PY_{out}	**Function** Component Y Signal Output Pin to output component Y signals. Clamp output pin. Pin voltage : SAG terminal is not used 0.9V (typ.) SAG terminal is used 0.4V (typ.) Output Dynamic Range : 2.8Vp-p (typ.) Keep the wire as short as possible between each video output pin and 75Ω. **External circuit**  **Input signal**  **Internal equivalent circuit** 

Pin No.	Pin name	Pin description
14 15	$V_{out\ sag}$ V_{out}	**Function** Composite Video Signal Output Pin to output composite video signals. Clamp output pin. Pin Voltage : SAG terminal is not used 0.9V (typ.) SAG terminal is used 0.4V (typ.) Output Dynamic Range : 2.8Vp-p (typ.) Keep the wire as short as possible between each video output pin and 75Ω. **External circuit**  **Input signal**  **Internal equivalent circuit** 

Absolute Maximum Ratings (Except where noted otherwise Ta=25°C)

Parameter	Symbol	Ratings	Units
Storage temperature	T_{stg_s}	−55~+150	°C
Operating temperature	T_{opr_s}	−40~+85	°C
Supply voltage	$V_{CC\ max.\_s}$	6	V
Junction Temperature	$T_{jmax.}$	150	°C
Power dissipation (Note1)	Pd_s	1.0	W

Note1 : When mounting on the board made of the glass epoxy. (40×40×1.6mm)

Recommended Operating Conditions

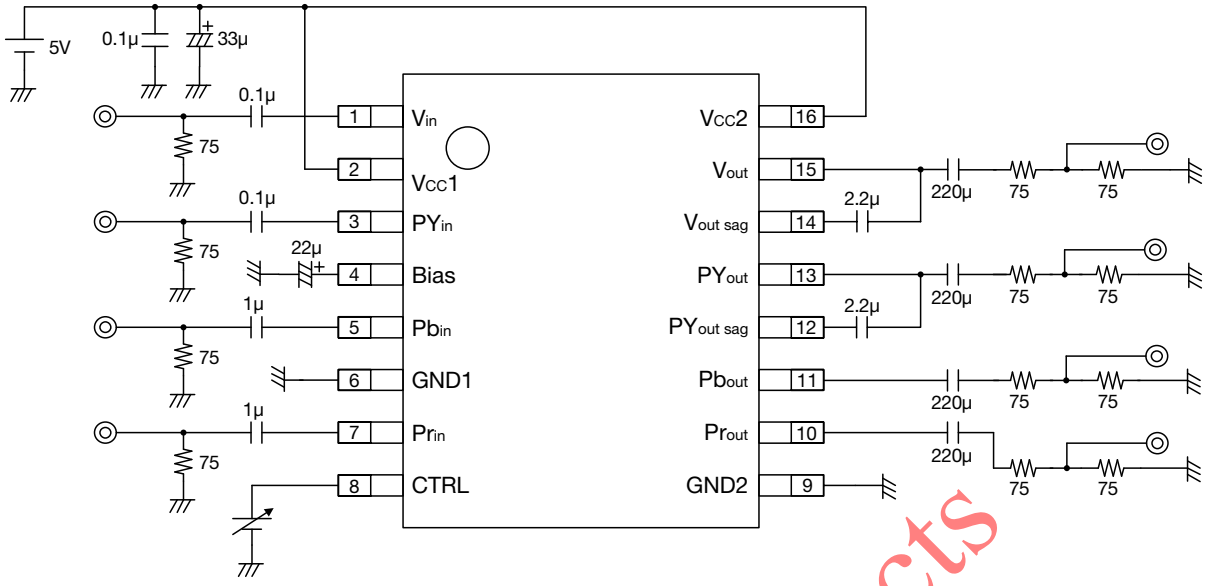
Parameter	Symbol	Ratings	Units
Operating temperature	T_{opr_s}	−40~+85	°C
Operating voltage	V_{ccop_s}	4.5~5.5	V

Electrical Characteristics (Except where noted otherwise Ta=25°C, Vcc1, Vcc2=5V)

Parameter		Symbol	Test conditions	Min.	Typ.	Max.	Units
Supply current 1		$I_{CC}1$	No signal	35	50	65	mA
Supply current 2		$I_{CC}2$	No signal Mute ON	1.8	2.5	3.2	mA
Terminal voltage	Composite video input	V_{Vin}		1.1	1.3	1.5	V
	Luminance input	V_{PYin}		1.1	1.3	1.5	V
	Component input	$V_{Pbin,\ Prin}$		2.3	2.6	2.9	V
	Composite video output 1	$V_{Vout}1$	14pin–15pin short-circuited		0.90		V
	Composite video output 2	$V_{Vout}2$	Sag terminal used		0.40		V
	Luminance output 1	$V_{Vout}1$	12pin–13pin short-circuited		0.90		V
	Luminance output 2	$V_{Vout}2$	Sag terminal used		0.40		V
	Component output	$V_{Pbout,\ Prout}$			2.70		V

Parameter		Symbol	Test conditions	Min.	Typ.	Max.	Units
Output dynamic range		DR_V	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V
		$DR_{PY, Pb, Pr}$	SIN wave : 100kHz, THD=1.0%	2.6	2.8		V
Control terminal input voltage	H	VthH		3.5		5.0	V
	M	VthM		1.4		3.0	V
	L	VthL				0.4	V
Control terminal input current	H	I_H	V_H=5V			190	µA
	M	I_M	V_M=3V			115	µA
	L	I_L	V_L=0.4V			15	µA
Input impedance		$Z_{Pbin,Prin}$		100	150	200	kΩ
Voltage gain		GV	SIN wave : 1V, f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic (V)		f1	SIN wave : 1V, 6.75MHz/100kHz	–1	0	1	dB
		f2	SIN wave : 1V, 27MHz/100kHz		–33	–27	dB
Frequency characteristic (PY, Pb, Pr-SD)		f3	SIN wave : 1V, 13.5MHz/100kHz	–1	0	1	dB
		f4	SIN wave : 1V, 54MHz/100kHz		–33	–27	dB
Frequency characteristic (PY-HD)		f5	SIN wave : 1V, 30MHz/100kHz	–1	0	1	dB
		f6	SIN wave : 1V, 74MHz/100kHz		–33	–27	dB
Frequency characteristic (Pb, Pr-HD)		f7	SIN wave : 1V, 15MHz/100kHz	–1	0	1	dB
		f8	SIN wave : 1V, 30MHz/100kHz	–3.0	–1.0	1.0	dB
		f9	SIN wave : 1V, 74MHz/100kHz		–33	–27	dB
Group delay (V)		t1	at 100kHz		45	80	ns
Group delay (PY, Pb, Pr)		t2	at 100kHz		25	50	ns
Group delay deviation 1 (V)		⊿t1	to 3.58MHz		4	10	ns
			to 4.43MHz		6	10	ns
			to 6MHz		12	20	ns
Group delay deviation 2 (PY, Pb, Pr)		⊿t2	to 4MHz		1	10	ns
			to 24MHz		6	15	ns
Between channel Group delay deviation 1		$⊿t1_{ch}$	Between PY and Pb (Pr) at 4MHz		1	10	ns
Differential gain		DG	Staircase signal 1V		0.5	2.0	%
Differential phase		DP	Staircase signal 1V		0.5	2.0	°
Crosstalk 1		CT1	f=4.43MHz, 1V		–60	–55	dB
Crosstalk 2		CT2	f=20MHz, 1V		–45	–40	dB
S/N 1		SN1	BW : 100k ~ 6MHz		–80		dB
S/N 2		SN2	BW : 100k ~ 6MHz at SD select		–80		dB
S/N 3		SN3	BW : 100k ~ 30MHz at HD select		–66		dB

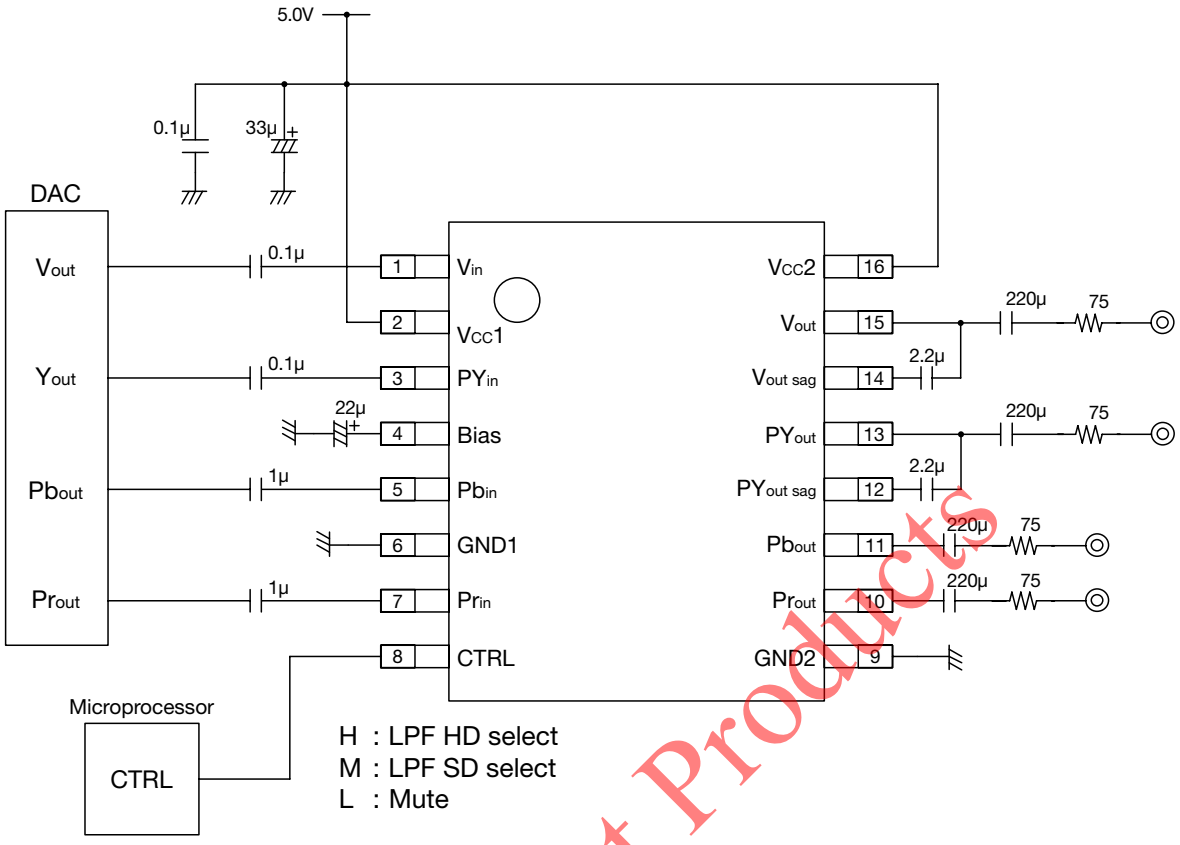
Measuring Circuit



Switch Control Table

CTRL-Pin	Mute	SD/HD select
H (3.5V~ 5.0V)	OFF	HD
M (1.4V~ 3.0V)	OFF	SD
L (0V~ 0.4V)	ON	
OPEN	ON	

Application Circuit



Note : Please arrange power supply bypass capacitor near the V_{CC} terminal (pin).

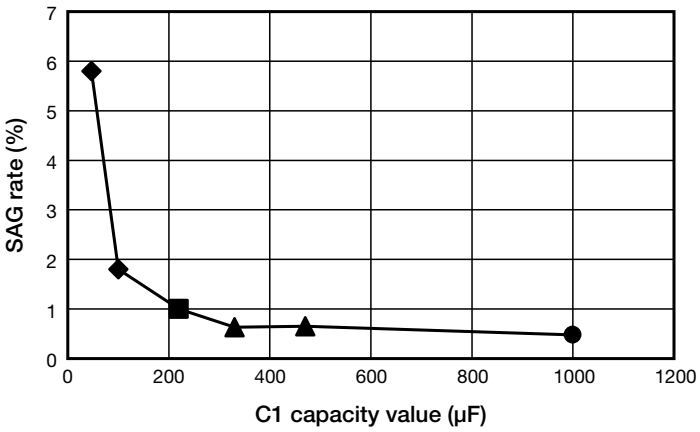
Note : Please arrange the stray capacity component added to a signal output terminal to 20pF or less.

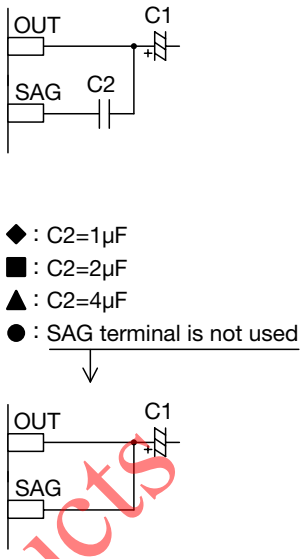
Note : Keep the wire as short as possible between each video output pin and 75Ω.

Note : Please use it after it confirms it enough by the installing set when you use applied circuit.

Supplemental 1 : SAG terminal

Please design the capacitor that connects it with the terminal SAG referring to the figure below.

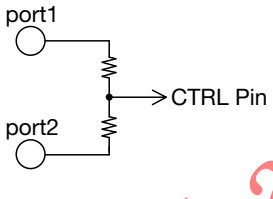




Supplemental 2 : CTRL terminal

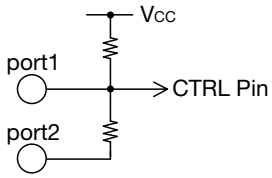
Please refer to figure shown below when you use microprocessor without three value output.

For CMOS output



port1	port2	CTRL
H	H	H
H	L	M
L	H	M
L	L	L

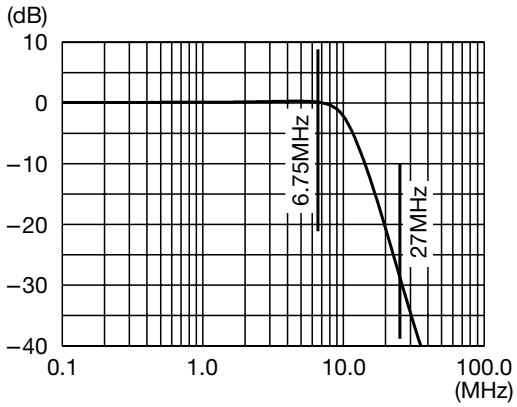
For NMOS open drain output



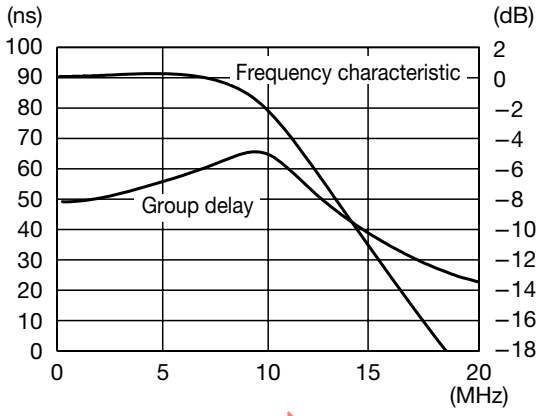
port1	port2	CTRL
H	H	H
H	L	M
L	H	L
L	L	L

Characteristics

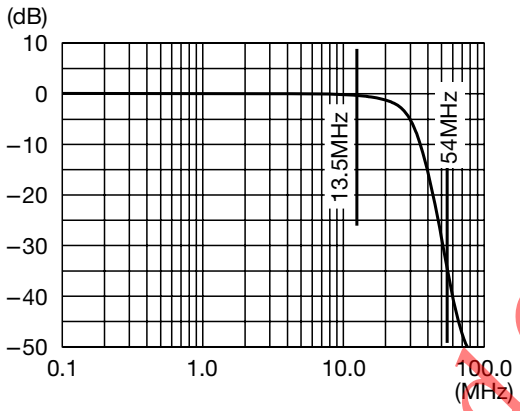
Frequency characteristic (V_{out})



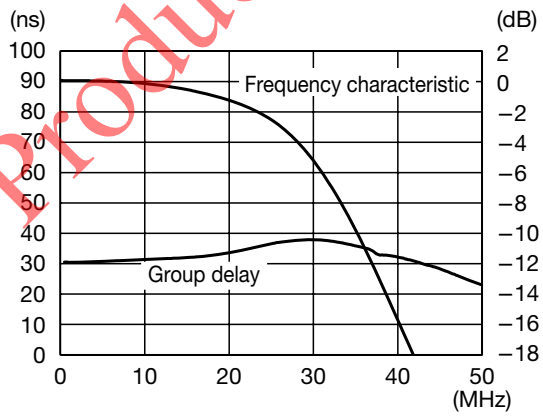
Group delay (V_{out})



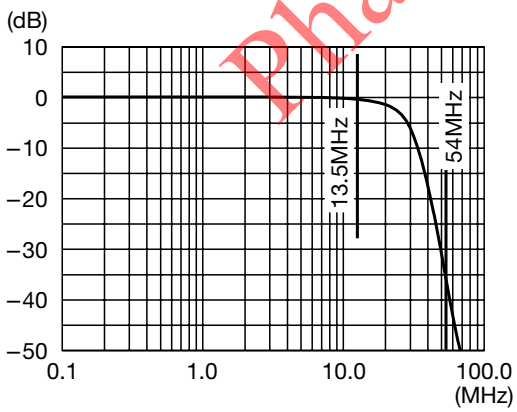
Frequency characteristic (PY_{out} at SD select)



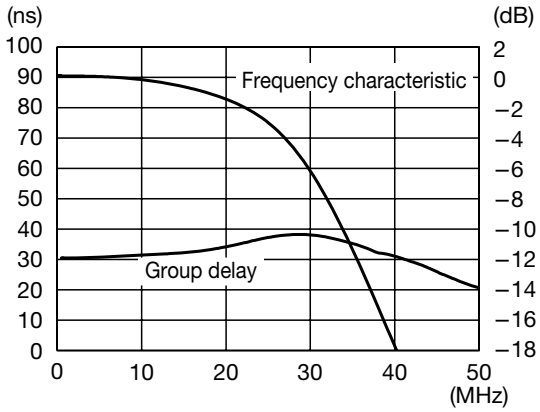
Group delay (PY_{out} at SD select)



Frequency characteristic (Pb_{out}/Pr_{out} at SD select)

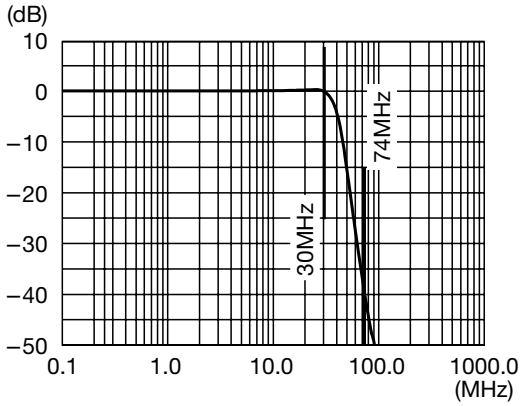


Group delay (Pb_{out}/Pr_{out} at SD select)

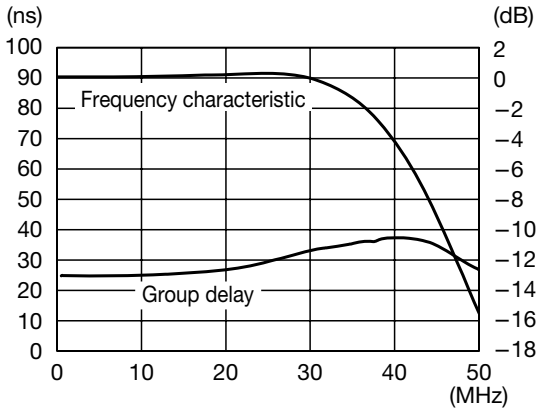


Note : The measurement point of all data is a middle point of 75Ω.

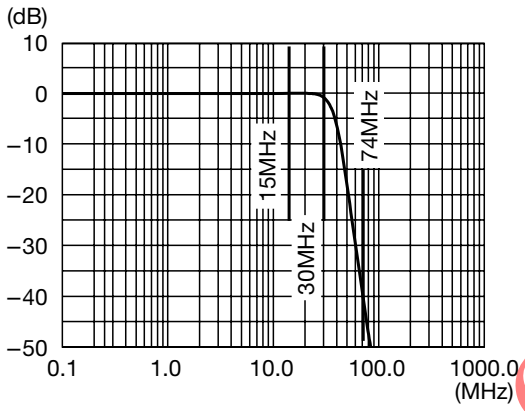
Frequency characteristic (PY$_{out}$ at HD select)



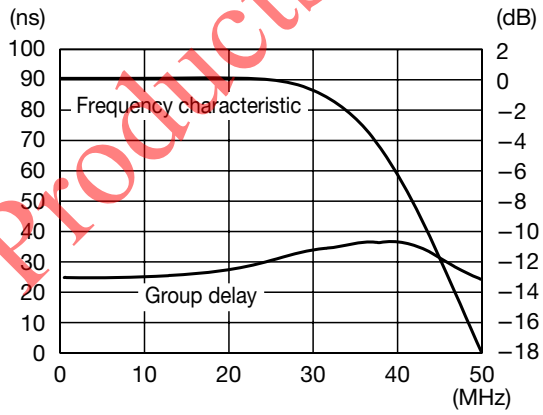
Group delay (PY$_{out}$ at HD select)



Frequency characteristic (Pb$_{out}$/Pr$_{out}$ at HD select)



Group delay (Pb$_{out}$/Pr$_{out}$ at HD select)



Note : The measurement point of all data is a middle point of 75Ω.