

# I<sup>2</sup>C BUS AV-SW IC

## Monolithic IC MM1783

### Outline

This IC is a full HD compatible I<sup>2</sup>C BUS controlled audio video switch IC for LCD (middle-end to high-end), PDP, and rear-projection televisions.

- |   |  |  |
|---|--|--|
| · Operating supply voltage:<br>using two power supplies<br>Vcc1: 8.5V - 9.5V<br>Vcc2: 4.5V - 5.5V | · Input channels:<br>Composite video input: 7 channels<br>S Video input: 4 channels<br>Component input: 3 channels<br>Audio input: 10 channels | · Output channels<br>Video output: 3 channels<br>Audio input: 3 channels |
|---|--|--|

### Features

1. Full HD compatible (frequency response -3dB at 100MHz, for OUT1 only)
2. Integrates video and audio outputs into one chip
3. Enables RGB input (1600 x 1200 max. [UXGA])
4. Three type of LPF cutoff frequency can be selected.  
(OUT1, OUT2 fBW [=7MHz, 13MHz], fC [=24MHz])
5. Includes a 75Ω driver for monitor output (D1 resolution)
6. Supports S1/S2-terminal detection
7. Supports D-terminal detection
8. Detailed power saving function allows reduction in power consumption of unused circuits.
9. If D4 output is used, D4 mode function allows further reduction in power consumption.
10. Complies with the CENELEC SCART standard

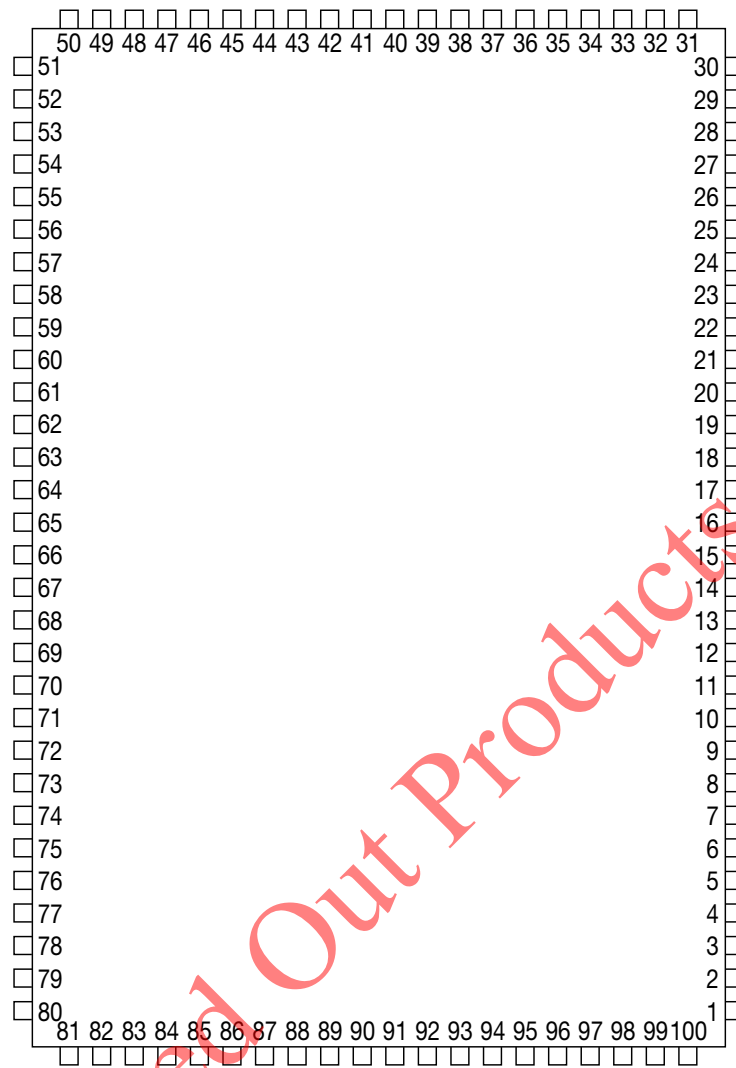
### Package

QFP-100A

### Applications

1. LCD TV (middle-end to high-end TV)
2. Plasma TV
3. Rear-projection TV
4. CRT TV

Pin Assignment

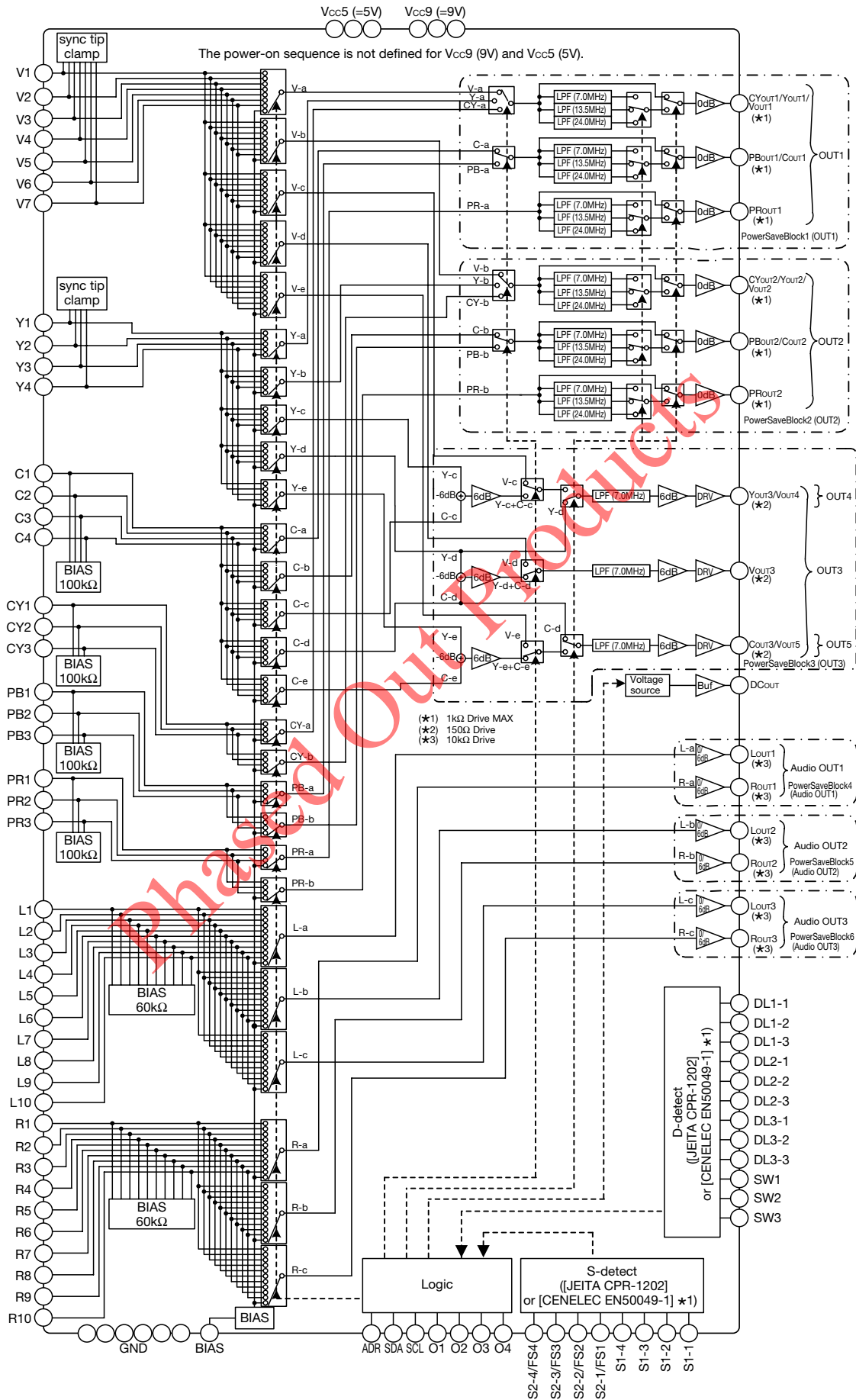


QFP-100A  
(TOP VIEW)

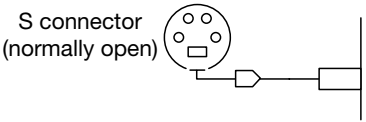
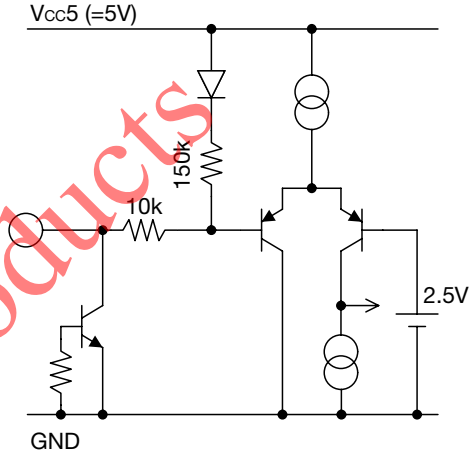
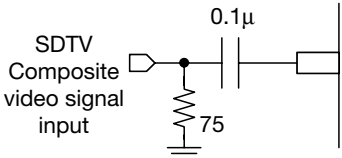
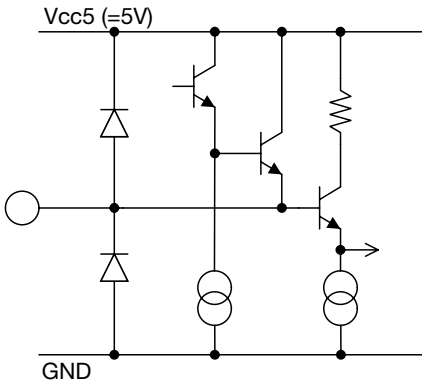
1	S1-1	21	S2-4/FS4	41	R10	61	Vcc9	81	DL1-1
2	Y1	22	C4	42	L10	62	DCout	82	CY1
3	S2-1/FS1	23	O3	43	R9	63	Cout3	83	DL2-1
4	C1	24	V5	44	L9	64	GND	84	PB1
5	O1	25	GND	45	R8	65	Vout3	85	DL3-1
6	V2	26	V6	46	L8	66	Vcc5	86	PR1
7	S1-2	27	Vcc5	47	R7	67	Yout3	87	DL1-2
8	Y2	28	V7	48	L7	68	GND	88	CY2
9	S2-2/FS2	29	O4	49	R6	69	PRout2	89	DL2-2
10	C2	30	GND	50	L6	70	PBout2	90	PB2
11	BIAS	31	SCL	51	R5	71	CYout2	91	DL3-2
12	V3	32	SDA	52	L5	72	Vcc9	92	PR2
13	S1-3	33	Vcc9	53	R4	73	PRout1	93	DL1-3
14	Y3	34	Rout3	54	L4	74	PBout1	94	CY3
15	S2-3/FS3	35	Lout3	55	R3	75	CYout1	95	DL2-3
16	C3	36	Rout2	56	L3	76	ADR	96	PB3
17	O2	37	Lout2	57	R2	77	SW3	97	DL3-3
18	V4	38	Rout1	58	L2	78	SW2	98	PR3
19	S1-4	39	Lout1	59	R1	79	SW1	99	Vcc5
20	Y4	40	GND	60	L1	80	GND	100	V1

\*: Vcc9=9V, Vcc5=5V

Block Diagram

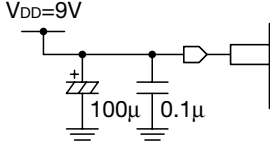
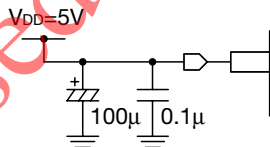


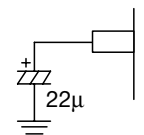
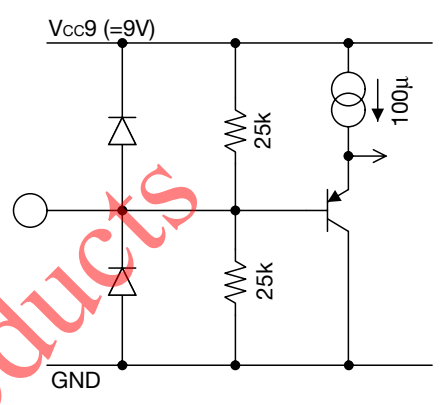
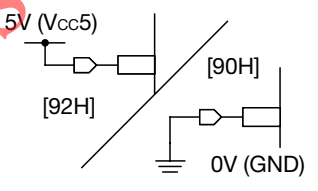
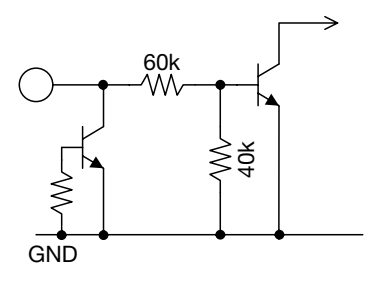
Pin Description

Pin No.	Pin name	Pin description	
1 7 13 19	S1-1 S1-2 S1-3 S1-4	<b>Function</b>	
		The terminal which detects the connection state of S connector A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers & threshold])  Threshold: 2.4V typ. Input impedance: 160kΩ typ.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>S connector (normally open)</p> <p>When not using it: open</p>	 <p>Vcc5 (=5V)</p> <p>150k</p> <p>10k</p> <p>2.5V</p> <p>GND</p>
		<b>Input signal</b>	
DC voltage: 0V (GND) or OPEN Note: When you impress voltage to a terminal, make it less than [6V].			
2 8 14 20	Y1 Y2 Y3 Y4	<b>Function</b>	
		Luminance signal input Input clamp Pin voltage: 1.9V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>SDTV Composite video signal input</p> <p>0.1μ</p> <p>75</p> <p>When not using it: open</p>	 <p>Vcc5 (=5V)</p> <p>75</p> <p>0.3V sync tip</p> <p>GND</p>
		<b>Input signal</b>	
Luminance signal 1V 0.3V sync tip			

Pin No.	Pin name	Pin description												
3 9 15 21	S2-1/FS1 S2-2/FS2 S2-3/FS3 S2-4/FS4	<b>Function</b>												
		<p>The terminal which detects the aspect ratio information of S connector, or which detects the voltage of FS pin of a SCART interface.</p> <p>Note: When it is used for FS (Function Switching), connect outside circuit as the resistance division of 47kΩ and 33kΩ</p> <p>Threshold 1: 1.2V typ. Threshold 2: 3.1V typ. Input impedance: 150kΩ typ.</p>												
		<b>External circuit</b>												
		<b>Input signal</b>												
		<p>DC voltage:</p> <table border="1"> <thead> <tr> <th></th> <th>S2</th> <th>FS</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0V</td> <td>0-2V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> <td>4.5-7V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> <td>9.5-12V</td> </tr> </tbody> </table>		S2	FS	L	0V	0-2V	M	1.4-2.4V	4.5-7V	H	3.5-5V	9.5-12V
	S2	FS												
L	0V	0-2V												
M	1.4-2.4V	4.5-7V												
H	3.5-5V	9.5-12V												
4 10 16 22	C1 C2 C3 C4	<b>Function</b>												
		<p>Chroma signal input</p> <p>Input bias</p> <p>Pin voltage: 3.2V typ.</p> <p>Input impedance: 100kΩ typ.</p> <p>Input dynamic range: 1.3V<sub>P-P</sub> min.</p>												
		<b>External circuit</b>												
		<b>Input signal</b>												

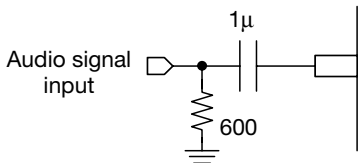
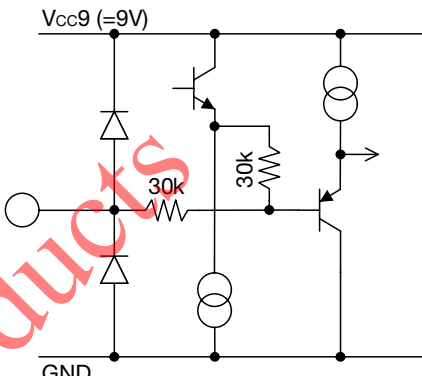
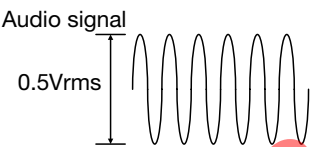
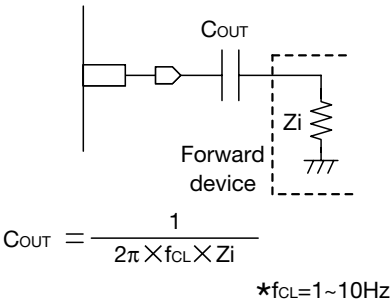
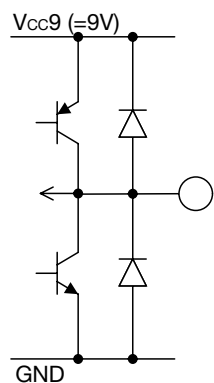
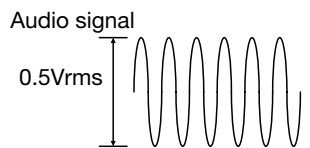
Pin No.	Pin name	Pin description																							
5 17 23 29	O1 O2 O3 O4	<b>Function</b>																							
		Output port It is the open collector type general-purpose output port in which I <sup>2</sup> C control is possible.  Sink current min.: 5mA																							
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																						
		<b>Input signal</b>																							
		DC voltage: <table border="1" style="display: inline-table; margin-right: 20px;"> <tr><td><b>b53</b></td><td><b>O1 (5pin)</b></td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open (High)</td></tr> </table> <table border="1" style="display: inline-table; margin-right: 20px;"> <tr><td><b>b52</b></td><td><b>O2 (17pin)</b></td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open (High)</td></tr> </table> <table border="1" style="display: inline-table; margin-right: 20px;"> <tr><td><b>b51</b></td><td><b>O3 (23pin)</b></td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open (High)</td></tr> </table> <table border="1" style="display: inline-table;"> <tr><td><b>b50</b></td><td><b>O4 (29pin)</b></td></tr> <tr><td>0</td><td>Low</td></tr> <tr><td>1</td><td>Open (High)</td></tr> </table>		<b>b53</b>	<b>O1 (5pin)</b>	0	Low	1	Open (High)	<b>b52</b>	<b>O2 (17pin)</b>	0	Low	1	Open (High)	<b>b51</b>	<b>O3 (23pin)</b>	0	Low	1	Open (High)	<b>b50</b>	<b>O4 (29pin)</b>	0	Low
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6 12 18 24 26 28 100	V2 V3 V4 V5 V6 V7 V1	<b>Function</b>																							
		Composite signal input Input clamp Pin voltage: 1.9V typ. Input dynamic range: 1.3V <sub>P-P</sub> min.																							
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																						
		<b>Input signal</b>																							

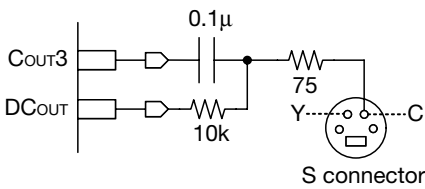
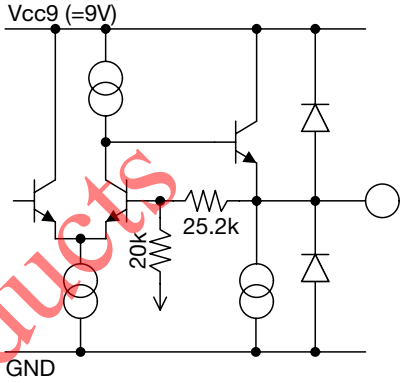
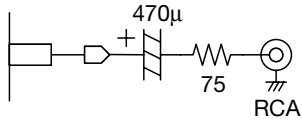
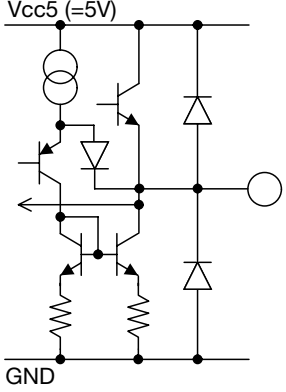
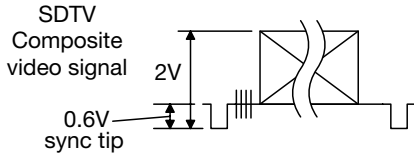
Pin No.	Pin name	Pin description	
33 61 72	V <sub>CC9</sub>	<b>Function</b>	
		<p>Voltage supply 1</p> <p>It is a supply voltage impression terminal. Please impress 9V. 33 pin, 61 pin and 72 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about V<sub>CC9</sub> (9V) and V<sub>CC5</sub> (5V). Please arrange a bypass capacitor near the terminal.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>	
		DC Voltage: +8.0~+10.0V	
27 66 99	V <sub>CC5</sub>	<b>Function</b>	
		<p>Voltage supply 2</p> <p>It is a supply voltage impression terminal. Please impress 5V. 27 pin, 66pin and 99 pin short-circuit inside IC. There is no regulation of the sequence of a power supply injection about V<sub>CC9</sub> (9V) and V<sub>CC5</sub> (5V). Please arrange a bypass capacitor to the terminal latest as much as possible.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
			
		<b>Input signal</b>	
		DC Voltage: +4.5~+5.5V	
25 30 40 64 68 80	GND	<b>Function</b>	
		<p>Ground</p> <p>It is a Ground terminal. 25pin, 30pin, 40pin, 64pin, 68pin and 80pin short-circuit inside IC.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		<b>Input signal</b>	

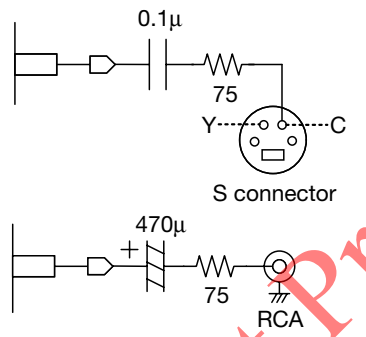
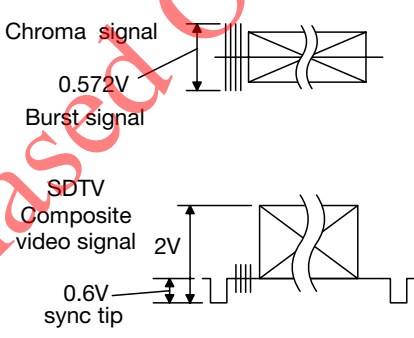
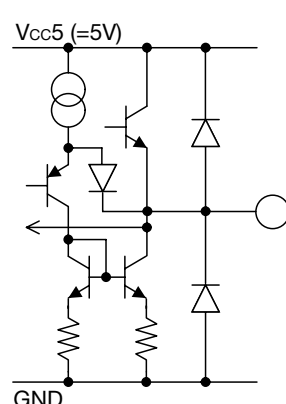
Pin No.	Pin name	Pin description	
11	BIAS	<b>Function</b>	
		<p><b>BIAS</b>                      All the reference voltage used inside IC is made based on resistance division of this terminal. It is the terminal which connects a filter capacitor to stabilize the reference voltage.</p> <p>Input impedance: 12.6kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Input signal</b>	
76	ADR	<b>Function</b>	
		<p><b>Slave address select pin</b>                      The I<sup>2</sup>C slave addresses 90H and 92H can be chosen with the voltage impressed to this terminal. It is set to 90H by Low, and is set to 92H by High.</p> <p>Threshold: 1.75V typ.                      Input impedance: 100kΩ typ.</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>	
		<b>Input signal</b>	
		<p>DC Voltage:                      0V (GND) to 5V (Vcc5)</p>	

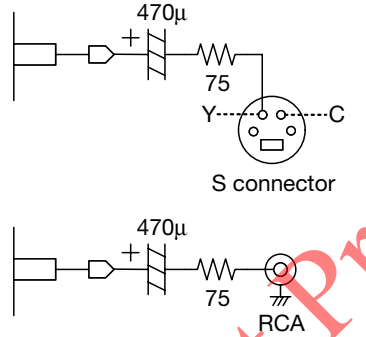
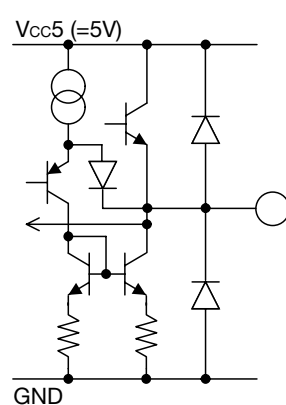
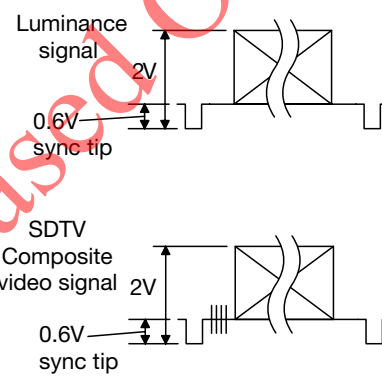
Pin No.	Pin name	Pin description
31	SCL	<b>Function</b>
		Clock input of I <sup>2</sup> C BUS It is the terminal which connects the SCL line of I <sup>2</sup> C BUS.
		<b>External circuit</b>
		<b>Input output signal</b>
		<b>Equivalent circuit diagram</b>
32	SDA	<b>Function</b>
		DATA I/O of I <sup>2</sup> C BUS It is the terminal which connects the SDA line of I <sup>2</sup> C BUS.
		<b>External circuit</b>
		<b>Input signal</b>
		<b>Equivalent circuit diagram</b>

Phased Out Products

Pin No.	Pin name	Pin description
41~60	L1~L10 R1~R10	<b>Function</b>
		<p>Audio line input</p> <p>Pin to input audio signals. It includes 10 channels; L1-L10, R1-R10.</p> <p>Pin voltage: 3.80V typ.</p> <p>Input impedance: 60kΩ typ.</p> <p>Input dynamic range: 3Vrms typ.</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		 <p>When not using it: connect to GND with 0.1μF</p>
		
		<b>Input signal</b>
		
34~39	Lout1~3 Rout1~3	<b>Function</b>
		<p>Audio line output</p> <p>Pin to output audio signals</p> <ul style="list-style-type: none"> <li>Select voltage gain 0dB or 6dB with control registers b44 - b46.</li> </ul> <p>Audio line output 1 (b46=0: 0dB mode, b46=1: 6dB mode)</p> <p>Audio line output 2 (b45=0: 0dB mode, b45=1: 6dB mode)</p> <p>Audio line output 3 (b44=0: 0dB mode, b44=1: 6dB mode)</p> <p>Pin voltage: 4.50V typ.</p> <p>Voltage gain: 0dB/6dB typ.</p> <p>Frequency characteristic: -3dB at 50kHz min.</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		 <p>When not using it: open</p>
		
		<b>Input signal</b>
		

Pin No.	Pin name	Pin description																			
62	DC <sub>OUT</sub>	<b>Function</b>																			
		DC output for S terminal It is the terminal which outputs S1/S2 signal of S terminal. The ternary output of L/M/H is controllable by I <sup>2</sup> C control. (refer to Table of status registers and Details of the contents of control)																			
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																		
		 <p style="text-align: center;">When not using it: open</p>																			
<b>Output signal</b>																					
DC voltage:																					
<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th></th> <th>b27</th> <th>b26</th> <th>DC<sub>OUT</sub></th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0</td> <td>0</td> <td>0V</td> </tr> <tr> <td>M</td> <td>0</td> <td>1</td> <td>2.2V</td> </tr> <tr> <td>H</td> <td>1</td> <td>0</td> <td>5V</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>Hi-Imp</td> </tr> </tbody> </table>					b27	b26	DC <sub>OUT</sub>	L	0	0	0V	M	0	1	2.2V	H	1	0	5V		1
	b27	b26	DC <sub>OUT</sub>																		
L	0	0	0V																		
M	0	1	2.2V																		
H	1	0	5V																		
	1	1	Hi-Imp																		
65	V <sub>OUT3</sub>	<b>Function</b>																			
		Monitor output (composite signal) It is a terminal for a composite signal external output. V or Y+C (MIX) can be chosen. (refer to Details of the contents of control)  Pin voltage: 1.3V typ. Load resistance: 150Ω Stray capacitance max.: 20pF																			
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>																		
		 <p style="text-align: center;">When not using it: open</p>																			
<b>Output signal</b>																					
SDTV Composite video signal 																					

Pin No.	Pin name	Pin description	
63	Cout3/Vout6	<b>Function</b>	
		<p>Monitor output (chroma or composite signal)</p> <p>It is a terminal for the chroma or composite signal external output. It becomes the chroma output terminal at the time of the separate switch OFF [b24=0], and becomes a composite output terminal at the time of the separate switch ON [b24=1]. C, V, and Y+C (MIX) can be chosen. (refer to Details of the contents of control)</p> <p>Pin voltage: 2.6V typ. [b24=0], 1.3V typ. [b24=1]                      Load resistance: 150Ω                      Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p style="text-align: center;">When not using it: open</p> <p style="text-align: center;"><b>Output signal</b></p> 	

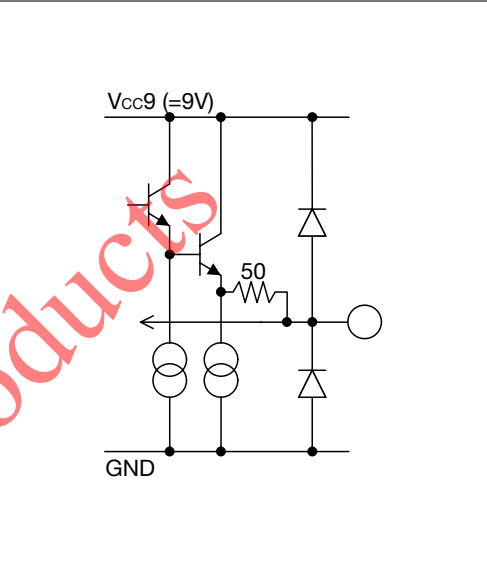
Pin No.	Pin name	Pin description	
67	Yout3/Vout5	<b>Function</b>	
		<p>Monitor output (Luminance or composite signal)</p> <p>It is a terminal for a Luminance or composite signal external output. It becomes a Luminance output terminal at the time of the separate switch OFF [b24=0], and becomes a composite output terminal at the time of the separate switch ON [b24=1]. Y, V, or Y+C (MIX) can be chosen. (refer to Details of the contents of control)</p> <p>Pin voltage: 1.3V typ.                      Load resistance: 150Ω                      Stray capacitance max.: 20pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p style="text-align: center;">When not using it: open</p>	
		<b>Output signal</b>	
 <p>Luminance signal 2V 0.6V sync tip</p> <p>SDTV Composite video signal 2V 0.6V sync tip</p>			

Pin No.	Pin name	Pin description
69	PRout2	<b>Function</b>
		<p>Color difference signal output It is a terminal for a Color difference signal external output.</p> <p>Pin voltage: 4.4V typ. Load resistance min.: 1kΩ Stray capacitance max.: 10pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>
70	PBout2/Cout2	<b>Function</b>
		<p>Color difference signal or Chroma signal output It is a terminal for a Color difference or Chroma signal external output.</p> <p>Pin voltage: 4.4V typ. Load resistance min.: 1kΩ Stray capacitance max.: 10pF</p>
		<b>External circuit</b>
		<b>Equivalent circuit diagram</b>
		<b>Output signal</b>

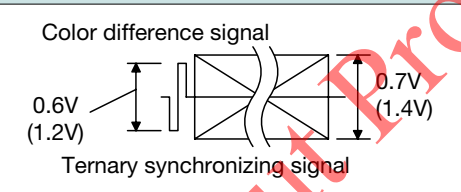
**External circuit**

$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$$
 \*f<sub>CL</sub>=1~10Hz  
 When not using it: open

**Equivalent circuit diagram**



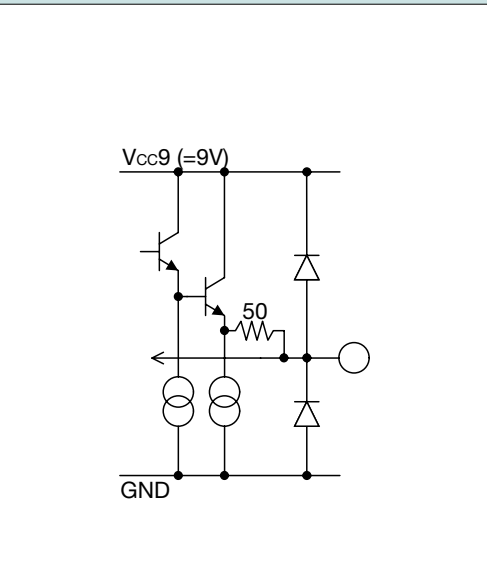
**Output signal**



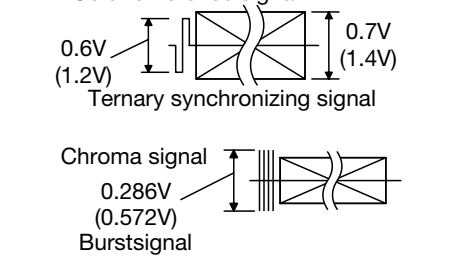
**External circuit**

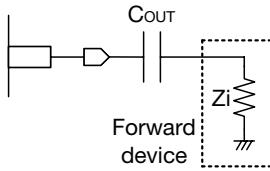
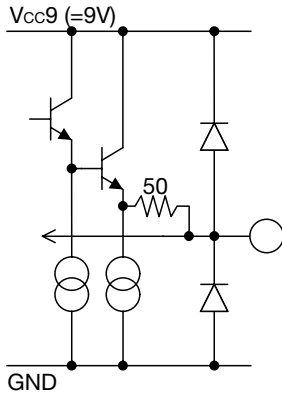
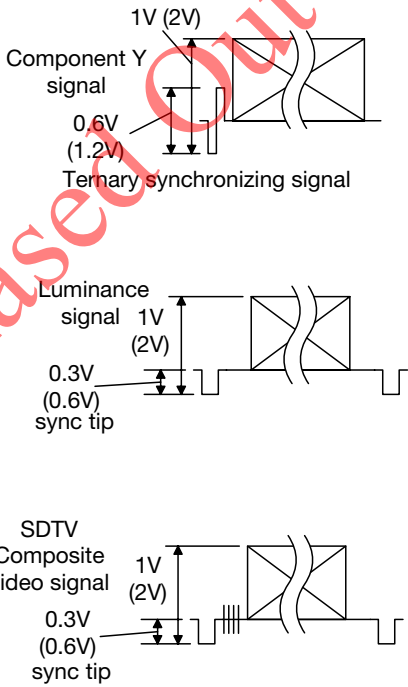
$$C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$$
 \*f<sub>CL</sub>=1~10Hz  
 When not using it: open

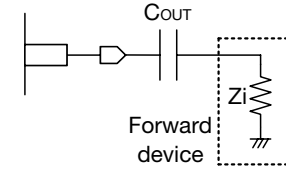
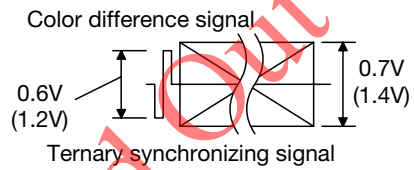
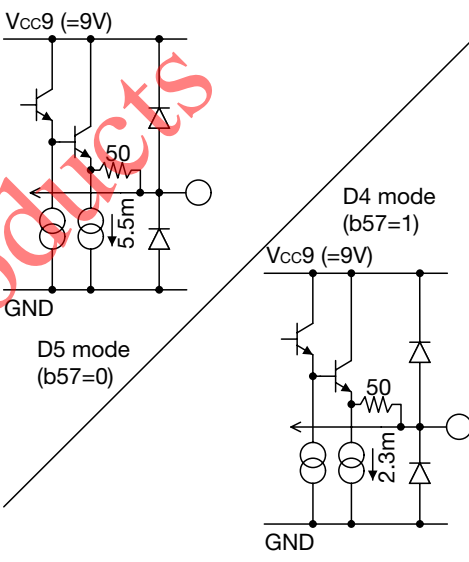
**Equivalent circuit diagram**



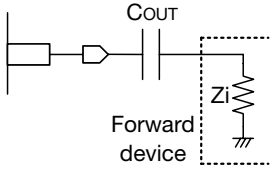

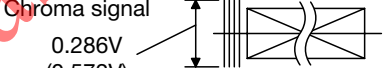
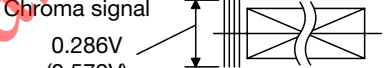
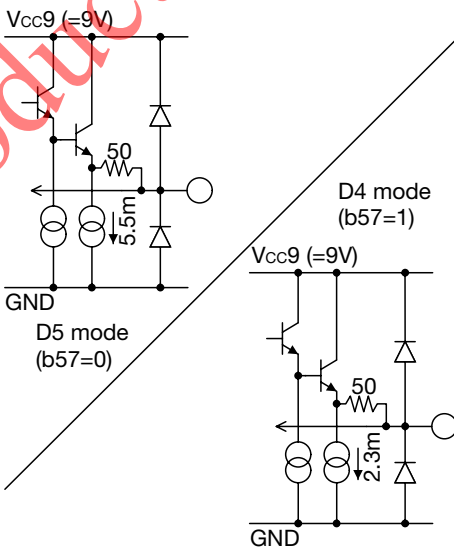
**Output signal**

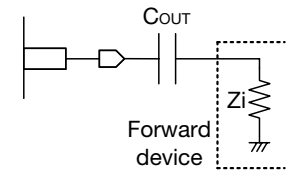
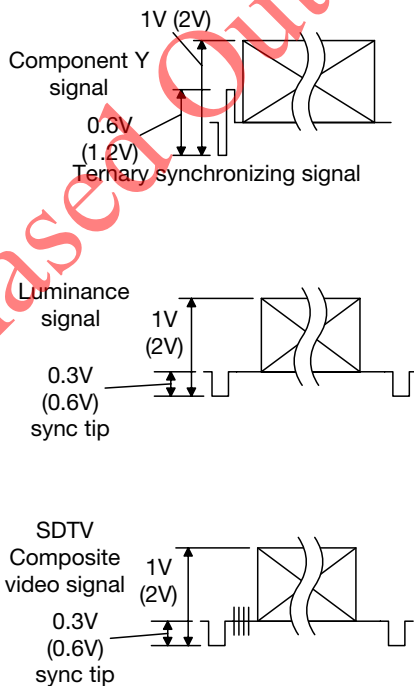
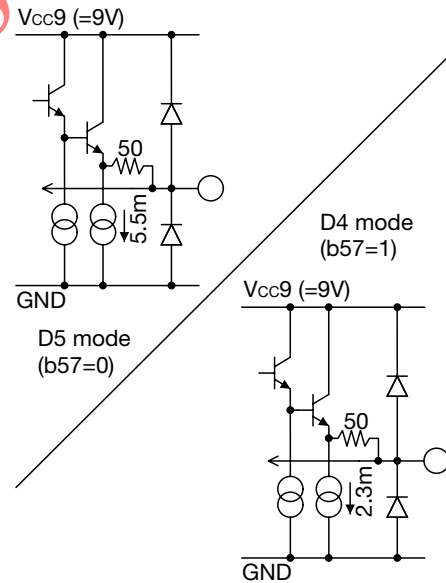


Pin No.	Pin name	Pin description	
71	CY <sub>out2</sub> /Y <sub>out2</sub> /V <sub>out2</sub>	<b>Function</b>	
		<p>Color difference signal , Luminance signal or Composite signal output It is a terminal for a Color difference or Luminance or Composite signal external output.</p> <p>Pin voltage: 2.2V typ. [V, Y] , 4.4V typ. [CY] Load resistance min.: 1kΩ Stray capacitance max.: 10pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f<sub>CL</sub>=1~10Hz</p> <p style="text-align: center;">When not using it: open</p>	
		<b>Output signal</b>	
			

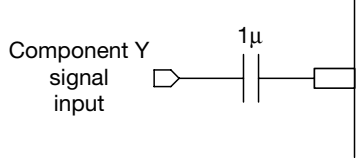
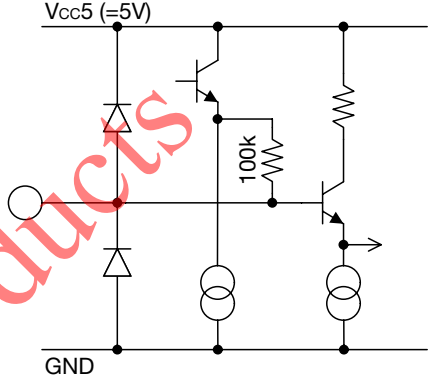
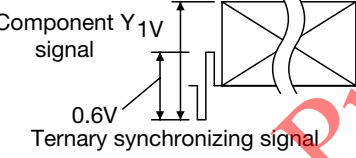
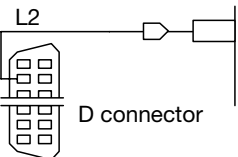
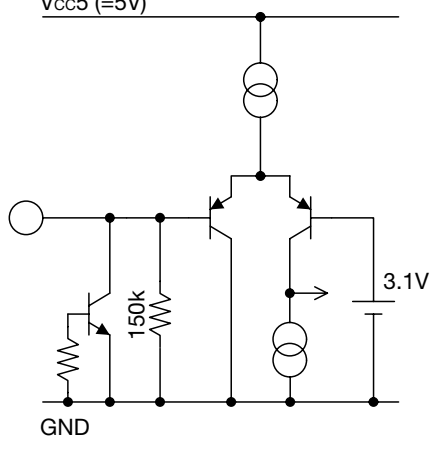
Pin No.	Pin name	Pin description	
73	PR <sub>out1</sub>	<b>Function</b>	
		<p>Color difference signal output</p> <p>It is a terminal for a Color difference signal external output.</p> <p>It can be switched with D5 mode or D4 mode.</p> <p>D4 mode is lower power than D5 mode.</p> <p>Pin voltage: 4.4V typ.</p> <p>Load resistance min.: 1kΩ</p> <p>Stray capacitance max.: 10pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f<sub>CL</sub>=1~10Hz</p> <p style="text-align: center;">When not using it: open</p> <p style="text-align: center;"><b>Output signal</b></p> 	 <p style="text-align: center;">D5 mode (b57=0)</p> <p style="text-align: center;">D4 mode (b57=1)</p>

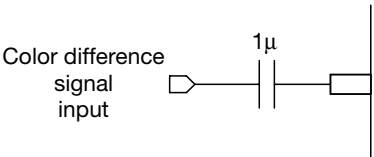
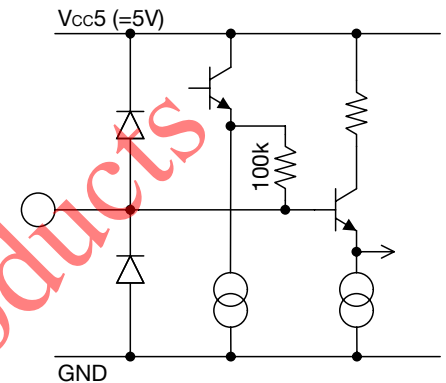
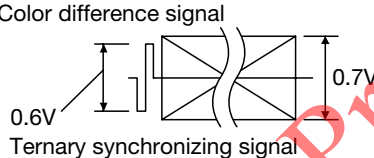
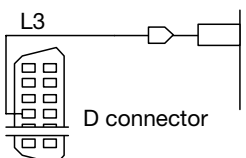
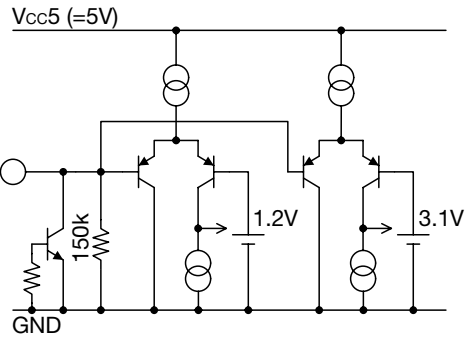
Phased Out Products

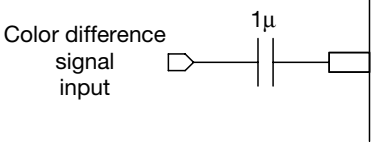
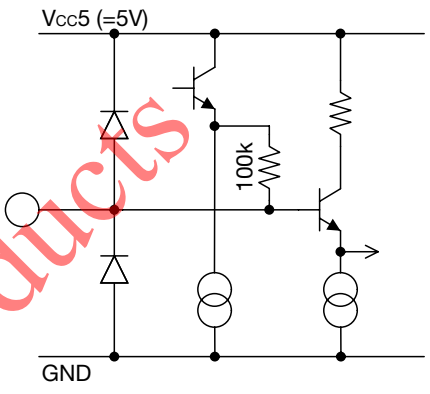
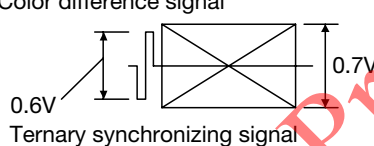
Pin No.	Pin name	Pin description	
74	PBout1/Cout1	<b>Function</b>	
		<p>Color difference signal or Chroma signal output</p> <p>It is a terminal for a Color difference or Chroma signal external output. It can be switched with D5 mode or D4 mode. D4 mode is lower power than D5 mode.</p> <p>Pin voltage: 4.4V typ. Load resistance min.: 1kΩ Stray capacitance max.: 10pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f<sub>CL</sub>=1~10Hz</p> <p>When not using it: open</p> <p><b>Output signal</b></p> <p>Color difference signal              Ternary synchronizing signal              Chroma signal              Burst signal</p>	 <p>D4 mode (b57=1)</p> <p>D5 mode (b57=0)</p>

Pin No.	Pin name	Pin description	
75	CY <sub>out1</sub> /Y <sub>out1</sub> /V <sub>out1</sub>	<b>Function</b>	
		<p>Color difference signal , Luminance signal or Composite signal output                      It is a terminal for a Color difference or Luminance or Composite signal external output.                      It can be switched with D5 mode or D4 mode.                      D4 mode is lower power than D5 mode.</p> <p>Pin voltage: 2.2V typ. [V, Y] , 4.4V typ. [CY]                      Load resistance min.: 1kΩ                      Stray capacitance max.: 10pF</p>	
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 $C_{OUT} = \frac{1}{2\pi \times f_{CL} \times Z_i}$ <p style="text-align: center;">*f<sub>CL</sub>=1~10Hz</p> <p>When not using it: open</p> <p style="text-align: center;"><b>Output signal</b></p> 	

Pin No.	Pin name	Pin description							
77 78 79	SW3 SW2 SW1	<b>Function</b>							
		<p>The terminal which detects the connection state of D connector.                      A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers &amp; threshold])</p> <p>Threshold: 2.4V typ.                      Input impedance: 160kΩ typ.</p>							
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>						
		<p>When not using it: open</p>							
<b>Input signal</b>									
		<p>DC voltage:                      0V (GND) or OPEN</p> <p>Note:                      When you impress voltage to a terminal, make it less than {6V}.</p>							
81 87 93	DL1-1 DL1-2 DL1-3	<b>Function</b>							
		<p>The terminal which detects the number-of-scanning-lines information on D connector.                      A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers &amp; threshold])</p> <p>Threshold 1: 1.2V typ.                      Threshold 2: 3.1V typ.                      Input impedance: 150kΩ typ.</p>							
		<b>External circuit</b>	<b>Equivalent circuit diagram</b>						
		<p>When not using it: open</p>							
<b>Input signal</b>									
		<p>DC voltage:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </table>		L	0V	M	1.4-2.4V	H	3.5-5V
L	0V								
M	1.4-2.4V								
H	3.5-5V								

Pin No.	Pin name	Pin description							
82 88 94	CY1 CY2 CY3	<p align="center"><b>Function</b></p> <p>Component Y signal input A RGB signal can also be inputted besides a component Y signal.</p> <p>Input bias Pin voltage: 3.2V typ. Input impedance: 100kΩ typ. Input dynamic range: 1.6V<sub>P-P</sub> min.</p>							
		<p align="center"><b>External circuit</b></p>  <p>Component Y signal input</p> <p>When not using it: open</p>	<p align="center"><b>Equivalent circuit diagram</b></p>  <p>Vcc5 (=5V)</p> <p>GND</p>						
		<p align="center"><b>Input signal</b></p>  <p>Component Y 1V signal</p> <p>0.6V Ternary synchronizing signal</p>							
83 89 95	DL2-1 DL2-2 DL2-3	<p align="center"><b>Function</b></p> <p>The terminal which detects the I/P information of D connector. A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers &amp; threshold])</p> <p>Threshold: 3.1V typ. Input impedance: 150kΩ typ.</p>							
		<p align="center"><b>External circuit</b></p>  <p>L2</p> <p>D connector</p> <p>When not using it: open</p>	<p align="center"><b>Equivalent circuit diagram</b></p>  <p>Vcc5 (=5V)</p> <p>GND</p> <p>3.1V</p>						
		<p align="center"><b>Input signal</b></p> <p>DC voltage:</p> <table border="1" data-bbox="545 1751 775 1863"> <thead> <tr> <th></th> <th>L2</th> </tr> </thead> <tbody> <tr> <td>M</td> <td>0V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </tbody> </table>		L2	M	0V	H	3.5-5V	
			L2						
M	0V								
H	3.5-5V								

Pin No.	Pin name	Pin description									
84 90 96	PB1 PB2 PB3	<p align="center"><b>Function</b></p> <p>Color difference signal input A RGB signal can also be inputted besides a color-difference signal.</p> <p>Input bias Pin voltage: 3.2V typ. Input impedance: 100kΩ typ. Input dynamic range: 1.6V<sub>P-P</sub> typ.</p>									
		<p align="center"><b>External circuit</b></p>  <p>Color difference signal input</p> <p>When not using it: open</p>	<p align="center"><b>Equivalent circuit diagram</b></p>  <p>Vcc5 (=5V)</p> <p>GND</p>								
		<p align="center"><b>Input signal</b></p>  <p>Color difference signal</p> <p>0.6V</p> <p>0.7V</p> <p>Ternary synchronizing signal</p>									
85 91 97	DL3-1 DL3-2 DL3-3	<p align="center"><b>Function</b></p> <p>The terminal which detects the aspect ratio information of D connector. A detected result is reflected in a status register. (refer to [Status registers] [Output data of status registers &amp; threshold])</p> <p>Threshold 1: 1.2V typ. Threshold 2: 3.1V typ. Input impedance: 150kΩ typ.</p>									
		<p align="center"><b>External circuit</b></p>  <p>L3</p> <p>D connector</p> <p>When not using it: open</p>	<p align="center"><b>Equivalent circuit diagram</b></p>  <p>Vcc5 (=5V)</p> <p>GND</p> <p>1.2V</p> <p>3.1V</p>								
		<p align="center"><b>Input signal</b></p> <p>DC voltage:</p> <table border="1" data-bbox="550 1747 774 1892"> <thead> <tr> <th></th> <th>L3</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0V</td> </tr> <tr> <td>M</td> <td>1.4-2.4V</td> </tr> <tr> <td>H</td> <td>3.5-5V</td> </tr> </tbody> </table>		L3	L	0V	M	1.4-2.4V	H	3.5-5V	
			L3								
L	0V										
M	1.4-2.4V										
H	3.5-5V										

Pin No.	Pin name	Pin description	
		<b>Function</b>	
		Color difference signal input A RGB signal can also be inputted besides a color-difference signal.  Input bias Pin voltage: 3.2V typ. Input impedance: 100kΩ typ. Input dynamic range: 1.6V <sub>P-P</sub> typ.	
86 92 98	PR1 PR2 PR3	<b>External circuit</b>	<b>Equivalent circuit diagram</b>
		 <p>Color difference signal input</p> <p>When not using it: open</p>	 <p>V<sub>CC5</sub> (-5V)</p> <p>100k</p> <p>GND</p>
		<b>Input signal</b>	
		 <p>Color difference signal</p> <p>0.6V</p> <p>0.7V</p> <p>Ternary synchronizing signal</p>	

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T <sub>STG</sub>	-65~+150	°C
Operating temperature	T <sub>OPR</sub>	-40~+85	°C
Supply voltage 1	V <sub>CC9max.</sub>	-0.2~+10.0	V
Supply voltage 2	V <sub>CC5max.</sub>	-0.2~+6.0	V
Input voltage 1	V <sub>IN1max.</sub>	-0.2~V <sub>CC9</sub> +0.2	V
Input voltage 2	V <sub>IN2max.</sub>	-0.2~V <sub>CC5</sub> +0.2	V
Output voltage 1	V <sub>OUT9max.</sub>	-0.2~V <sub>CC9</sub> +0.2	V
Output voltage 2	V <sub>OUT5max.</sub>	-0.2~V <sub>CC5</sub> +0.2	V
Output current	I <sub>OUTmax.</sub>	25	mA
Junction temperature	T <sub>jmax.</sub>	150	°C
Thermal resistance	θ <sub>j-c</sub>	6.0	°C/W
Allowable loss (*1)	P <sub>d</sub>	3.6	W

Note1: \*1 Board mounting allowable loss. Board size 193×189×1.6mm

**Recommended Operating Conditions**

Item	Symbol	Ratings	Units
Operating temperature	T <sub>OPR</sub>	-40~+85	°C
Operating voltage 1	V <sub>CC9OP</sub>	+8.0~+10.0	V
Operating voltage 2	V <sub>CC5OP</sub>	+4.5~+5.5	V

**Electrical Characteristics** (Except where noted otherwise Ta=25°C, Vcc9=9V, Vcc5=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
<b>Current consumption</b>								
Current consumption	V <sub>CC9</sub> (9V)	I <sub>CC9-0</sub>	[b05, b15, b25, b57, b56, b55, b54=' 0, 0, 0, 0, 0, 0, 0 ']		42	70	98	mA
	V <sub>CC5</sub> (5V)	I <sub>CC5-0</sub>			54	90	126	
<b>All Power save current consumption</b>								
All Power save current consumption	V <sub>CC9</sub> (9V)	I <sub>CC9-0</sub>	[b05, b15, b25, b56, b55, b54=' 1, 1, 1, 1, 1, 1 ']		5	10	15	mA
	V <sub>CC5</sub> (5V)	I <sub>CC5-0</sub>			27	45	63	
<b>Block current consumption</b>								
OUT1 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-V1</sub>	I <sub>CC</sub> [b05=' 0 ']-I <sub>CC</sub> [b05=' 1 ']			30		mA
	V <sub>CC5</sub> (5V)	I <sub>CC5-V1</sub>				8		
OUT2 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-V2</sub>	I <sub>CC</sub> [b15=' 0 ']-I <sub>CC</sub> [b15=' 1 ']			20		mA
	V <sub>CC5</sub> (5V)	I <sub>CC5-V2</sub>				8		
OUT3 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-V3</sub>	I <sub>CC</sub> [b25=' 0 ']-I <sub>CC</sub> [b25=' 1 ']			0		mA
	V <sub>CC5</sub> (5V)	I <sub>CC5-V3</sub>				30		
AUDIO OUT1 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-A1</sub>	I <sub>CC</sub> [b56=' 0 ']-I <sub>CC</sub> [b56=' 1 ']			4		mA
AUDIO OUT2 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-A2</sub>	I <sub>CC</sub> [b55=' 0 ']-I <sub>CC</sub> [b55=' 1 ']			4		mA
AUDIO OUT3 Block current consumption (refer to block diagram)	V <sub>CC9</sub> (9V)	I <sub>CC9-A3</sub>	I <sub>CC</sub> [b54=' 0 ']-I <sub>CC</sub> [b54=' 1 ']			4		mA
Graphics Resolution current consumption	V <sub>CC9</sub> (9V)	I <sub>CC9-GR</sub>	I <sub>CC</sub> [b57=' 0 ']-I <sub>CC</sub> [b57=' 1 ']			10		mA
<b>Input pin voltage</b>								
Input pin voltage 1 (V, Y)	V <sub>IN1</sub>	100, 6, 12, 18, 24, 26, 28, 2, 8, 14, 20 pin			1.4	1.9	2.4	V
Input pin voltage 2 (C, CY, PB, PR)	V <sub>IN2</sub>	4, 10, 16, 22, 82, 84, 86, 88, 90, 92, 94, 96, 98 pin			2.6	3.2	3.8	V
Input pin voltage 3 (L, R)	V <sub>IN3</sub>	41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 pin			3.2	3.8	4.4	V
<b>Output pin voltage (OUT1, 2)</b>								
Output pin voltage 1 (V, Y)	V <sub>OUT1</sub>	70, 71, 74, 75 pin			1.8	2.2	2.6	V
Output pin voltage 2 (C, CY, PB, PR)	V <sub>OUT2</sub>	63, 69, 70, 71, 73, 74, 75 pin			4.0	4.4	4.8	V
<b>Output pin voltage (OUT3, 4, 5)</b>								
Output pin voltage 3 (V, Y)	V <sub>OUT3</sub>	65, 67 pin			0.9	1.3	1.7	V
Output pin voltage 4 (C)	V <sub>OUT4</sub>	63 pin			2.2	2.6	3.0	V
<b>Audio output pin voltage (OUT1, 2, 3)</b>								
Audio output pin voltage (L, R)	V <sub>OUT5</sub>	34, 35, 36, 37, 38, 39 pin			4.1	4.5	4.9	V
<b>S-DCOUT pin output voltage</b>								
S-DC <sub>OUT</sub> pin output voltage	L	V <sub>DCOUTL</sub>	62 pin R <sub>L</sub> =10kΩ+100kΩ		GND	0.1	0.5	V
	M	V <sub>DCOUTM</sub>	62 pin R <sub>L</sub> =10kΩ+100kΩ		1.6	2.1	2.4	V
	H	V <sub>DCOUTH</sub>	62 pin R <sub>L</sub> =10kΩ+100kΩ		4.3	4.6	V <sub>CC5</sub>	V

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>Bias input impedance</b>							
C <sub>IN</sub> input impedance	Z <sub>CIN</sub>	4, 10, 16, 22 pin	70	100	130	kΩ	
CY <sub>IN</sub> input impedance	Z <sub>CYIN</sub>	82, 88, 94 pin	70	100	130	kΩ	
Pb <sub>IN</sub> input impedance	Z <sub>PbIN</sub>	84, 90, 96 pin	70	100	130	kΩ	
Pr <sub>IN</sub> input impedance	Z <sub>PrIN</sub>	86, 92, 98 pin	70	100	130	kΩ	
L <sub>IN</sub> input impedance	Z <sub>LIN</sub>	60, 58, 56, 54, 52, 50, 48, 46, 44, 42 pin	47	60	73	kΩ	
R <sub>IN</sub> input impedance	Z <sub>RIN</sub>	59, 57, 55, 53, 51, 49, 47, 45, 43, 41 pin	47	60	73	kΩ	
<b>V<sub>OUT3</sub> (65pin) electrical characteristics</b>							
V <sub>OUT3</sub> Voltage gain	G <sub>VVOUT3</sub>	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB	
V <sub>OUT3</sub> Frequency characteristic	with filter	f <sub>1VOUT3</sub>	SIN wave: 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>2VOUT3</sub>	SIN wave: 1V 27MHz/100kHz		-33.0	-24.0	dB
V <sub>OUT3</sub> Input dynamic range	DR <sub>VOUT3</sub>	SIN wave: 100kHz THD=1.0%	1.3	1.4		V	
V <sub>OUT3</sub> Group delay	with filter	t <sub>GD VOUT3</sub>	at 100kHz		55	ns	
V <sub>OUT3</sub> Group delay deviation 1	with filter	Δt <sub>1GD VOUT3</sub>	to 3.58MHz		4	20	ns
V <sub>OUT3</sub> Group delay deviation 2	with filter	Δt <sub>2GD VOUT3</sub>	to 4.43MHz		6	20	ns
V <sub>OUT3</sub> Group delay deviation 3	with filter	Δt <sub>3GD VOUT3</sub>	to 6MHz		13	20	ns
V <sub>OUT3</sub> Crosstalk	CT <sub>VOUT3</sub>	SIN wave: 1V f=4.43MHz		-60	-55	dB	
<b>Y<sub>OUT3</sub>/V<sub>OUT4</sub> (67pin) electrical characteristics</b>							
Y <sub>OUT3</sub> Voltage gain	G <sub>VYOUT3</sub>	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB	
Y <sub>OUT3</sub> Frequency characteristic	with filter	f <sub>1YOUT3</sub>	SIN wave: 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>2YOUT3</sub>	SIN wave: 1V 27MHz/100kHz		-33.0	-24.0	dB
Y <sub>OUT3</sub> Input dynamic range	DR <sub>YOUT3</sub>	SIN wave: 100kHz THD=1.0%	1.3	1.4		V	
Y <sub>OUT3</sub> Group delay	with filter	t <sub>GD YOUT3</sub>	at 100kHz		55	ns	
Y <sub>OUT3</sub> Group delay deviation 1	with filter	Δt <sub>1GD YOUT3</sub>	to 3.58MHz		4	20	ns
Y <sub>OUT3</sub> Group delay deviation 2	with filter	Δt <sub>2GD YOUT3</sub>	to 4.43MHz		6	20	ns
Y <sub>OUT3</sub> Group delay deviation 3	with filter	Δt <sub>3GD YOUT3</sub>	to 6MHz		13	20	ns
Y <sub>OUT3</sub> Crosstalk	CT <sub>YOUT3</sub>	SIN wave: 1V f=4.43MHz		-60	-55	dB	
<b>C<sub>OUT3</sub>/V<sub>OUT5</sub> (63pin) electrical characteristics</b>							
C <sub>OUT3</sub> Voltage gain	G <sub>VCOUT3</sub>	SIN wave: 1V f=100kHz	5.7	6.0	6.3	dB	
C <sub>OUT3</sub> Frequency characteristic	with filter	f <sub>1COUT3</sub>	SIN wave: 1V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>2COUT3</sub>	SIN wave: 1V 27MHz/100kHz		-33.0	-24.0	dB
C <sub>OUT3</sub> Input dynamic range	DR <sub>COUT3</sub>	SIN wave: 100kHz THD=1.0%	1.3	1.4		V	
C <sub>OUT3</sub> Group delay	with filter	t <sub>GD COUT3</sub>	at 100kHz		55	ns	
C <sub>OUT3</sub> Group delay deviation 1	with filter	Δt <sub>1GD COUT3</sub>	to 3.58MHz		4	20	ns
C <sub>OUT3</sub> Group delay deviation 2	with filter	Δt <sub>2GD COUT3</sub>	to 4.43MHz		6	20	ns
C <sub>OUT3</sub> Group delay deviation 3	with filter	Δt <sub>3GD COUT3</sub>	to 6MHz		13	20	ns
C <sub>OUT3</sub> Crosstalk	CT <sub>COUT3</sub>	SIN wave: 1V f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>CY<sub>OUT1</sub> (75pin) electrical characteristics</b>							
<b>CY<sub>OUT1</sub> Voltage gain</b>	G <sub>V</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>CY<sub>OUT1</sub> Frequency characteristic peak</b>	f <sub>peak</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB	
<b>CY<sub>OUT1</sub> Frequency characteristic</b>	without filter	f <sub>1</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 100MHz/100kHz	-4.0	-3.0	-2.0	dB
	with filter1	f <sub>11</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>12</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	with filter2	f <sub>21</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f <sub>22</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	with filter3	f <sub>31</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f <sub>32</sub> CY <sub>OUT1</sub>	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>CY<sub>OUT1</sub> Input dynamic range</b>	DR <sub>CY<sub>OUT1</sub></sub>	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>CY<sub>OUT1</sub> Group delay</b>	with filter1	t <sub>1GD</sub> CY <sub>OUT1</sub>	at 100kHz		30	ns	
	with filter2	t <sub>2GD</sub> CY <sub>OUT1</sub>	at 100kHz		25	ns	
	with filter3	t <sub>3GD</sub> CY <sub>OUT1</sub>	at 100kHz		25	ns	
CY <sub>OUT1</sub> Group delay deviation 11	with filter1	Δt <sub>11GD</sub> CY <sub>OUT1</sub>	to 3.58MHz		4	20	ns
CY <sub>OUT1</sub> Group delay deviation 12		Δt <sub>12GD</sub> CY <sub>OUT1</sub>	to 4.43MHz		6	20	ns
CY <sub>OUT1</sub> Group delay deviation 13		Δt <sub>13GD</sub> CY <sub>OUT1</sub>	to 6MHz		12	20	ns
CY <sub>OUT1</sub> Group delay deviation 21	with filter2	Δt <sub>21GD</sub> CY <sub>OUT1</sub>	to 3.58MHz		3	20	ns
CY <sub>OUT1</sub> Group delay deviation 22		Δt <sub>22GD</sub> CY <sub>OUT1</sub>	to 4.43MHz		5	20	ns
CY <sub>OUT1</sub> Group delay deviation 23		Δt <sub>23GD</sub> CY <sub>OUT1</sub>	to 12MHz		8	20	ns
CY <sub>OUT1</sub> Group delay deviation 31	with filter3	Δt <sub>31GD</sub> CY <sub>OUT1</sub>	to 3.58MHz		1	20	ns
CY <sub>OUT1</sub> Group delay deviation 32		Δt <sub>32GD</sub> CY <sub>OUT1</sub>	to 4.43MHz		1	20	ns
CY <sub>OUT1</sub> Group delay deviation 33		Δt <sub>33GD</sub> CY <sub>OUT1</sub>	to 21MHz		5	20	ns
<b>CY<sub>OUT1</sub> Crosstalk</b>	CT <sub>CY<sub>OUT1</sub></sub>	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	
<b>P<sub>OUT1</sub> (74pin) electrical characteristics</b>							
<b>P<sub>OUT1</sub> Voltage gain</b>	G <sub>V</sub> P <sub>OUT1</sub>	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>P<sub>OUT1</sub> Frequency characteristic peak</b>	f <sub>peak</sub> P <sub>OUT1</sub>	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB	
<b>P<sub>OUT1</sub> Frequency characteristic</b>	without filter	f <sub>1</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 100MHz/100kHz	-4.0	-3.0	-2.0	dB
	with filter1	f <sub>11</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>12</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	with filter2	f <sub>21</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f <sub>22</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	with filter3	f <sub>31</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f <sub>32</sub> P <sub>OUT1</sub>	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>P<sub>OUT1</sub> Input dynamic range</b>	DR <sub>P<sub>OUT1</sub></sub>	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>P<sub>OUT1</sub> Group delay</b>	with filter1	t <sub>1GD</sub> P <sub>OUT1</sub>	at 100kHz		30	ns	
	with filter2	t <sub>2GD</sub> P <sub>OUT1</sub>	at 100kHz		25	ns	
	with filter3	t <sub>3GD</sub> P <sub>OUT1</sub>	at 100kHz		25	ns	
P <sub>OUT1</sub> Group delay deviation 11	with filter1	Δt <sub>11GD</sub> P <sub>OUT1</sub>	to 3.58MHz		4	20	ns
P <sub>OUT1</sub> Group delay deviation 12		Δt <sub>12GD</sub> P <sub>OUT1</sub>	to 4.43MHz		6	20	ns
P <sub>OUT1</sub> Group delay deviation 13		Δt <sub>13GD</sub> P <sub>OUT1</sub>	to 6MHz		12	20	ns
P <sub>OUT1</sub> Group delay deviation 21	with filter2	Δt <sub>21GD</sub> P <sub>OUT1</sub>	to 3.58MHz		3	20	ns
P <sub>OUT1</sub> Group delay deviation 22		Δt <sub>22GD</sub> P <sub>OUT1</sub>	to 4.43MHz		5	20	ns
P <sub>OUT1</sub> Group delay deviation 23		Δt <sub>23GD</sub> P <sub>OUT1</sub>	to 12MHz		8	20	ns
P <sub>OUT1</sub> Group delay deviation 31	with filter3	Δt <sub>31GD</sub> P <sub>OUT1</sub>	to 3.58MHz		1	20	ns
P <sub>OUT1</sub> Group delay deviation 32		Δt <sub>32GD</sub> P <sub>OUT1</sub>	to 4.43MHz		1	20	ns
P <sub>OUT1</sub> Group delay deviation 33		Δt <sub>33GD</sub> P <sub>OUT1</sub>	to 21MHz		5	20	ns
<b>P<sub>OUT1</sub> Crosstalk</b>	CT <sub>P<sub>OUT1</sub></sub>	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>PrOUT1 (73pin) electrical characteristics</b>							
<b>PrOUT1 Voltage gain</b>	G <sub>VPrOUT1</sub>	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>PrOUT1 Frequency characteristic peak</b>	f <sub>peakPrOUT1</sub>	SIN wave: 0.7V f=100kHz~100MHz	0.0	0.5	1.0	dB	
<b>PrOUT1 Frequency characteristic</b>	without filter	f <sub>1PrOUT1</sub>	SIN wave: 0.7V 100MHz/100kHz	-4.0	-3.0	-2.0	dB
	<b>With filter1</b>	f <sub>11PrOUT1</sub>	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>12PrOUT1</sub>	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	<b>with filter2</b>	f <sub>21PrOUT1</sub>	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f <sub>22PrOUT1</sub>	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	<b>with filter3</b>	f <sub>31PrOUT1</sub>	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f <sub>32PrOUT1</sub>	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>PrOUT1 Input dynamic range</b>	DR <sub>PrOUT1</sub>	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>PrOUT1 Crosstalk</b>	CT <sub>PrOUT1</sub>	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	
<b>PrOUT1 Group delay</b>	<b>with filter1</b>	t <sub>1GD PrOUT1</sub>	at 100kHz		30	ns	
	<b>with filter2</b>	t <sub>2GD PrOUT1</sub>	at 100kHz		25	ns	
	<b>with filter3</b>	t <sub>3GD PrOUT1</sub>	at 100kHz		25	ns	
<b>PrOUT1 Group delay deviation 11</b>	<b>with filter1</b>	Δt <sub>11GD PrOUT1</sub>	to 3.58MHz		4	20	ns
<b>PrOUT1 Group delay deviation 12</b>		Δt <sub>12GD PrOUT1</sub>	to 4.43MHz		6	20	ns
<b>PrOUT1 Group delay deviation 13</b>		Δt <sub>13GD PrOUT1</sub>	to 6MHz		12	20	ns
<b>PrOUT1 Group delay deviation 21</b>	<b>with filter2</b>	Δt <sub>21GD PrOUT1</sub>	to 3.58MHz		3	20	ns
<b>PrOUT1 Group delay deviation 22</b>		Δt <sub>22GD PrOUT1</sub>	to 4.43MHz		5	20	ns
<b>PrOUT1 Group delay deviation 23</b>		Δt <sub>23GD PrOUT1</sub>	to 12MHz		8	20	ns
<b>PrOUT1 Group delay deviation 31</b>	<b>with filter3</b>	Δt <sub>31GD PrOUT1</sub>	to 3.58MHz		1	20	ns
<b>PrOUT1 Group delay deviation 32</b>		Δt <sub>32GD PrOUT1</sub>	to 4.43MHz		1	20	ns
<b>PrOUT1 Group delay deviation 33</b>		Δt <sub>33GD PrOUT1</sub>	to 21MHz		5	20	ns
<b>Group delay deviation between each channels</b>							
<b>Group delay deviation between C and Y</b>	Δt <sub>1chGD</sub>	between C and Y at 3.58MHz		0	10	ns	
<b>Group delay deviation between CY and Pb (Pr)</b>	Δt <sub>2chGD</sub>	between CY and Pb (Pr) at 8MHz		0	10	ns	

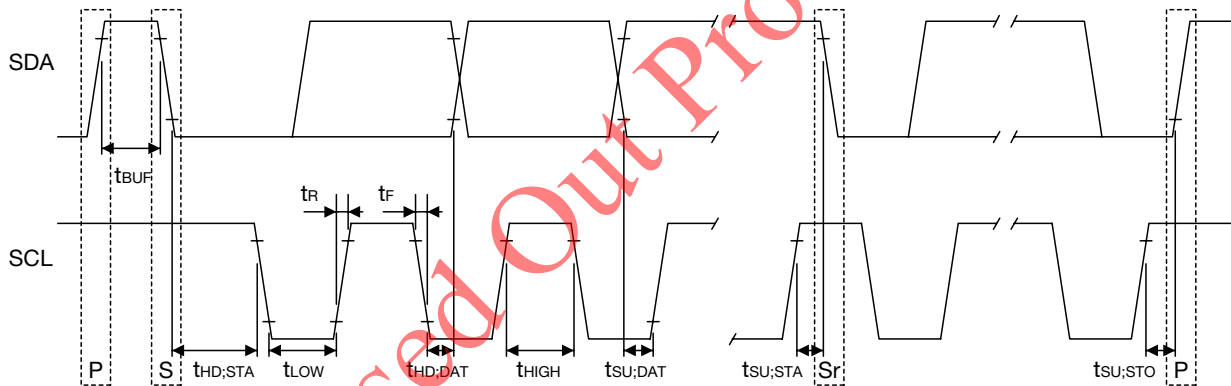
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>CY<sub>OUT2</sub> (71pin) electrical characteristics</b>							
<b>CY<sub>OUT2</sub> Voltage gain</b>	G <sub>VCYOUT2</sub>	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>CY<sub>OUT2</sub> Frequency characteristic peak</b>	f <sub>peakCYOUT2</sub>	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB	
<b>CY<sub>OUT2</sub> Frequency characteristic</b>	without filter	f <sub>1CYOUT2</sub>	SIN wave: 0.7V 50MHz/100kHz	-3.0	-1.0	0.0	dB
	with filter1	f <sub>11CYOUT2</sub>	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>12CYOUT2</sub>	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	with filter2	f <sub>21CYOUT2</sub>	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f <sub>22CYOUT2</sub>	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	with filter3	f <sub>31CYOUT2</sub>	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f <sub>32CYOUT2</sub>	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>CY<sub>OUT2</sub> Input dynamic range</b>	DR <sub>CYOUT2</sub>	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>CY<sub>OUT2</sub> Group delay</b>	with filter1	t <sub>1GD CYOUT2</sub>	at 100kHz		30		ns
	With filter2	t <sub>2GD CYOUT2</sub>	at 100kHz		25		ns
	With filter3	t <sub>3GD CYOUT2</sub>	at 100kHz		25		ns
CY <sub>OUT2</sub> Group delay deviation 11	with filter1	Δt <sub>11GD CYOUT2</sub>	to 3.58MHz		4	20	ns
CY <sub>OUT2</sub> Group delay deviation 12		Δt <sub>12GD CYOUT2</sub>	to 4.43MHz		6	20	ns
CY <sub>OUT2</sub> Group delay deviation 13		Δt <sub>13GD CYOUT2</sub>	to 6MHz		12	20	ns
CY <sub>OUT2</sub> Group delay deviation 21	with filter2	Δt <sub>21GD CYOUT2</sub>	to 3.58MHz		3	20	ns
CY <sub>OUT2</sub> Group delay deviation 22		Δt <sub>22GD CYOUT2</sub>	to 4.43MHz		5	20	ns
CY <sub>OUT2</sub> Group delay deviation 23		Δt <sub>23GD CYOUT2</sub>	to 12MHz		8	20	ns
CY <sub>OUT2</sub> Group delay deviation 31	with filter3	Δt <sub>31GD CYOUT2</sub>	to 3.58MHz		1	20	ns
CY <sub>OUT2</sub> Group delay deviation 32		Δt <sub>32GD CYOUT2</sub>	to 4.43MHz		1	20	ns
CY <sub>OUT2</sub> Group delay deviation 33		Δt <sub>33GD CYOUT2</sub>	to 21MHz		5	20	ns
<b>CY<sub>OUT2</sub> Crosstalk</b>	CT <sub>CYOUT2</sub>	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	
<b>Pb<sub>OUT2</sub> (70pin) electrical characteristics</b>							
<b>Pb<sub>OUT2</sub> Voltage gain</b>	G <sub>VPbOUT2</sub>	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>Pb<sub>OUT2</sub> Frequency characteristic peak</b>	f <sub>peakPbOUT2</sub>	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB	
<b>Pb<sub>OUT2</sub> Frequency characteristic</b>	without filter	f <sub>1PbOUT2</sub>	SIN wave: 0.7V 50MHz/100kHz	-3.0	-1.0	0.0	dB
	With filter1	f <sub>11PbOUT2</sub>	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f <sub>12PbOUT2</sub>	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	with filter2	f <sub>21PbOUT2</sub>	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f <sub>22PbOUT2</sub>	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	with filter3	f <sub>31PbOUT2</sub>	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f <sub>32PbOUT2</sub>	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>Pb<sub>OUT2</sub> Input dynamic range</b>	DR <sub>PbOUT2</sub>	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>Pb<sub>OUT2</sub> Group delay</b>	with filter1	t <sub>1GD PbOUT2</sub>	at 100kHz		30		ns
	with filter2	t <sub>2GD PbOUT2</sub>	at 100kHz		25		ns
	with filter3	t <sub>3GD PbOUT2</sub>	at 100kHz		25		ns
Pb <sub>OUT2</sub> Group delay deviation 11	with filter1	Δt <sub>11GD PbOUT2</sub>	to 3.58MHz		4	20	ns
Pb <sub>OUT2</sub> Group delay deviation 12		Δt <sub>12GD PbOUT2</sub>	to 4.43MHz		6	20	ns
Pb <sub>OUT2</sub> Group delay deviation 13		Δt <sub>13GD PbOUT2</sub>	to 6MHz		12	20	ns
Pb <sub>OUT2</sub> Group delay deviation 21	with filter2	Δt <sub>21GD PbOUT2</sub>	to 3.58MHz		3	20	ns
Pb <sub>OUT2</sub> Group delay deviation 22		Δt <sub>22GD PbOUT2</sub>	to 4.43MHz		5	20	ns
Pb <sub>OUT2</sub> Group delay deviation 23		Δt <sub>23GD PbOUT2</sub>	to 12MHz		8	20	ns
Pb <sub>OUT2</sub> Group delay deviation 31	with filter3	Δt <sub>31GD PbOUT2</sub>	to 3.58MHz		1	20	ns
Pb <sub>OUT2</sub> Group delay deviation 32		Δt <sub>32GD PbOUT2</sub>	to 4.43MHz		1	20	ns
Pb <sub>OUT2</sub> Group delay deviation 33		Δt <sub>33GD PbOUT2</sub>	to 21MHz		5	20	ns
<b>Pb<sub>OUT2</sub> Crosstalk</b>	CT <sub>PbOUT2</sub>	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>PrOUT2 (69pin) electrical characteristics</b>							
<b>PrOUT2 Voltage gain</b>	GvPrOUT2	SIN wave: 0.7V f=100kHz	-0.3	0.0	0.3	dB	
<b>PrOUT2 Frequency characteristicJ peak</b>	fpeakPrOUT2	SIN wave: 0.7V f=100kHz~50MHz	0.0	0.5	1.0	dB	
<b>PrOUT2 Frequency characteristic</b>	without filter	f1PrOUT2	SIN wave: 0.7V 50MHz/100kHz	-3.0	-1.0	0.0	dB
	<b>With filter1</b>	f11PrOUT2	SIN wave: 0.7V 6.75MHz/100kHz	-1.0	0.0	1.0	dB
		f12PrOUT2	SIN wave: 0.7V 27MHz/100kHz		-33.0	-24.0	dB
	<b>with filter2</b>	f21PrOUT2	SIN wave: 0.7V 13.5MHz/100kHz	-5.0	-3.0	-2.0	dB
		f22PrOUT2	SIN wave: 0.7V 54MHz/100kHz		-33.0	-24.0	dB
	<b>with filter3</b>	f31PrOUT2	SIN wave: 0.7V 24MHz/100kHz	-5.0	-3.0	1.0	dB
	f32PrOUT2	SIN wave: 0.7V 96MHz/100kHz		-33.0	-24.0	dB	
<b>PrOUT2 Input dynamic range</b>	DRPrOUT2	SIN wave: 100kHz THD=1.0%	1.6	2.0		V	
<b>PrOUT2 Crosstalk</b>	CTPrOUT2	SIN wave: 0.7V f=4.43MHz		-60	-55	dB	
<b>PrOUT2 Group delay</b>	<b>with filter1</b>	t1GD PrOUT2	at 100kHz		30		ns
	<b>with filter2</b>	t2GD PrOUT2	at 100kHz		25		ns
	<b>with filter3</b>	t3GD PrOUT2	at 100kHz		25		ns
<b>PrOUT2 Group delay deviation 11</b>	<b>with filter1</b>	$\Delta t11GD PrOUT2$	to 3.58MHz		4	20	ns
<b>PrOUT2 Group delay deviation 12</b>		$\Delta t12GD PrOUT2$	to 4.43MHz		6	20	ns
<b>PrOUT2 Group delay deviation 13</b>		$\Delta t13GD PrOUT2$	to 6MHz		12	20	ns
<b>PrOUT2 Group delay deviation 21</b>	<b>with filter2</b>	$\Delta t21GD PrOUT2$	to 3.58MHz		3	20	ns
<b>PrOUT2 Group delay deviation 22</b>		$\Delta t22GD PrOUT2$	to 4.43MHz		5	20	ns
<b>PrOUT2 Group delay deviation 23</b>		$\Delta t23GD PrOUT2$	to 12MHz		8	20	ns
<b>PrOUT2 Group delay deviation 31</b>	<b>with filter3</b>	$\Delta t31GD PrOUT2$	to 3.58MHz		1	20	ns
<b>PrOUT2 Group delay deviation 32</b>		$\Delta t32GD PrOUT2$	to 4.43MHz		1	20	ns
<b>PrOUT2 Group delay deviation 33</b>		$\Delta t33GD PrOUT2$	to 21MHz		5	20	ns
<b>Group delay deviation between each channels</b>							
<b>Group delay deviation between C and Y</b>	$\Delta t1chGD$	between C and Y at 3.58MHz		0	10	ns	
<b>Group delay deviation between CY and Pb (Pr)</b>	$\Delta t2chGD$	between CY and Pb (Pr) at 8MHz		0	10	ns	
<b>L, ROUT (34~39pin) electrical characteristics</b>							
<b>L, ROUT Voltage gain</b>	<b>0dB</b>	Gv1L, ROUT	SIN wave: 1Vrms f=1kHz	-0.3	0.0	0.3	dB
	<b>6dB</b>	Gv2L, ROUT	SIN wave: 1Vrms f=1kHz	5.7	6.0	6.3	dB
<b>L, ROUT Frequency characteristic</b>	<b>0dB</b>	f1L, ROUT	SIN wave: 1Vrms f=50kHz	-3.0			dB
	<b>6dB</b>	f2L, ROUT	SIN wave: 1Vrms f=50kHz	-3.0			dB
<b>Total harmonic distortion</b>	THD	SIN wave: 1Vrms f=1kHz, Gv=0dB		0.03	0.05	%	
<b>Input dynamic range</b>	DR	f=1kHz, THD=0.5% Gv=0dB	2.8	3.0		Vrms	
<b>Crosstalk</b>	CT	SIN wave: 1Vrms f=1kHz		-90	-80	dB	
<b>Ripple rejection</b>	PSRR	Vcc=9V+0.1Vrms (SIN wave) at 100Hz		-50	-40	dB	
<b>Output offset voltage</b>	V <sub>OFF1</sub>	DC offset at the switching time, Gv=0dB	-15	0	15	mV	
	V <sub>OFF2</sub>	DC offset at the switching time, Gv=6dB	-30	0	30	mV	
<b>S/N ratio</b>	S/N1	1kHz, A curve, 1Vrms Gv=0dB		-90	-80	dB	
	S/N2	1kHz, A curve, 1Vrms Gv=6dB		-80	-70	dB	
<b>O1 (5pin) electrical characteristics</b>							
<b>O1 pin low level output voltage</b>	V <sub>O1</sub>	O1 pin sink 5mA	GND		0.4	V	
<b>O1 pin Leak current (at the time of OFF)</b>	I <sub>O1</sub>		-10		10	μA	
<b>O2 (17pin) electrical characteristics</b>							
<b>O2 pin low level output voltage</b>	V <sub>O2</sub>	O2 pin sink 5mA	GND		0.4	V	
<b>O2 pin Leak current (at the time of OFF)</b>	I <sub>O2</sub>		-10		10	μA	

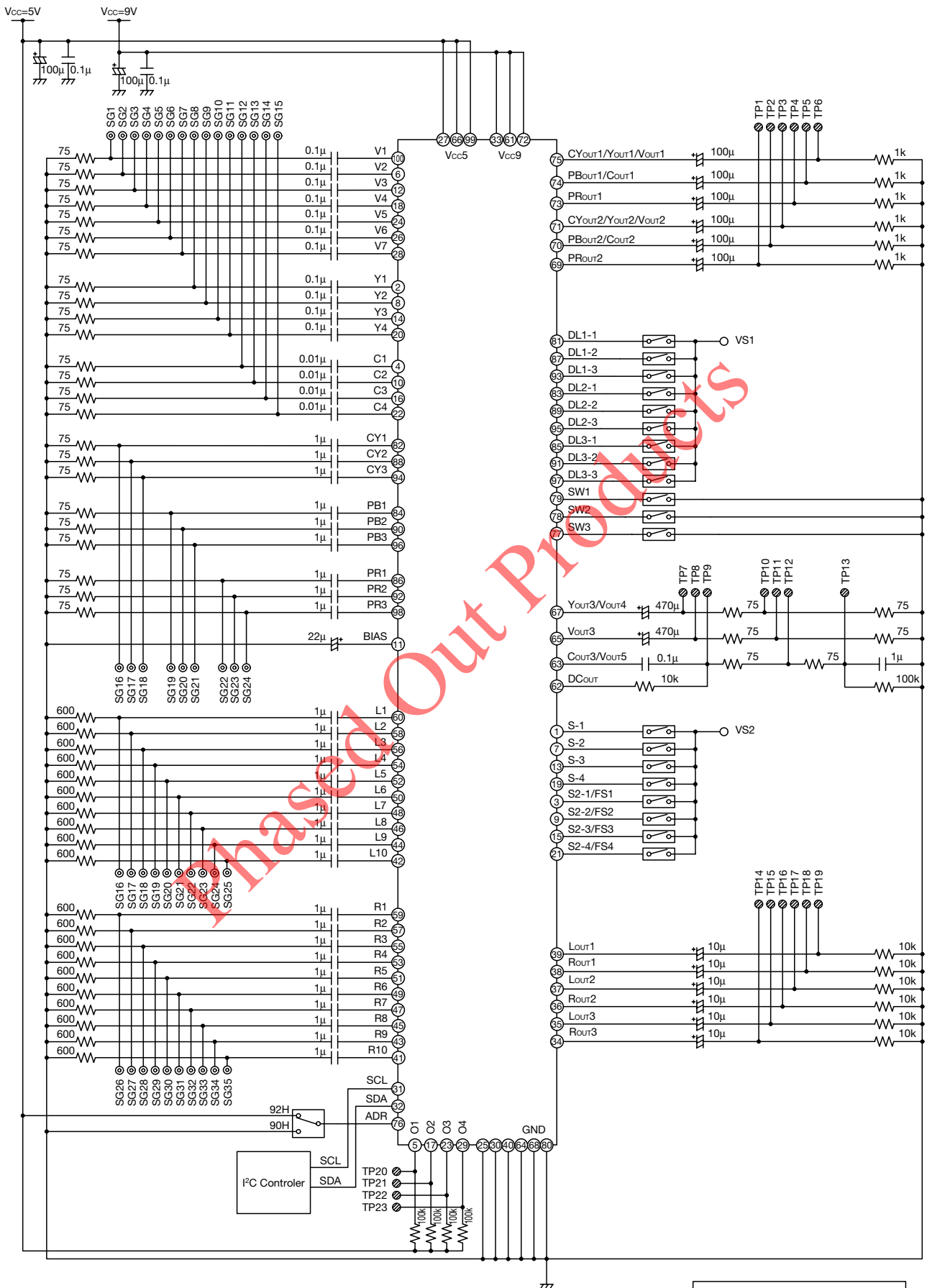
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	
<b>O3 (23pin) electrical characteristics</b>							
O3 pin low level output voltage	V <sub>O3</sub>	O3 pin sink 5mA	GND		0.4	V	
O3 pin Leak current (at the time of OFF)	I <sub>O3</sub>		-10		10	μA	
<b>O4 (29pin) electrical characteristics</b>							
O4 pin low level output voltage	V <sub>O4</sub>	O4 pin sink 5mA	GND		0.4	V	
O4 pin Leak current (at the time of OFF)	I <sub>O4</sub>		-10		10	μA	
<b>DL1 (81, 87, 93pin) electrical characteristics</b>							
DL1 Input voltage 1	Low	V <sub>1L DL1</sub>	GND		1.0	V	
	Middle	V <sub>1M DL1</sub>	1.3		2.7	V	
	High	V <sub>1H DL1</sub>	3.5		V <sub>cc5</sub>	V	
<b>DL2 (83, 89, 95pin) electrical characteristics</b>							
DL2 Input voltage	Low	V <sub>L DL2</sub>	GND		2.7	V	
	High	V <sub>H DL2</sub>	3.5		V <sub>cc5</sub>	V	
<b>DL3 (85, 91, 97pin) electrical characteristics</b>							
DL3 Input voltage	Low	V <sub>L DL3</sub>	GND		1.0	V	
	Middle	V <sub>M DL3</sub>	1.3		2.7	V	
	High	V <sub>H DL3</sub>	3.5		V <sub>cc5</sub>	V	
<b>SW (79, 78, 77pin) electrical characteristics</b>							
SW Input voltage	Low	V <sub>L SW</sub>	GND		2.0	V	
	High	V <sub>H SW</sub>	3.0		V <sub>cc5</sub>	V	
SW output current at terminal voltage Low	I <sub>SW</sub>		19	27	35	μA	
<b>S2/FS (3, 9, 15, 21pin) electrical characteristics</b>							
S2/FS Input voltage 1	Low	V <sub>1L S2/FS</sub>	S, D-Detect Mode		GND	1.0	V
	Middle	V <sub>1M S2/FS</sub>			1.3	2.7	V
	High	V <sub>1H S2/FS</sub>			3.5	V <sub>cc5</sub>	V
S2/FS Input voltage 2	Low	V <sub>2L S2/FS</sub>	FS-Detect Mode		GND	1.0	V
	Middle	V <sub>2M S2/FS</sub>			1.5	3.0	V
	High	V <sub>2H S2/FS</sub>			3.5	V <sub>cc5</sub>	V
<b>S (1, 7, 13, 19pin) electrical characteristics</b>							
S Input voltage	Low	V <sub>L S1</sub>	GND		2.0	V	
	High	V <sub>H S1</sub>	3.0		V <sub>cc5</sub>	V	
S output current at terminal voltage Low	I <sub>S1</sub>		19	27	35	μA	
<b>ADR (76pin) electrical characteristics</b>							
ADR Input voltage	Low	V <sub>L ADR</sub>	90H select		GND	0.8	V
	High	V <sub>H ADR</sub>	92H select		2.5	V <sub>cc5</sub>	V
ADR input current at terminal voltage High	I <sub>ADR</sub>		50	70	90	μA	

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I <sup>2</sup> C condition						
Input voltage L	V <sub>IL</sub>		GND		0.8	V
Input voltage H	V <sub>IH</sub>		2.2		V <sub>CC5</sub>	V
SDA low level output voltage	V <sub>OL</sub>	SDA sink 3mA	GND		0.4	V
High level input current	I <sub>IH</sub>	SDA, SCL=4.5V	-10		10	μA
Low level input current	I <sub>IL</sub>	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f <sub>SCL</sub>				100	kHz
Data transfer wait time	t <sub>BUF</sub>		4.7			μs
SCL start hold time	t <sub>HD;STA</sub>		4.0			μs
SCL low level hold time	t <sub>LOW</sub>		4.7			μs
SCL high level hold time	t <sub>HIGH</sub>		4.0			μs
Start condition setup time	t <sub>SU;STA</sub>		4.7			μs
SDA data hold time	t <sub>HD;DAT</sub>		0			μs
SDA data setup time	t <sub>SU;DAT</sub>		250			ns
SDA, SCL rise time	t <sub>r</sub>				1000	ns
SDA, SCL fall time	t <sub>f</sub>				300	ns
Stop condition setup time	t <sub>SU;STO</sub>		4.0			μs

Note: I<sup>2</sup>C condition

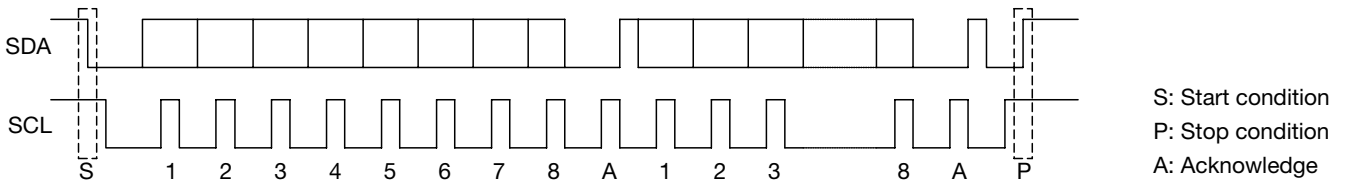


Measuring Circuit



\* Ⓞ SG ... Signal input  
 Ⓞ TP ... Test point  
 ○ VS ... Voltage supply

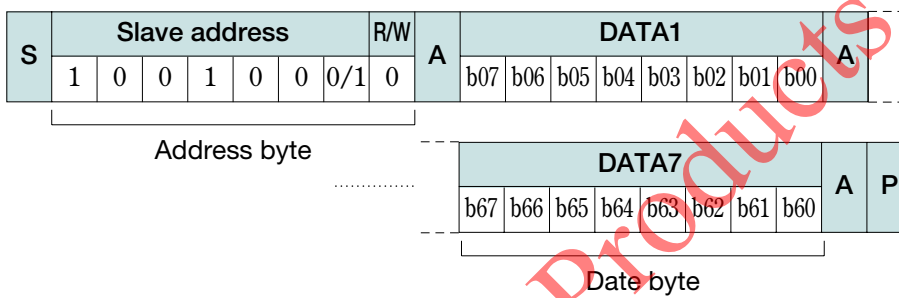
I<sup>2</sup>C BUS



I<sup>2</sup>C BUS is inter IC bus system controlled by 2 lines (SDA, SCL). Data is transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start conditions.

[Control registers]

Control register is data sent from the master for determining the switch conditions. The data format is set as shown in the following figure.



Out of the Address byte, first 7bits are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 0 when data is used control register. As MM1783 slave address, either 90H or 92H can be selected according to the ADR terminal conditions. When ADR terminal is L, 90H is selected.

The following figure indicates the control contents of control registers and switches. Each bit of control registers is reset to 0, when the device is turned on.

MM1783 consists of one address byte and 7 control data bytes (8bytes in total). All data over the limited length (9th and subsequent bytes) is fully neglected. For details of the control contents of switches, refer to the another table.

The reset circuit in the MM1783 is configured with a 5V power supply. The threshold voltage to operate the reset function is 2.5V±0.5V.

Even if a 9V power supply and 5V power supply are independently blacked out as a power sequence, I<sup>2</sup>C control is properly performed after power is recovered.

Table of control registers

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	OUT1 LPF select		OUT1 power save		OUT1 line select			
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
	OUT2 LPF select		OUT2 power save		OUT2 line select			
DATA3 [00H]	b27	b26	b25	b24	b23	b22	b21	b20
	DC <sub>OUT</sub> voltage		OUT3-5 power save	OUT3 separate	OUT3 line select			
DATA4 [00H]	b37	b36	b35	b34	b33	b32	b31	b30
	Audio OUT1 line select				Audio OUT2 line select			
DATA5 [00H]	b47	b46	b45	b44	b43	b42	b41	b40
		AO1 GAIN SW	AO2 GAIN SW	AO3 GAIN SW	Audio OUT3 line select			
DATA6 [00H]	b57	b56	b55	b54	b53	b52	b51	b50
	OUT1 graphics resolution	AO1 power save	AO2 power save	AO3 power save	O1	O2	O3	O4
DATA7 [00H]	b67	b66	b65	b64	b63	b62	b61	b60
	OUT4 line select				OUT5 line select			

\*: [00H] is in the initial state of control registers.

■ Details of contents of control-1

OUT1 line select

b03	b02	b01	b00	CY <sub>OUT1</sub> (75pin)	Pb <sub>OUT1</sub> (74pin)	Pr <sub>OUT1</sub> (73pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V1	Mute	Mute
0	0	1	0	V2	Mute	Mute
0	0	1	1	V3	Mute	Mute
0	1	0	0	V4	Mute	Mute
0	1	0	1	V5	Mute	Mute
0	1	1	0	V6	Mute	Mute
0	1	1	1	V7	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

OUT2 line select

b13	b12	b11	b10	CY <sub>OUT2</sub> (71pin)	Pb <sub>OUT2</sub> (70pin)	Pr <sub>OUT2</sub> (69pin)
0	0	0	0	Mute	Mute	Mute
0	0	0	1	V1	Mute	Mute
0	0	1	0	V2	Mute	Mute
0	0	1	1	V3	Mute	Mute
0	1	0	0	V4	Mute	Mute
0	1	0	1	V5	Mute	Mute
0	1	1	0	V6	Mute	Mute
0	1	1	1	V7	Mute	Mute
1	0	0	0	Y1	C1	Mute
1	0	0	1	Y2	C2	Mute
1	0	1	0	Y3	C3	Mute
1	0	1	1	Y4	C4	Mute
1	1	0	0	CY1	PB1	PR1
1	1	0	1	CY2	PB2	PR2
1	1	1	0	CY3	PB3	PR3
1	1	1	1	Mute	Mute	Mute

■ Details of contents of control-2

OUT3 line select (OUT3 Separator SW OFF [b24=0]) \*1

b24	b23	b22	b21	b20	V <sub>OUT3</sub> (65pin)	Y <sub>OUT3</sub> (67pin)	C <sub>OUT3</sub> (63pin)
0	0	0	0	0	Mute	Mute	Mute
0	0	0	0	1	Y1+C1	Y1	C1
0	0	0	1	0	Y2+C2	Y2	C2
0	0	0	1	1	Y3+C3	Y3	C3
0	0	1	0	0	Y4+C4	Y4	C4
0	0	1	0	1	Mute	Mute	Mute
0	0	1	1	0	Mute	Mute	Mute
0	0	1	1	1	Mute	Mute	Mute
0	1	0	0	0	Mute	Mute	Mute
0	1	0	0	1	V1	Mute	Mute
0	1	0	1	0	V2	Mute	Mute
0	1	0	1	1	V3	Mute	Mute
0	1	1	0	0	V4	Mute	Mute
0	1	1	0	1	V5	Mute	Mute
0	1	1	1	0	V6	Mute	Mute
0	1	1	1	1	V7	Mute	Mute

OUT4 line select (OUT3 Separator SW ON [b24=1]) \*1

b24	b67	b66	b65	b64	V <sub>OUT3</sub> (65pin)	Y <sub>OUT3</sub> (67pin)	C <sub>OUT3</sub> (63pin)
1	0	0	0	0	Regardless of b24, It is controlled by the b23-b20. Refer to the upper table.	Mute	It is controlled by the b63-b60 at the time of b24=1. Refer to following table.
1	0	0	0	1		Y1+C1	
1	0	0	1	0		Y2+C2	
1	0	0	1	1		Y3+C3	
1	0	1	0	0		Y4+C4	
1	0	1	0	1		Mute	
1	0	1	1	0		Mute	
1	0	1	1	1		Mute	
1	1	0	0	0		Mute	
1	1	0	0	1		V1	
1	1	0	1	0		V2	
1	1	0	1	1		V3	
1	1	1	0	0		V4	
1	1	1	0	1		V5	
1	1	1	1	0		V6	
1	1	1	1	1		V7	

OUT5 line select (OUT3 Separator SW ON [b24=1]) \*1

b24	b63	b62	b61	b60	V <sub>OUT3</sub> (65pin)	Y <sub>OUT3</sub> (67pin)	C <sub>OUT3</sub> (63pin)
1	0	0	0	0	Regardless of b24, It is controlled by the b23-b20. Refer to the upper table.	It is controlled by the b67-b64 at the time of b24=1. Refer to the upper table.	Mute
1	0	0	0	1			Y1+C1
1	0	0	1	0			Y2+C2
1	0	0	1	1			Y3+C3
1	0	1	0	0			Y4+C4
1	0	1	0	1			Mute
1	0	1	1	0			Mute
1	0	1	1	1			Mute
1	1	0	0	0			Mute
1	1	0	0	1			V1
1	1	0	1	0			V2
1	1	0	1	1			V3
1	1	1	0	0			V4
1	1	1	0	1			V5
1	1	1	1	0			V6
1	1	1	1	1			V7

\*1: When DC<sub>OUT</sub> is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

■ Details of contents of control-3

LPF cutoff frequency select

OUT1 (73, 74, 75pin)

b07	b06	LPF fc
0	0	through
0	1	24.0MHz
1	0	13.5MHz
1	1	6.75MHz

OUT2 (69, 70, 71pin)

b17	b16	LPF fc
0	0	through
0	1	24.0MHz
1	0	13.5MHz
1	1	6.75MHz

Powersave

OUT1 (73, 74, 75pin)

b05	Conditions
0	Active
1	Powersave

OUT2 (69, 70, 71pin)

b15	Conditions
0	Active
1	Powersave

OUT3 (63, 65, 67pin)

b25	Conditions
0	Active
1	Powersave

Output PORT control

O1 (5pin)

b53	Conditions
0	Low
1	Open

O2 (17pin)

b52	Conditions
0	Low
1	Open

O3 (23pin)

b51	Conditions
0	Low
1	Open

O4 (29pin)

b50	Conditions
0	Low
1	Open

DC<sub>OUT</sub> (62pin) output voltage

b27	b26	Voltage
0	0	0V
0	1	2.2V
1	0	5V
1	1	Hi-Impedance *

\*: When DC<sub>OUT</sub> is set to Hi-Impedance mode, OUT3 is automatically set to Mute mode.

Graphics resolution

OUT1 (73, 74, 75pin)

b57	Conditions
0	D5
1	D4

■ Details of contents of control-4

Audio OUT1 line select

b37	b36	b35	b34	L <sub>OUT1</sub> (39pin)	R <sub>OUT1</sub> (38pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT2 line select

b33	b32	b31	b30	L <sub>OUT12</sub> (37pin)	R <sub>OUT12</sub> (36pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

Audio OUT3 line select

b43	b42	b41	b40	L <sub>OUT3</sub> (35pin)	R <sub>OUT3</sub> (34pin)
0	0	0	0	Mute	Mute
0	0	0	1	L1	R1
0	0	1	0	L2	R2
0	0	1	1	L3	R3
0	1	0	0	L4	R4
0	1	0	1	L5	R5
0	1	1	0	L6	R6
0	1	1	1	L7	R7
1	0	0	0	L8	R8
1	0	0	1	L9	R9
1	0	1	0	L10	R10
1	0	1	1	Mute	Mute
1	1	0	0	Mute	Mute
1	1	0	1	Mute	Mute
1	1	1	0	Mute	Mute
1	1	1	1	Mute	Mute

■ Details of contents of control-5

**Audio GAIN SW**

**OUT1 (38, 39pin)**

b46	GAIN
0	0dB
1	6dB

**OUT2 (36, 37pin)**

b45	GAIN
0	0dB
1	6dB

**OUT3 (34, 35pin)**

b44	GAIN
0	0dB
1	6dB

**Audio Powersave**

**OUT1 (38, 39pin)**

b56	Conditions
0	Active
1	Powersave

**OUT2 (36, 37pin)**

b55	Conditions
0	Active
1	Powersave

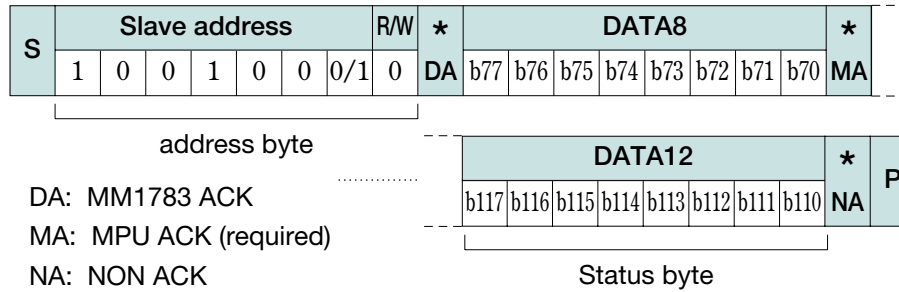
**OUT3 (34, 35pin)**

b54	Conditions
0	Active
1	Powersave

Phased Out Products

[Status register]

Status register is data to inform the master of the device status. The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers. As MM1783 slave address, either 91H or 93H can be selected according to the ADR terminal conditions. When ADR terminal is L, 91H is selected. Set the confirmation acknowledgement after the end of status register to non-ACK. The following figure shows the correspondence of the output data of status register.

Table of status registers

No.	DATA condition							
	b77	b76	b75	b74	b73	b72	b71	b70
DATA8			SW1 detect	DL1-1 detect		DL2-1 detect	DL3-1 detect	
DATA9			SW2 detect	DL1-2 detect		DL2-2 detect	DL3-2 detect	
DATA10			SW3 detect	DL1-3 detect		DL2-3 detect	DL3-3 detect	
DATA11	b107	b106	b105	b104	b103	b102	b101	b100
			S-1 detect	S2-1/FS1 detect		S-2 detect	S2-2/FS2 detect	
DATA12	b117	b116	b115	b114	b113	b112	b111	b110
			S-3 detect	S2-3/FS3 detect		S-4 detect	S2-4/FS4 detect	

■ Output data of status register & threshold

It is based on CPR1202 which is the specification of JEITA.

(Except where noted otherwise Ta=25°C, Vcc9=9V, Vcc5=5V)

S1~S4 (1, 7, 13, 19pin) detect

S1~S4 voltage	Conditions	S4	S3	S2	S1
		b112	b115	b102	b105
$GND \leq V_{DC} \leq 2.0V$	Connected	1	1	1	1
$3.0V \leq V_{DC} \leq V_{CC5}$	Unconnected	0	0	0	0

S2-1~S2-4 (3, 9, 15, 21pin) detect (Aspect)

S2-1~S2-4 voltage	Aspect	S2-4		S2-3		S2-2		S2-11	
		b111	b110	b114	b113	b101	b100	b104	b103
$GND \leq V_{DC} \leq 1.0V$	4 : 3	0	0	0	0	0	0	0	0
$1.3V \leq V_{DC} \leq 2.7V$	Letterbox	0	1	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{CC5}$	16 : 9	1	0	1	0	1	0	1	0

DL1-1, DL1-2, DL1-3 (81, 87, 93pin) detect (Scanning line)

DL1-1~DL1-3 voltage	Scanning line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
$GND \leq V_{DC} \leq 1.0V$	480	0	0	0	0	0	0
$1.3V \leq V_{DC} \leq 2.7V$	720	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{CC5}$	1080	1	0	1	0	1	0

DL2-1, DL2-2, DL2-3 (83, 89, 95pin) detect (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
$GND \leq V_{DC} \leq 2.7V$	Interlace	0	0	0
$3.5V \leq V_{DC} \leq V_{CC5}$	Progressive	1	1	1

DL3-1, DL3-2, DL3-3 (85, 91, 97pin) detect (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
$GND \leq V_{DC} \leq 1.0V$	4 : 3	0	0	0	0	0	0
$1.3V \leq V_{DC} \leq 2.7V$	Letterbox	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{CC5}$	16 : 9	1	0	1	0	1	0

SW1~SW3 (79, 78, 77pin) detect

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
$GND \leq V_{DC} \leq 2.0V$	Connected	1	1	1
$3.0V \leq V_{DC} \leq V_{CC5}$	Unconnected	0	0	0

It is based on EN50049-1 which is the specification of CENELEC. Please drop the voltage of FS terminal on resistance division(47kΩ&33kΩ), and input it.

(Except where noted otherwise Ta=25°C, Vcc9=9V, Vcc5=5V)

FS1~FS4 (3, 9, 15, 21pin) detect (Scanning Line)

FS1~FS3 voltage	Level	FS4		FS3		FS2		FS1	
		b111	b110	b114	b113	b101	b100	b104	b103
$GND \leq V_{DC} \leq 1.0V$	0	0	0	0	0	0	0	0	0
$1.5V \leq V_{DC} \leq 3.0V$	1A	0	1	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{cc5}$	1B	1	0	1	0	1	0	1	0

\*: Level 0 ...television broadcast reproduction

Level 1A ...reproduction of an external source with aspect ratio 16 : 9

Level 1B ...peritelevision reproduction

S1~S4 (1, 7, 13, 19pin) detect

S1~S4 voltage	Conditions	S4	S3	S2	S1
		b112	b115	b102	b105
$GND \leq V_{DC} \leq 2.0V$	Connected	1	1	1	1
$3.0V \leq V_{DC} \leq V_{cc5}$	Unconnected	0	0	0	0

S2-1~S2-4 (3, 9, 15, 21pin) detect (Aspect)

S2-1~S2-4 voltage	Aspect	S2-4	S2-3	S2-2	S2-1
$GND \leq V_{DC} \leq 1.0V$	4 : 3	↓	↓	↓	↓
$1.3V \leq V_{DC} \leq 2.7V$	Letterbox	FS4	FS3	FS2	FS1
$3.5V \leq V_{DC} \leq V_{cc5}$	16 : 9				

DL1-1, DL1-2, DL1-3 (81, 87, 93pin) detect (Scanning Line)

DL1-1~DL1-3 voltage	Scanning line	DL1-3		DL1-2		DL1-1	
		b94	b93	b84	b83	b74	b73
$GND \leq V_{DC} \leq 1.0V$	480	0	0	0	0	0	0
$1.3V \leq V_{DC} \leq 2.7V$	720	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{cc5}$	1080	1	0	1	0	1	0

DL2-1, DL2-2, DL2-3 (83, 89, 95pin) detect (I/P)

DL2-1~DL2-3 voltage	I/P	DL2-3	DL2-2	DL2-1
		b92	b82	b72
$GND \leq V_{DC} \leq 2.7V$	Interlace	0	0	0
$3.5V \leq V_{DC} \leq V_{cc5}$	Progressive	1	1	1

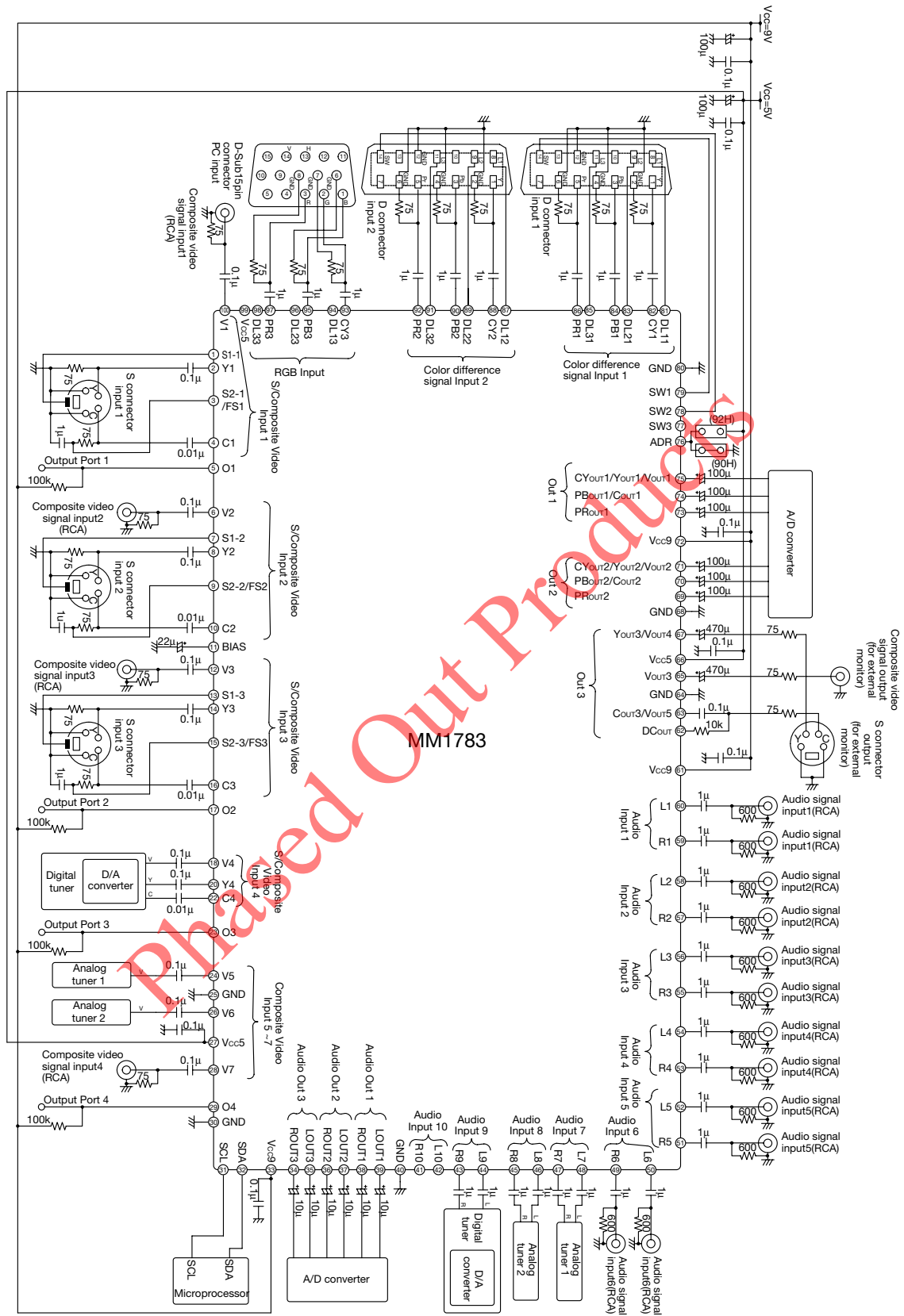
DL3-1, DL3-2, DL3-3 (85, 91, 97pin) detect (Aspect)

DL3-1~DL3-3 voltage	Aspect	DL3-3		DL3-2		DL3-1	
		b91	b90	b81	b80	b71	b70
$GND \leq V_{DC} \leq 1.0V$	4 : 3	0	0	0	0	0	0
$1.3V \leq V_{DC} \leq 2.7V$	Letterbox	0	1	0	1	0	1
$3.5V \leq V_{DC} \leq V_{cc5}$	16 : 9	1	0	1	0	1	0

SW1~SW3 (79, 78, 77pin) detect

SW1~SW3 voltage	Conditions	SW3	SW2	SW1
		b95	b85	b75
$GND \leq V_{DC} \leq 2.0V$	Connected	1	1	1
$3.0V \leq V_{DC} \leq V_{cc5}$	Unconnected	0	0	0

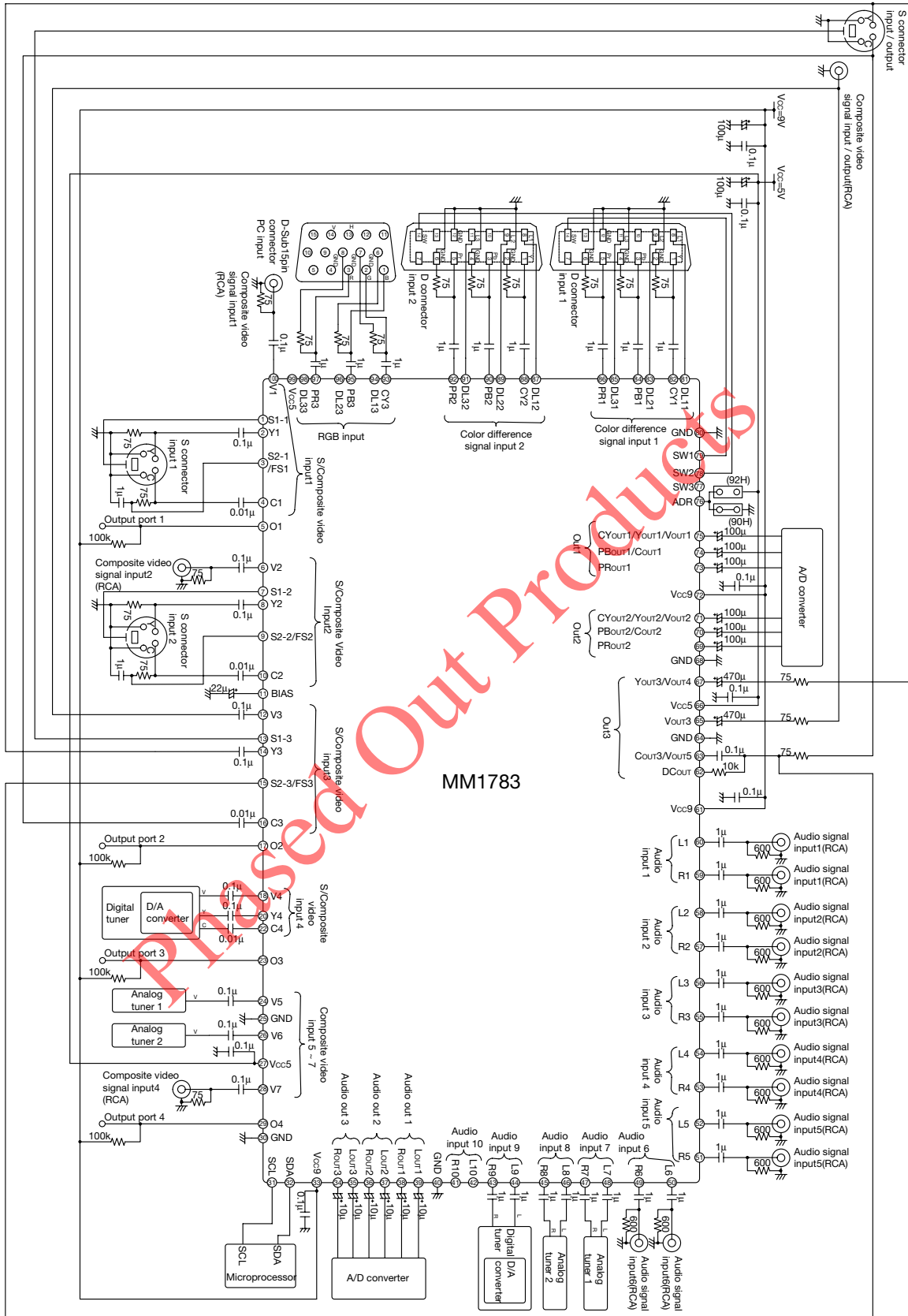
Application Circuit 1



Note: Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

- We shall not be liable for any trouble or damage caused by using this circuit.
- In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.

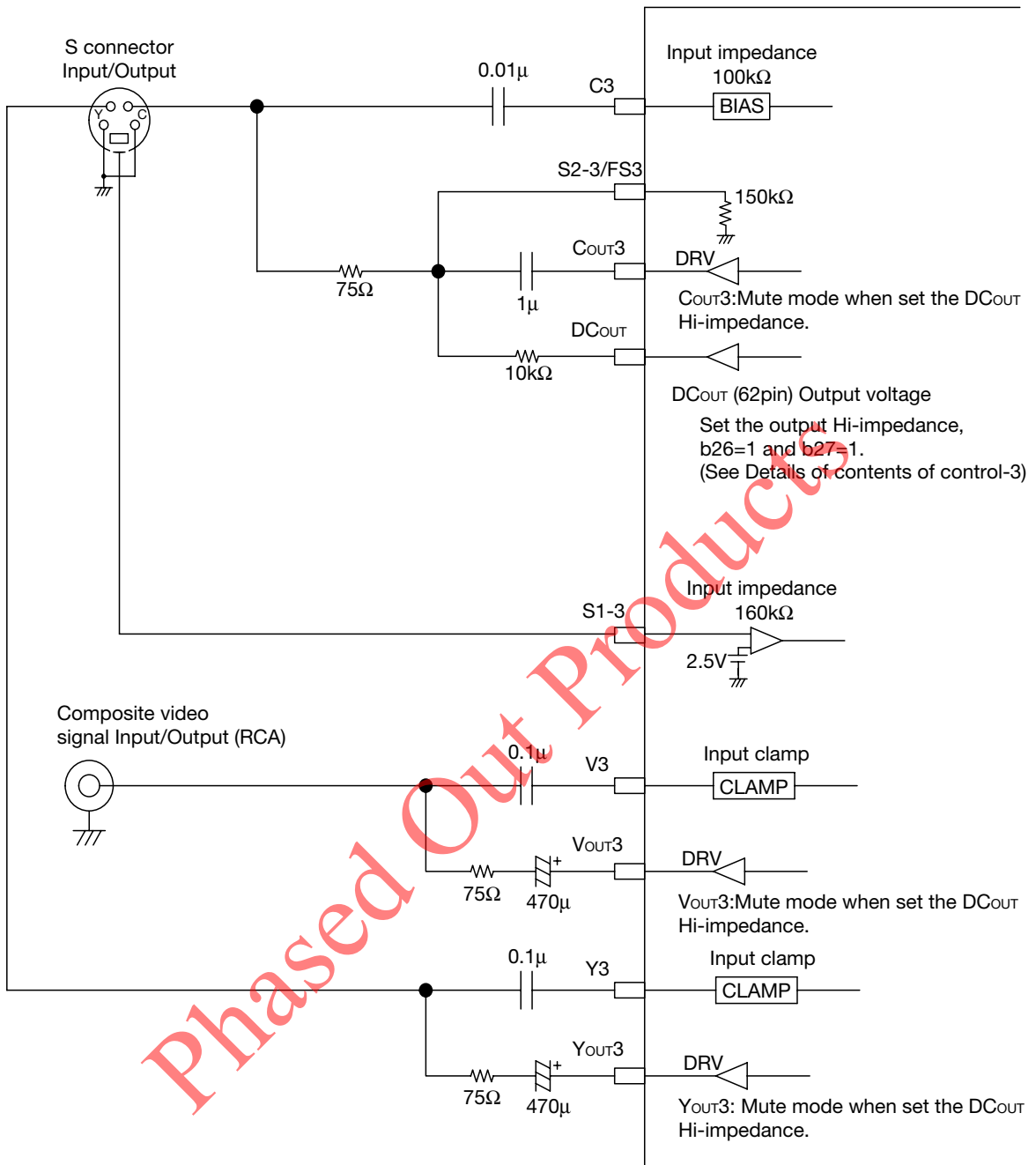
Application Circuit 2



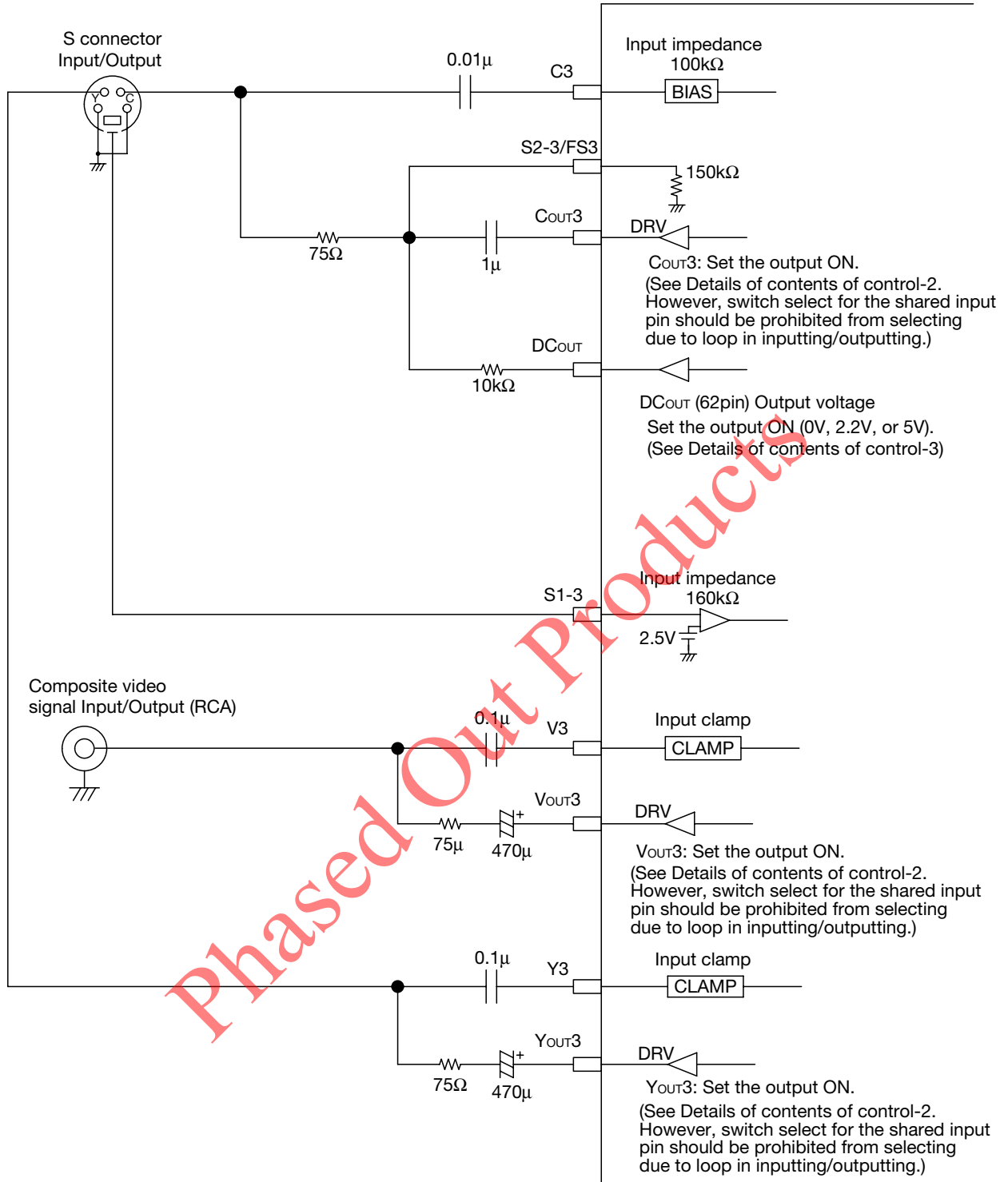
Note: Be careful because a DC voltage changes when you short an adjoining terminal by the resistance.

- We shall not be liable for any trouble or damage caused by using this circuit.
- In the event a problem which may affect industrial property or any other rights of us or a third party happens during the use of information in these circuit, we shall not be liable for any problem, nor grant a license therefore.

■ Application circuit as an output or an input pin  
 (1) Settings when used as an input pin

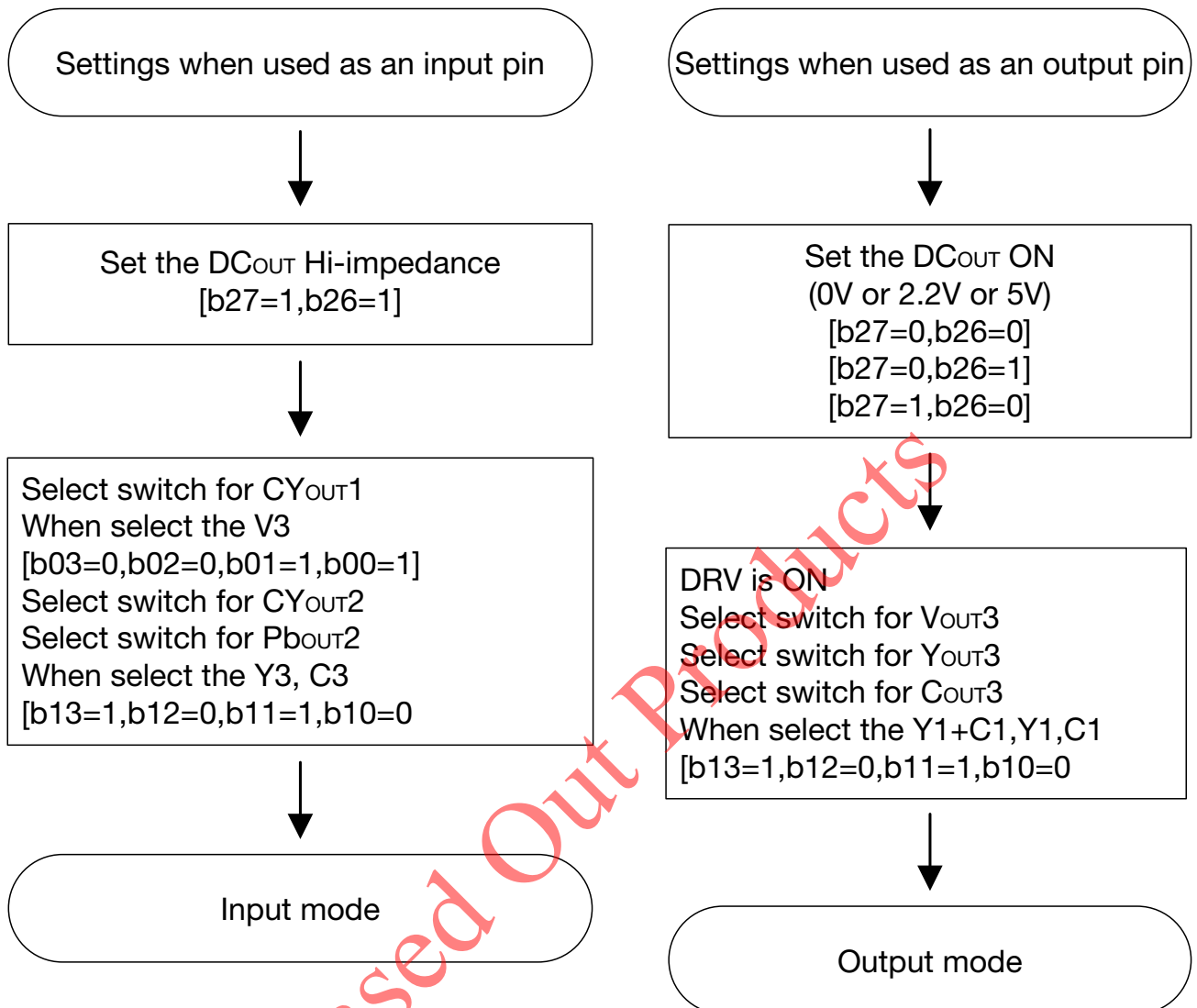


(2) Settings when used as an output pin



■ Flowchart for applications as an output or an input pin

This is a flowchart applying to the Application Circuit2

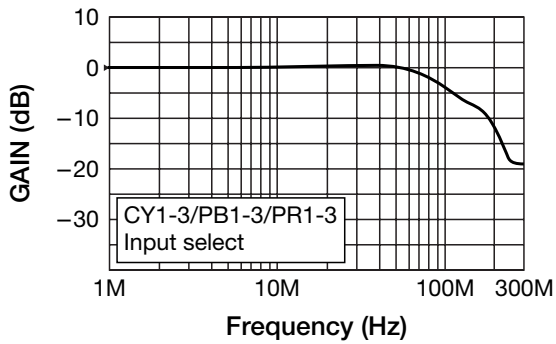


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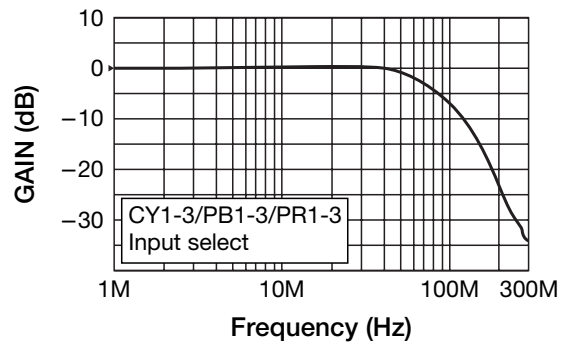
**Characteristics**

Frequency characteristic

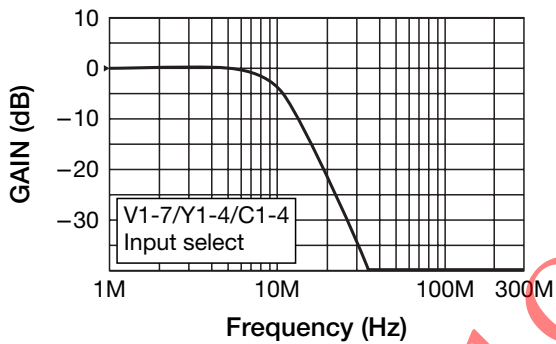
■ OUT1 THRU 0dB



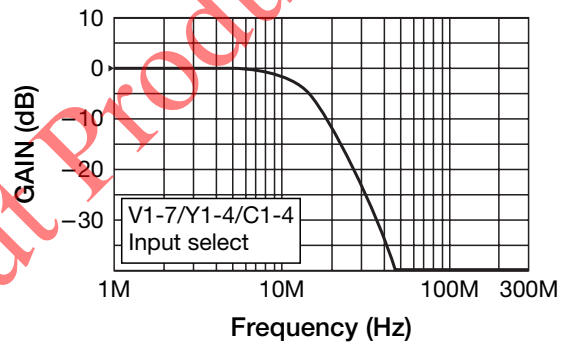
■ OUT2 THRU 0dB



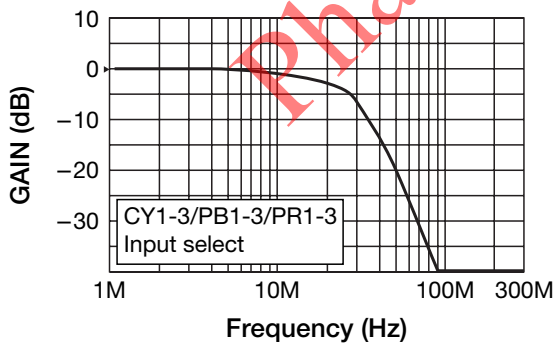
■ OUT1, 2 LPF1 (fc=6.75MHz) 0dB



■ OUT1, 2 LPF2 (fc=13.5MHz) 0dB



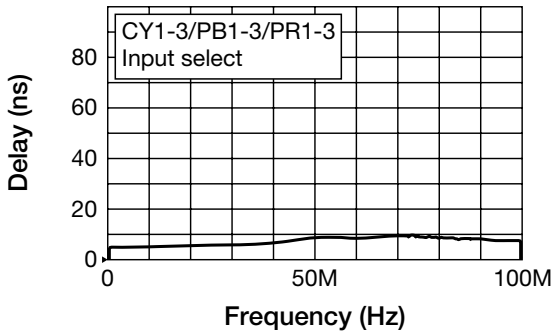
■ OUT1, 2 LPF3 (fc=24MHz) 0dB



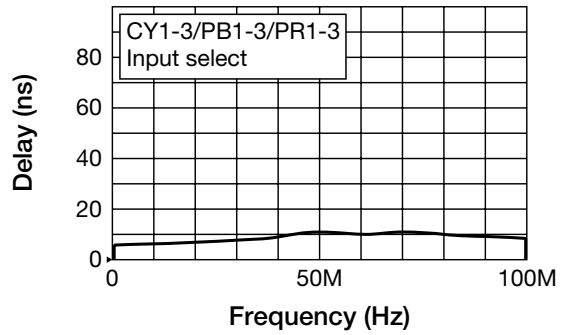
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Group delay

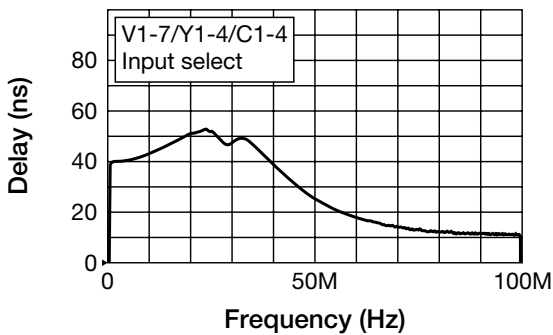
■ OUT1 THRU



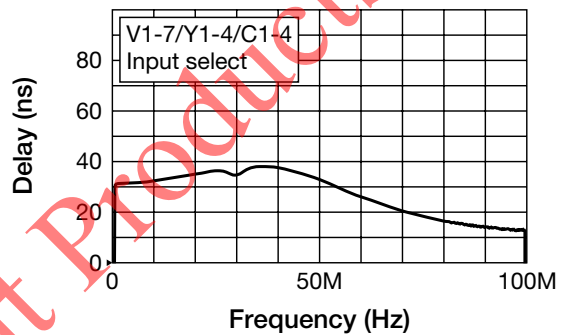
■ OUT2 THRU



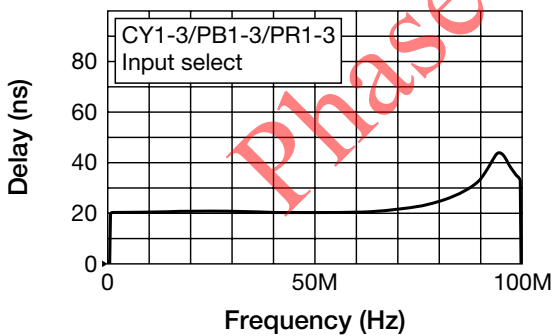
■ OUT1, 2 LPF1 (fc=6.75MHz)



■ OUT1, 2 LPF2 (fc=13.5MHz)



■ OUT1, 2 LPF3 (fc=24MHz)



Phased Out Product